AN10063

ISP1301 power pins interfacing

Rev. 02 — 11 February 2010 **Application note**

Document information

Info	Content
Keywords	isp1301, usb, power source, por
Abstract	This document contains information on how to interface with the ISP1301 transceiver.

ST ERICSSON

Revision history

Rev	Date	Description
02	20100211	Rebranded to the ST-Ericsson template.
01	20060703	First release.

Contact information

For additional information, please visit: http://www.stericsson.com

For document related queries, please send an email to: wired.support@stericsson.com

1. Introduction

The ISP1301 is a Universal Serial Bus (USB) On-The-Go (OTG) transceiver device that is ideal for use in portable electronic devices, such as mobile phones, digital still cameras, digital video cameras, Personal Digital Assistants (PDAs) and digital audio players. It allows USB Application-Specific Integrated Circuits (ASICs), Programmable Logic Devices (PLDs) and any system chip set (with the USB host or device function built-in but without the USB physical layer) to interface to the physical layer of the USB.

This document demonstrates interfacing of the ISP1301 transceiver.

2. Interfacing

Fig 1 shows the ISP1301 interfacing block diagram.

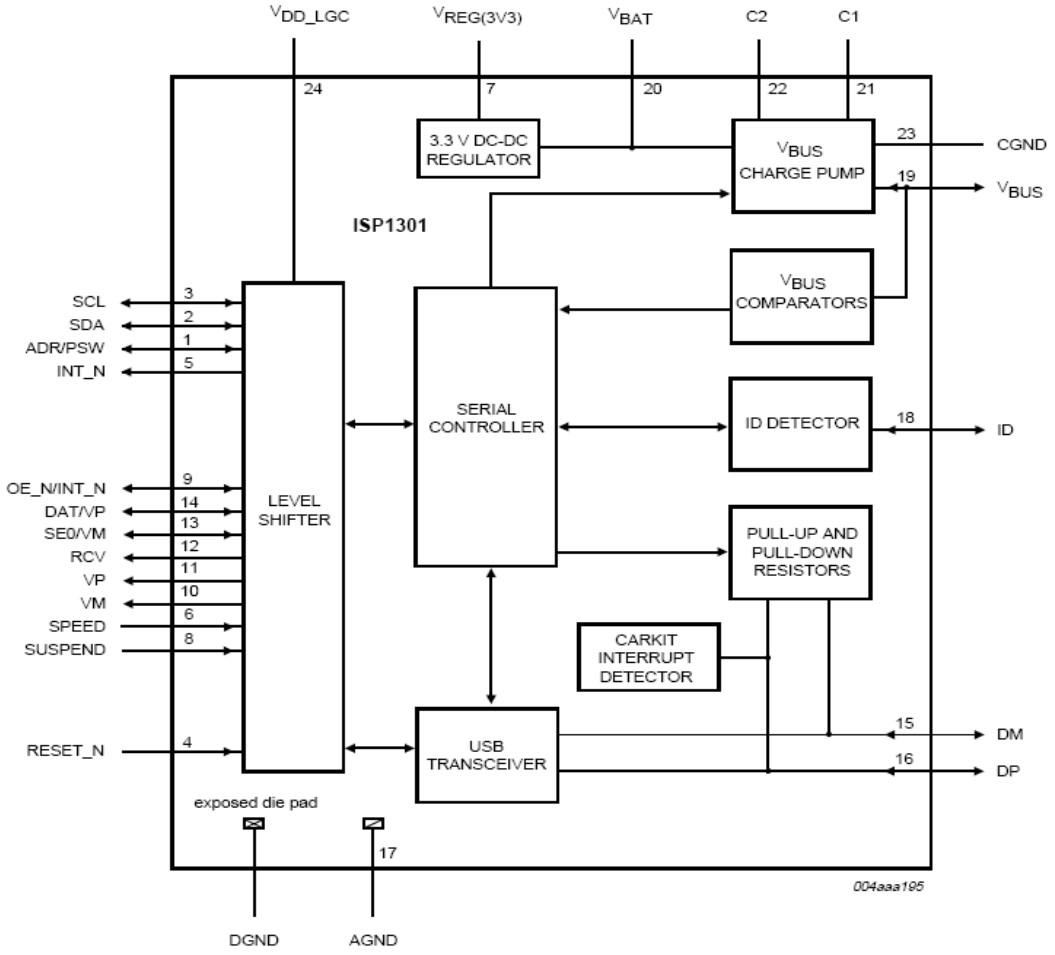

Fig 1. ISP1301 block diagram

2.1 Points to take into consideration

2.1.1 Current found on the V_{BAT} pin without V_{DD_LGC}

When V_{BAT} is directly connected to the battery (without the presence of V_{DD_LGC}), there will be about 300 μA of leakage current on V_{BAT}. V_{DD_LGC} will only be available after the phone is switched on. This leakage current is because the chip is not configured to be fully powered-down when it is first turned on. To ensure that the ISP1301 stays in global power-down mode, set bit GLOBAL_PWR_DN in the Mode Control 2 register to logic 1 before the phone is powered down. The leakage current of 300 μA will be reduced to less than 20 μA, which is the power-down mode current ($I_{BAT(pd)}$) even when V_{DD_LGC} is not present.

Fig 2 shows V_{BAT} directly connected to the battery.

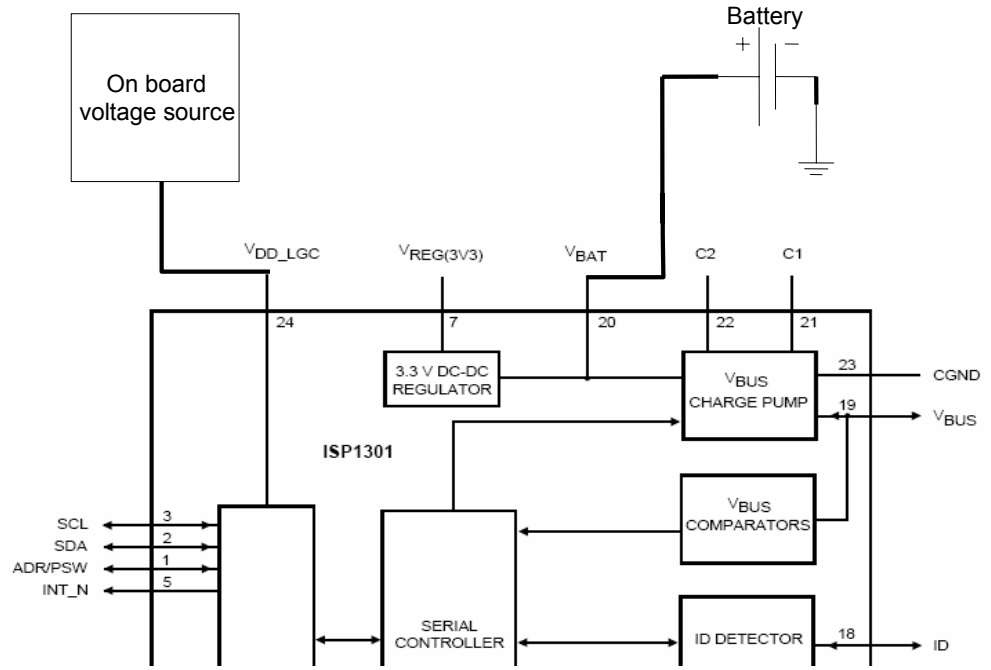

Fig 2. Connecting V_{BAT} directly to the battery

Another way to remove the leakage current on the V_{BAT} pin is to connect V_{BAT} and V_{DD_LGC} to the same voltage source. In this way, both the voltage sources will be present at the same time, so that the software can always initialize the GLOBAL_PWR_DN bit to make sure that the ISP1301 is set to power-down mode. Note that in this connection, the voltage range must be between 2.7 V to 3.6 V.

Fig 3 shows V_{BAT} connected to V_{DD_LGC}, no leakage current issue.

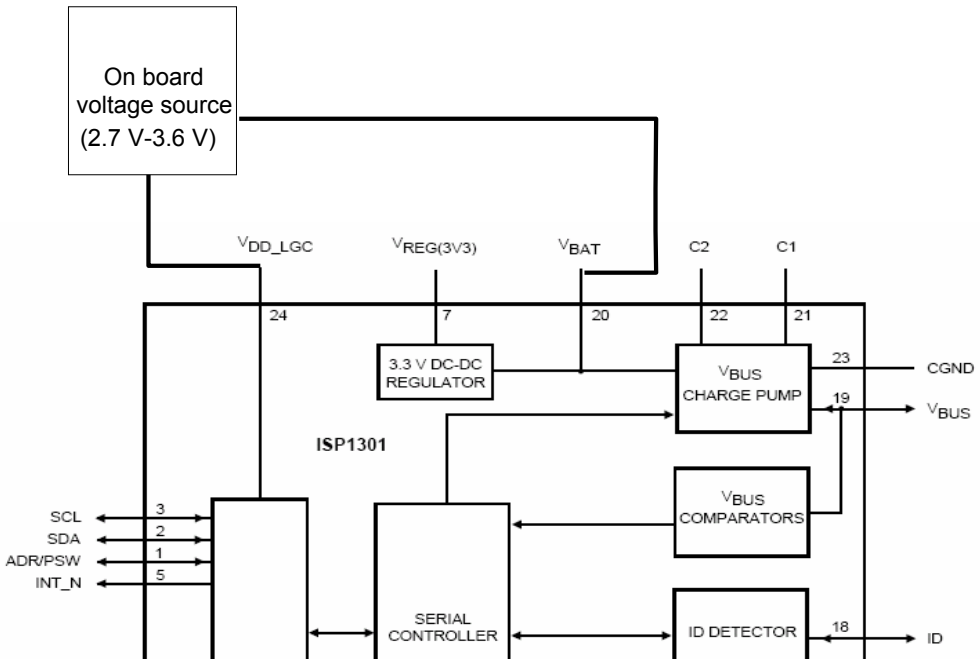

Fig 3. V_{BAT} connected to V_{DD_LGC}

2.1.2 SDA line pulled LOW during power-on process

With V_{BAT} and V_{DD_LGC} are connected to the same voltage source, sometimes the SDA line will be driven LOW during power-up. This will cause problem for the I^2C-bus operation. In some application systems this might affect other I^2C-bus devices, such as SDA will be permanently driven LOW by other devices.

Fig 4 shows the waveform of power-up for SDA and V_{DD_LGC}. When V_{DD_LGC} is less than 0.7 V, SDA is in high-impedance state, so it follows the V_{DD_LGC} voltage from external pull-up resistor. When V_{DD_LGC} is above 0.7 V, SDA may be driven to LOW by internal logic that is powered by VREG3V3 because VREG is lower than V_{DD_LGC}. When VREG rises above POR threshold (2.0V), the internal logic will reset and SDA will be in high-impedance.

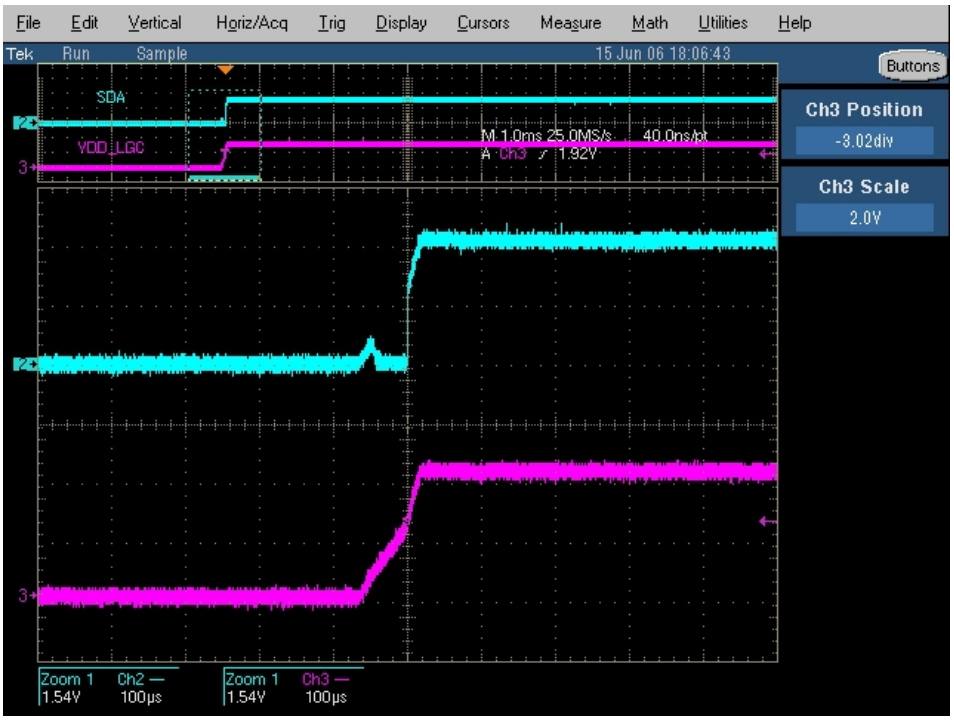

Fig 4. Waveform showing SDA line driven LOW until POR occurs and resets

To avoid SDA from driving LOW during power-up, it is recommended that you connect VREG3V3 together with V_{BAT} and V_{DD_LGC}. In this case, all the three voltages rise at the same time therefore SDA will not be driven LOW by the ISP1301.

Fig 5 shows V_{BAT}, V_{DD_LGC} and V_{REG3V3} connected to the same voltage source.

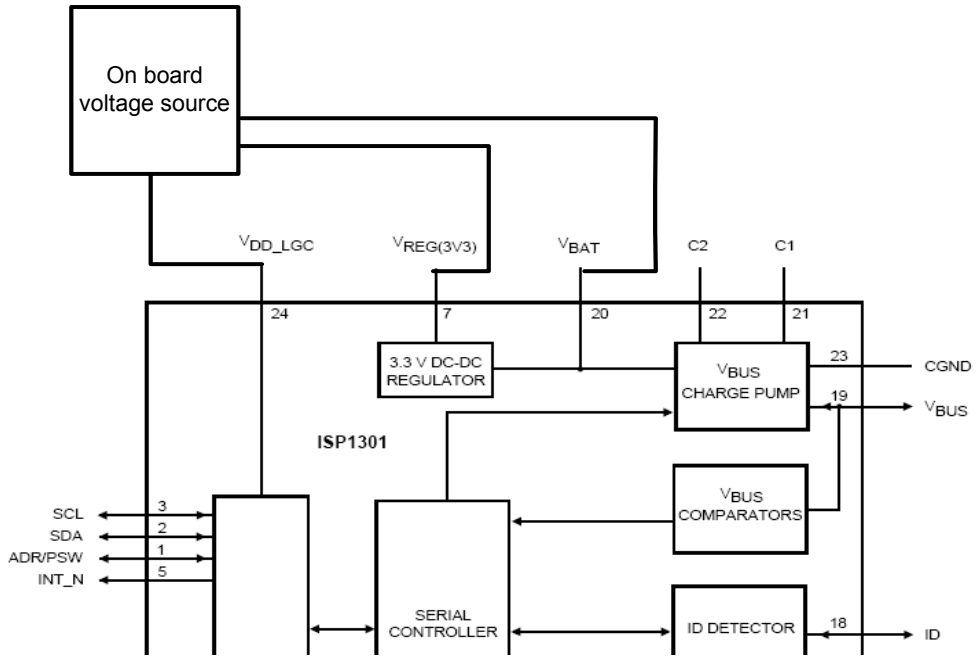

Fig 5. Connecting V_{BAT}, V_{DD_LGC} and V_{REG3V3} to the same voltage source

Fig 6 shows no delay if VREG3V3 is connected to V_{BAT} and V_{DD_LGC}.

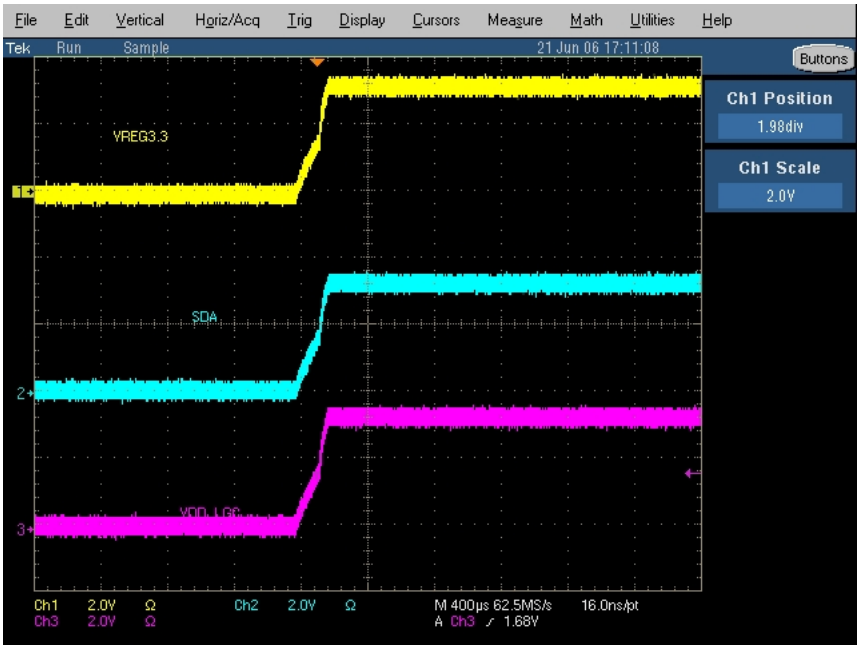

Fig 6. Waveform when VREG3V3 is connected to V_{BAT} and V_{DD_LGC}

2.1.3 ADR_REG bit

There is no ADR_REG bit because it is just a latch value depending on the pull-up or pull-down resistor that is connected to the ADR/PSW_N pin. To set the ADR/PSW pin to be an output, you need to set the PSW_OE bit to logic 1. Then the logic level of the ADR/PSW output will be determined by the ADR_REG value from the latch.

Fig 7 shows the latching value of the ADR_REG bit.

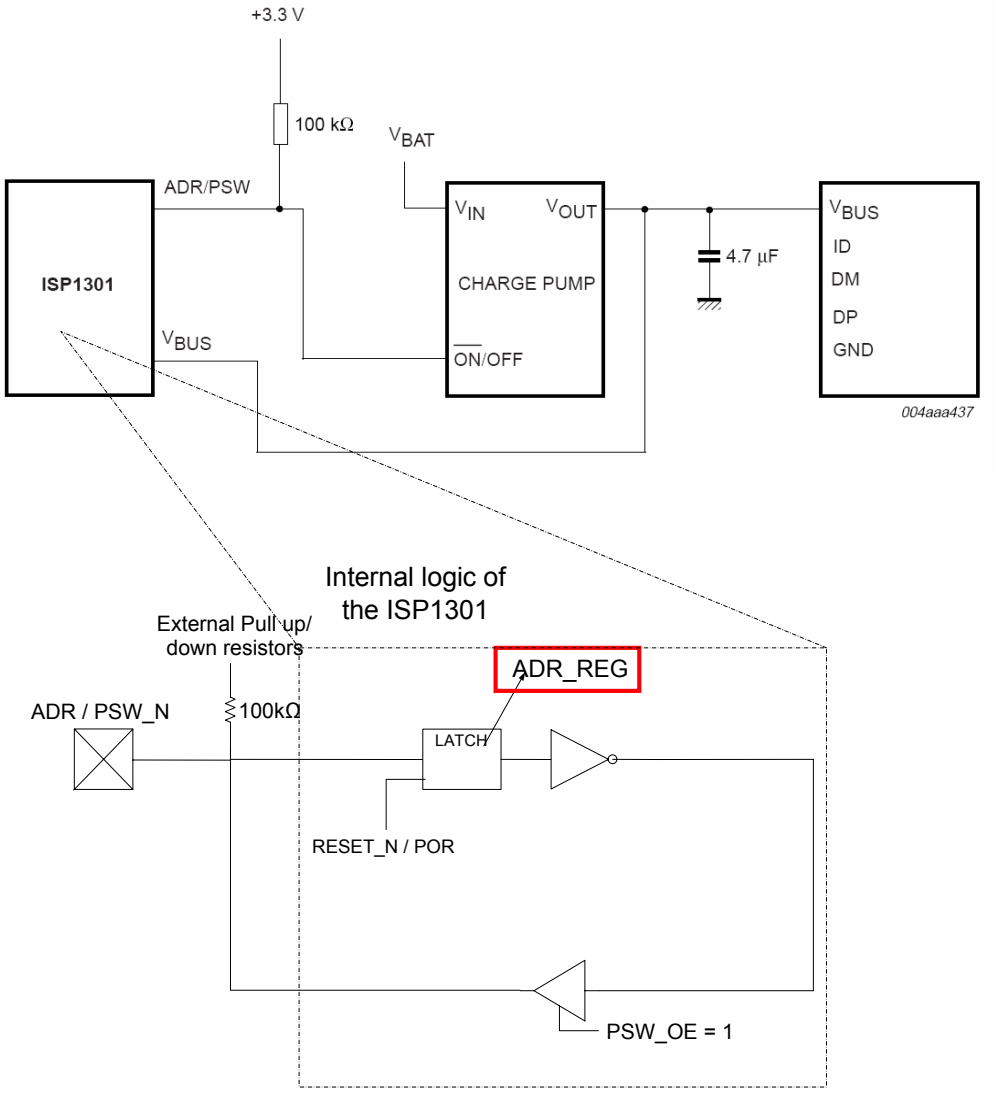

Fig 7. Latching value of the ADR_REG bit

3. Legal information

Please Read Carefully:

The contents of this document are subject to change without prior notice. ST-Ericsson makes no representation or warranty of any nature whatsoever (neither expressed nor implied) with respect to the matters addressed in this document, including but not limited to warranties of merchantability or fitness for a particular purpose, interpretability or interoperability or, against infringement of third party intellectual property rights, and in no event shall ST-Ericsson be liable to any party for any direct, indirect, incidental and or consequential damages and or loss whatsoever (including but not limited to monetary losses or loss of data), that might arise from the use of this document or the information in it.

Contact information at www.stericsson.com under Contacts

www.stericsson.com

4. Contents

For more information, please visit: http://www.stericsson.com
For document related queries, email to: wired.support@stericsson.com

Date of release: 11 February 2010
Document identifier: CD00264983