AS8579

Capacitive Sensor with I and Q

General Description

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Key Benefits and Features

The benefits and features of this device are listed below:

Figure 1: Added Value of Using AS8579

Benefits	Features
Accurate capacitive measurement	I and Q
Higher durability and lower system costs (no shield needed)	Magnetic stray field immunity
Enabler for safety critical applications	Functional safety, diagnostics
Suitable for automotive applications	AEC-Q100 Grade 1 qualified

Applications

The AS8579 is ideal for automotive applications.

Revision History

Revision	Date	Owner	Description
0.1	03.07.2018	rei	Initial Version
0.2	17.07.2018	rei	Added Diagnostic
0.3	19.07.2018	jhua	Added System Timing vs. ADCTL setting Added Pin-Diagramm
0.4	21.08.2018	rei	Changed Disclaimer
0.5	06.09.2018	jhua	Added Sensing Range
0.6	20.09.2018	jhua	Changed Register in Single Conversion Description
0.7	27.09.2018	jhua	Added Register description for TXV, BLANK and PLUS/MINUS Added Flowchart of functional behavior
0.8	18.10.2018	jhua	Changed OTPF SM description
0.9	05.11.2018	jhua	Status register Bitposition changed SPI description updated

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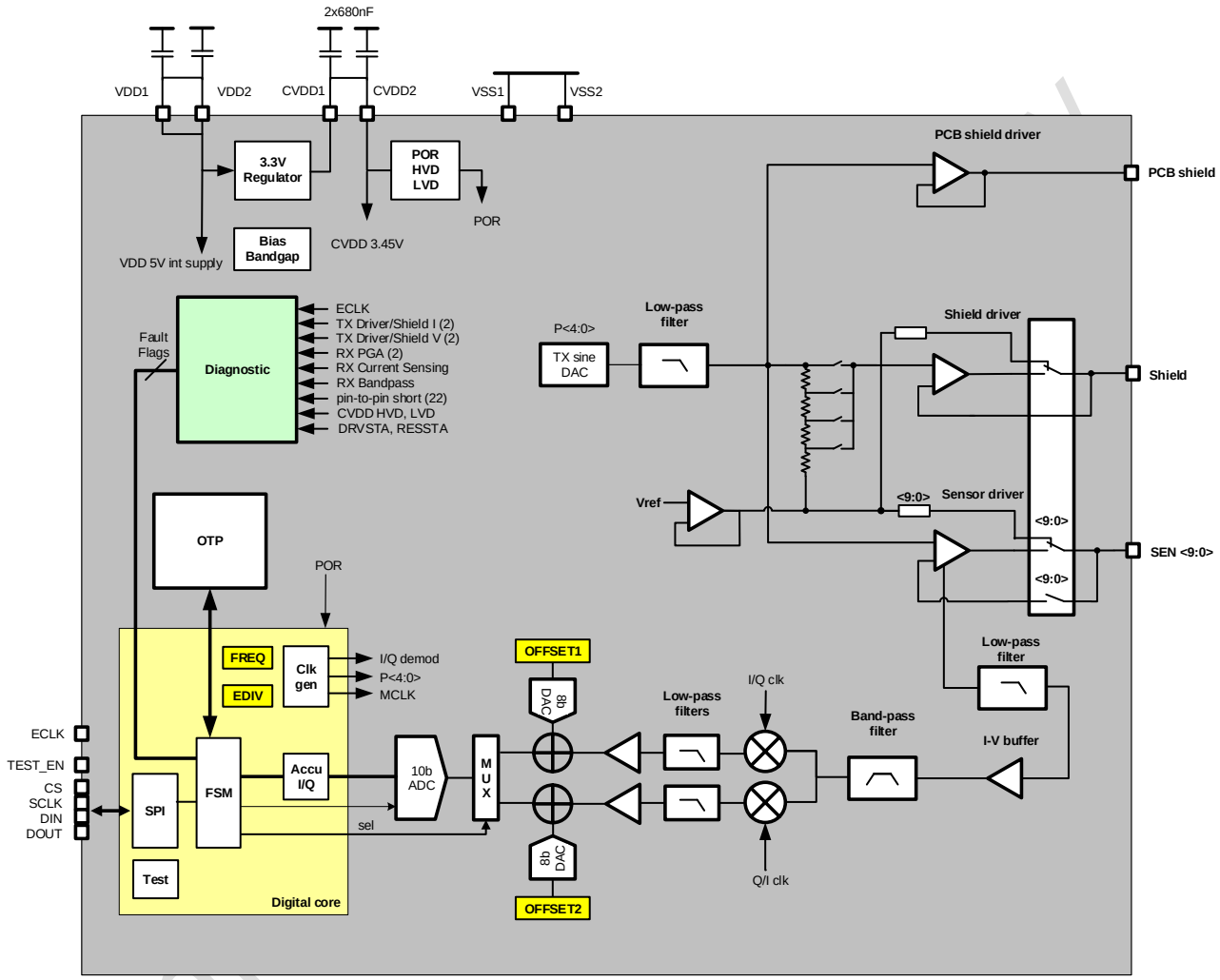
Block Diagram

The functional blocks of this device are shown below:

Figure 2: Functional Blocks of the AS8579



(*) detailed safety mechanism information can be found in chapter Diagnostic

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Pin Assignment

Pin Diagram

Figure 3: AS8579 Pin Assignment (top view, SSOP24)

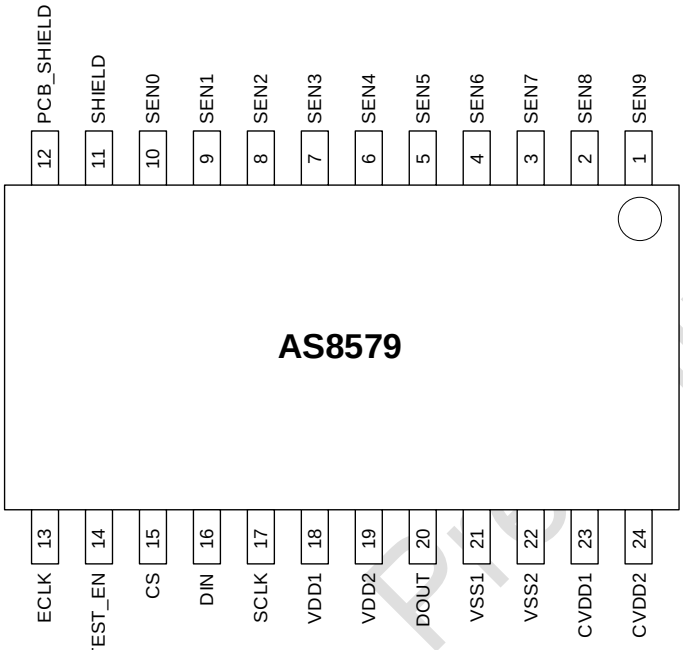

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Figure 4: AS8579 Pin Description

Pin Number	Name	Type	Description
1	SEN9	AIO 0 Ohm	Sensor
2	SEN8	AIO 0 Ohm	Sensor
3	SEN7	AIO 0 Ohm	Sensor
4	SEN6	AIO 0 Ohm	Sensor
5	SEN5	AIO 0 Ohm	Sensor
6	SEN4	AIO 0 Ohm	Sensor
7	SEN3	AIO 0 Ohm	Sensor
8	SEN2	AIO 0 Ohm	Sensor
9	SEN1	AIO 0 Ohm	Sensor
10	SEN0	AIO 0 Ohm	Sensor
11	SHIELD	AIO 0 Ohm	Driven Shield
12	PCB_SHIELD	AIO 0 Ohm	PCB Driven Shield or analog test mode output
13	ECLK	PI_PD	System clock
14	TEST_EN	PI_PD AIO 0 Ohm	Test enable Analog test input
15	CS	PI_PD	SPI chip select
16	DIN	PI_PD	SPI data in
17	SCLK	PI_PD	SPI clock
18	VDD1	S	External 5V supply
19	VDD2	S	External 5V supply
20	DOUT	DO	SPI data out
21	VSS1	S	Ground
22	VSS2	S	Ground
23	CVDD1	S	Internal 3.45V supply
24	CVDD2	S	Internal 3.45V supply

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Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings “may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
VDD	DC Supply Voltage at VDD pin	-0.3	7	V	Not operational
VDC_IO	DC Voltage at digital IO pins	-0.3	VDD + 0.3	V	
VDC_SEN	Sensor analog pins (SENx, Shield)	-0.3	20	V	
ISCR	Input Current (latch-up immunity)	+/-100		mA	Norm: AEC-Q100-004
Electrostatic Discharge					
ESD_HBM	Electrostatic Discharge HBM	+/-2		kV	Norm: AEC-Q100-002
ESD_MM	ESD-Machine Model	125		V	Norm: AEC-Q100-003
ESD_CDM	ESD – Charged Device Model	750		V	For reference only
Temperature Ranges and Storage Conditions					
T_{AMB}	Operating temperature range	-40	+125	°C	
T_J	Operating temperature range	-40	150	°C	
TaProg	Programming Temperature	5	45	°C	Programming@ Room temperature (25°C +/- 20°C)
T_{STRG}	Storage Temperature Range	-55	+150	°C	
T_{BODY}	Package Body Temperature		+260	°C	The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.” The lead finish

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					for Pb-free leaded packages is “Matte Tin” (100% Sn)
RH_{NC}	Relative Humidity non-condensing	5	85	%	
MSL	Moisture Sensitive Level	3			Represents a maximum floor life time of 168 hours
Bump Temperature (soldering)					
T_{PEAK}	Operating Temperature	235	245	°C	Peak Temperature
t_{WELL}	Junction to Ambient Thermal Resistance	30	45	S	Well Time above 217°C

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

All in this datasheet defined tolerances for external components need to be assured over the whole operation conditions range and also over lifetime.

Overall condition: Tamb= -40°C to 125°C Components spec; unless otherwise noted

Figure 6: Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD	Positive supply voltage	Static condition	4.8		5.2	V
CVDD	Regulator Voltage		3.3	3.45	3.6	V
IDD_1	Dynamic Supply Current average	ECLK =48MHz, SCLK= 8MHz, FREQ = 125kHz Drivers enabled			50	mA
IDD_2	Dynamic Supply Current average	ECLK =48MHz, SCLK= 8MHz, FREQ = 125kHz Drivers disabled			15	mA
I_VL	Input Low Voltage	ECLK, CS, SCLK, DIN,	VSS		0.3*VDD	V
I_VH	Input high voltage	ECLK, CS, SCLK, DIN,	VSS		VDD	V
I_PD	Pull-down value	ECLK, CS, SCLK, DIN,	0.7*VDD		100	µA

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ECLK_F	ECLK frequency		3		50	MHz
SCLK_F	SCLK frequency				10	MHz
O_VL	Output low voltage	DOUT	VSS		0.4	V
O_VH	Output high voltage	DOUT	4.0		VDD	V
O_IOUT	Output current	DOUT			4	mA
O_PD	Pull-down value	DOUT	30		200	kΩ

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System Specification

Figure 7: Analog Front End

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AFE_TS	Measurement settling time				400	µs
SCT	System Cycle Time				752	µs
AFE_SENS	System Sensitivity	At PGA=0, CBG=0, TXV=2, FREQ=3	9.375	12.5	15.625	LSB/pF
AFE_LIN	Overall system linearity	Sensor capacitance range 0 to 2nF			1	%
AFE_RI	Resistive in-phase parasitic current	Limits the max. capacitance at CBG=0 and TXV=2	0.1	0.3	0.5	mApk
AFE_N	System noise	On I or Q registers 3σ noise referenced to full scale			±0.2	%
PSR	System power supply rejection				±20	lsb
AFE_VMM	Output voltage mismatch between drivers				1	%
AFE_PMM	Output Phase mismatch between drivers				2	Deg
AFE_ROUT1	SENx outputs, Shield Driver, PCB Shield Driver output impedance (incl. MUX)				10	Ω
AFE_ROUT2	SENx Output DC resistance		3.5	5	6.5	kΩ
AFE_ROUT0	SENx Output DC resistance	MODE=0 at one pin, other SENx grounded Vpin>0.2V	10*			MΩ
AFE_RI	Sensor crosstalk impedance	Differential impedance between	5			MΩ

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		SENx pins at transmitter frequencies				
AFE_CAP	Output Capacitance				8	pF
AFE_DCAP	Driver Output Capacitance drift over temp / lifetime				0.5	pF
AFE_GMM	I to Q channel overall gain mismatch				2	%
AFE_HD	Driver Harmonic Level				10	mV

The Sensor Driver has the ability to drive a continuously changing load of 20pF to 2000pF in parallel with 5k□, with a 1.0Vp-p AC term over a frequency range of 45KHz – 125KHz.

The driver (gain 1V/V) provides a low impedance output to drive the outputs (SEN0 – SEN9)

Figure 8: TX Driver and current sensing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TXDRV_VDC	Output DC voltage		1.18	1.23	1.28	Vpp
TXDRV_AC2	Output voltage, TXV=2		1.020	1.070	1.120	Vpp
TXDRV_AC1	Output voltage, TXV=1		0.510	0.535	0.560	Vpp
ATXDRV_IOUT	Output AC peak current				0.425	mA
TXDRV_IRX	Current sensing scaling factor			1		mA/mA
AFE_ROUT	Output imped-ance closed loop				10	Ω

Figure 9: RX ADC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RES_ADC	Resolution			10		Bit
DNL_ADC	Differential Nonlinearity		-1.5		+1.5	LSB
INL_ADC	Nonlinearity		-3		+3	LSB
OFFS_ADC	Offset error		-6		6	LSB

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Figure 10: RX Offset DACS I and Q Channels

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RES_DAC	Resolution			8		Bit
DNL_DAC	Differential Nonlinearity		-3		+3	LSB
INL_DAC	Nonlinearity		-0.5		+0.5	LSB

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Detailed Description

The transceiver Analog Front-end (AFE) architecture performs the primary function of the ASIC, which is to sense the load impedance. This is done using transmitter and receiver blocks. The transmitter block creates a sine wave across the load. The receiver block then detects the current response of the load. The current response is converted to a voltage and then demodulated into in phase (I) and quad-rature (Q) components. I and Q components are then filtered and converted to 10-bit digital words. These I & Q words are accumulated awaiting 16-bit SPI transmission.

Current response can be measured on any of the 10 pins connected to the Sensor Driver through analog multiplexers (MUX). The external processor controls the MUX. The processor retrieves the I and Q components of each sensor from AS8579 and then determines the size of the impedance load of the external sensor(s).

There are four selectable non-harmonic sensor frequencies: 45.45kHz, 71.43kHz, 100kHz and 125kHz.

TIA

The current to voltage function is implemented with a programmable transimedance amplifier

Figure 11: TIA

Symbol	Program Parameter	Conditions	Min	Typ	Max	Unit
TIA_A0	0x00		16.2	18	19.8	kOhm
TIA_A1	0x01		8.1	9	9.9	kOhm
TIA_A2	0x10		4.05	4.5	4.95	kOhm
TIA_A3	0x11		2.02	2.25	2.47	kOhm

Programmable Gain and Summing Amplifier

The demodulated and filtered DC signals are amplified by a PGA, where the Offsets Signal are summed up. I-Q Signals paths share a programmable common gain.

Figure 12: RX ADC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PGA_GM	I to Q Gain Mismatch				1	%
PGA_G0			-34.56	-36	-37.44	V/V
PGA_G1			-23.04	-24	-25	V/V
PGA_G2			-15.36	-16	-16.64	V/V
PGA_G3			-10.24	2.25	2.47	V/V
PGA_G4			-6.83	-7.11	-7.40	V/V
PGA_G5			-4.55	-4.74	-4.93	V/V

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PGA_G6			-3.03	-3.16	-3.29	V/V
PGA_G7			-2.02	-2.11	-2.19	V/V
PGA_G8			-19.2	-20	-20.8	V/V
PGA_OFR	Offset voltage		CVDD*2/255		CVDD-CVDD*2/255	V
PGA_VOS	Input offset		10		-10	mV
PGA_OR	Output DC Voltage range		0.2		CVDD-0.2	V

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SPI Interface

The Sensor contains a single serial peripheral interface (SPI), consisting of Serial Clock (SCLK), Data Out (DOUT), Data In (DIN), and Chip Select (CS) pins. The ASIC is configured as a SPI slave. The SPI interface is used to access Control, Status, and Data registers in the ASIC.

The CS input selects this device for serial transfers. CS is active high. Register data is shifted in the DIN pin and shifted out the DOUT pin on each subsequent SCLK. The CS input has a pull-down internal to the ASIC, which pulls this pin to the negated state should an open circuit condition occur.

The SCLK input is the clock signal input for synchronization of serial data transfer. When CS is asserted, both the SPI master and the slave latch input data on the rising edge of SCLK. The SPI master typically shifts data out on the falling edge of SCLK, as does this device. SCLK input has a pull-down internal to the ASIC which pulls this pin to the negated state should an open circuit condition occur. SCLK can idle in either state (high or low).

The DOUT output pin is in a tri-state condition when CS is low. Data is transmitted on DOUT MSB first. DOUT has a weak pull-down to set the bus to a defined state when the output is in tri-state mode.

DIN takes data from the master microprocessor while CS is asserted. Data is received MSB first. DIN has a pull-down internal to the ASIC which pulls this pin to the negated state should an open circuit condition occur

Figure 13: SPI Timing

	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	t_{SCK}	SCLK Period		125			ns
2	t_{LEAD}	Enable Lead Time		16.25			ns
3	t_{LAG}	Enable Lag Time		12.5			ns
4	t_{SCKHS}	SCLK High Time		25			ns
5	t_{SCKLS}	SCLK Low Time		25			ns
6	t_{SUS}	DIN Input Setup Time		5			ns
7	t_{HS}	DIN Input Hold Time		5			ns
8	t_{A}	DOUT Access Time				50	ns
9	t_{DIS}	DOUT Disable Time				25	ns
10	t_{VS}	DOUT Output Valid Time				20	ns
11	t_{HO}	DOUT Output Hold Time		0			ns
12	t_{RO}	Rise Time				7.2	ns
13	t_{FO}	Fall Time				7.5	ns
14	t_{CS_N}	CS_N Negated Time		50			ns
15	f_{OP}	Transfer Frequency		DC		8	MHz

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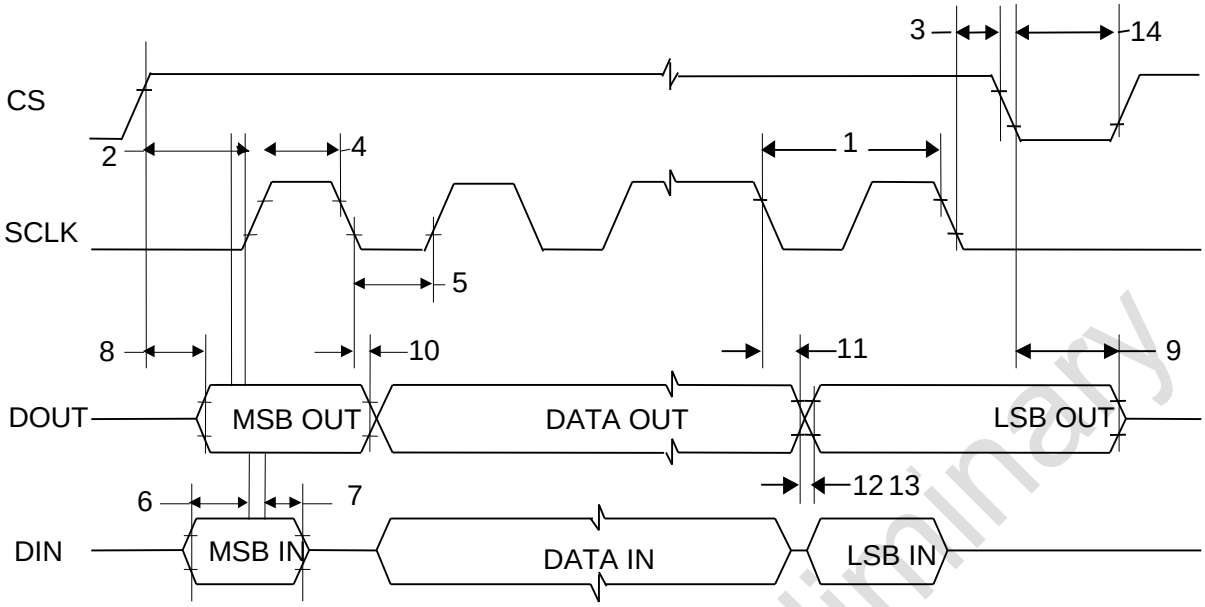
Figure 14: SPI Timing Diagramm



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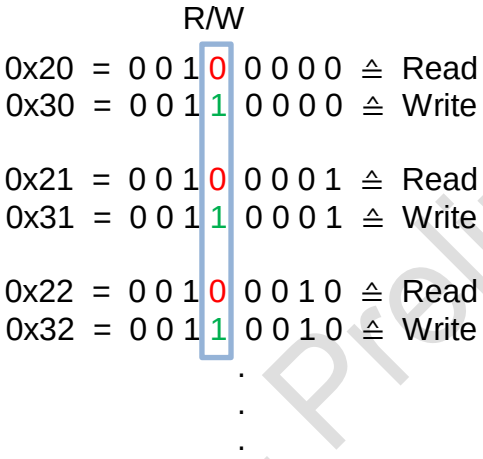
SPI Interface Detailed Description:

The serial communications shall be accomplished with the CS, SCLK, DIN, and DOUT pins. The host CPU selects the ASIC with the CS signal and shifts data into the ASIC DIN input using the SCLK for synchronizing the bit shifts. Upon receiving SCLKs from the host CPU (when selected), the ASIC shifts data out the DOUT pin. Serial data from DIN is latched into the shift register on the rising edge of SCLK. Data is shifted out to DOUT on the falling edge of SCLK.

There are 3 types of commands for the SPI: Read, Write, and “Quick Read”. All command and data bytes are 8-bits wide. Data bytes always sent and received MSB first.

Read/Write-Command Bitdefinition:



All Write commands are 3 bytes long with the order: command, data, data. For these commands data will always be sent and received in Big Endian format; i.e. most significant byte first. Incoming data will be padded with zeros to fill the 2 data bytes. The first returned byte will be an echo of the command. The second and third bytes will return 0x00. Following the third byte, subsequent clocks will return a ‘0’. Most Read commands are 3 bytes long with the order: command, data, data. When reading I and Q registers at the same time for a “quick read” 5 bytes are required in this order: command, I data, I data, Q data, Q data. For all Read commands data will always be sent and received in Big Endian format; i.e. most significant byte first. The 2 or 4 bytes of data from the host should all be 0x00. The first returned byte will be an echo of the command. The second through fifth bytes will return the data in the register(s) being read. Following the third/fifth byte, subsequent clocks will return the last data bit.

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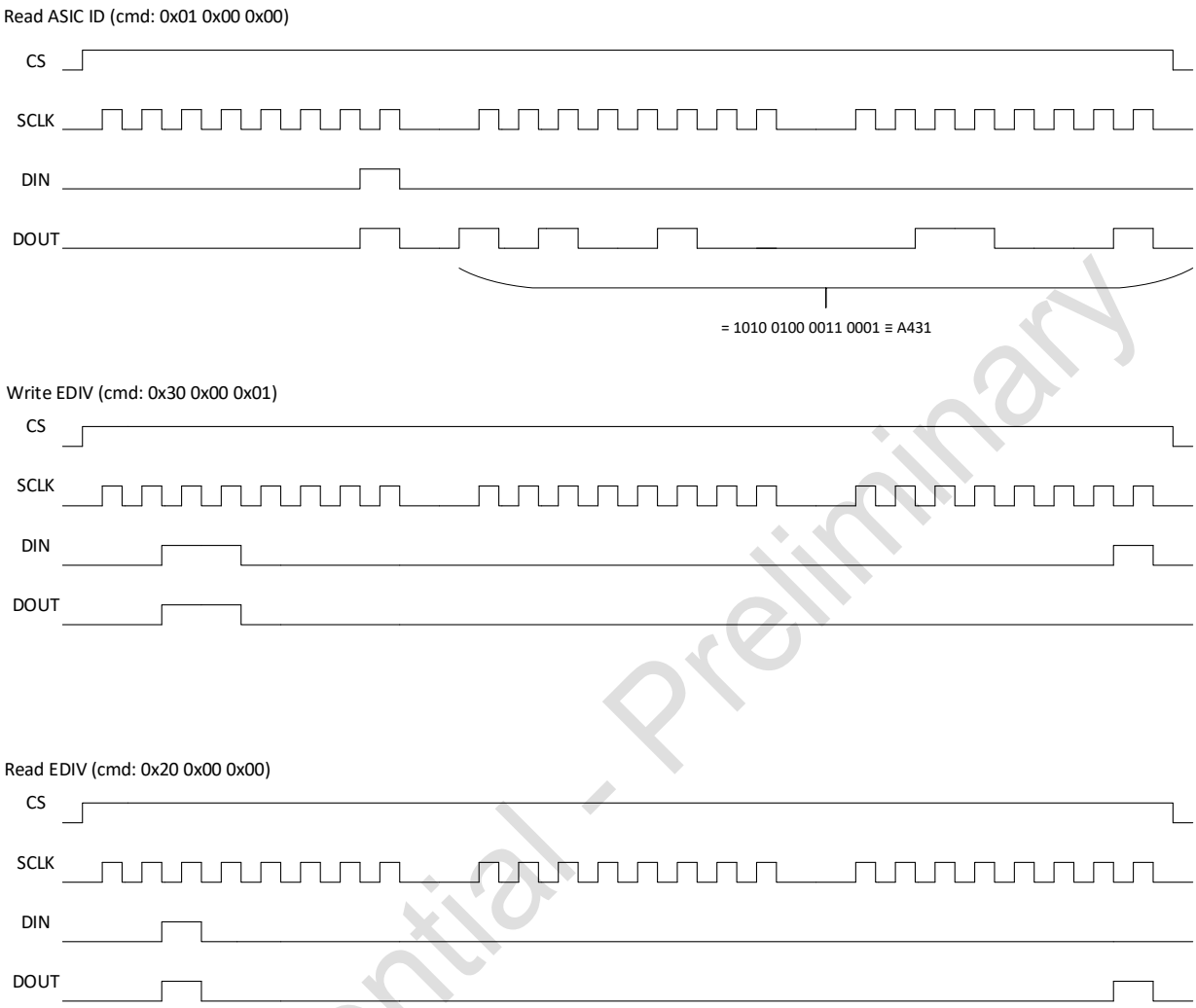
Figure 16: SPI commands



Command 0x01 followed by 2 bytes of zeros will lead to a readout from the ASIC ID.
Command 0x03 followed by the 2 Data bytes (here 00000000 00000001) will lead to write 1 in EDIV register.
Command 0x02 followed by 2 bytes of zeros will lead to a read out of the EDIV Register.

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Diagnostic

SM	Diagnostic Name	Description / Safe State
SM1	REGF	1 = Low Voltage or High Voltage Detected on 3.3V regulator. Blanking not needed.
SM2	BPFF	1 = Output is out of range in BPF. This signal requires to be synchronized and filtered to avoid spike in MCLK domain: this signal must stay at 1 for at least some MCLK_p specified by BLANK sfr, to be visible at 1 by SPI.
SM3	OCSLD	1 = Over current condition on the Shield Driver. This signal requires to be synchronized and filtered to avoid spike in MCLK domain: this signal must stay at 1 for at least some MCLK_p specified by BLANK sfr, to be visible at 1 by SPI.
SM4	OCSEN	1 = Over current condition on the Sensor Driver. This signal requires to be synchronized and filtered to avoid spike in MCLK domain: this signal must stay at 1 for at least some MCLK_p specified by BLANK sfr, to be visible at 1 by SPI.
SM6	OTPF	1 = Signature Calculation error of OTP content. The signature check is executed each time the OTP receive a reset pulse, that is at every Power on and after each EDIV update. Blanking not needed.
SM7	TX1F	1 = Sensor Driver output voltage outside operating range. This signal requires to be synchronized and filtered to avoid spike in MCLK domain: this signal must stay at 1 for at least some MCLK_p specified by BLANK sfr, to be visible at 1 by SPI.
SM8	TX2F	1 = Shield Driver output voltage outside operating range. This signal requires to be synchronized and filtered to avoid spike in MCLK domain: this signal must stay at 1 for at least some MCLK_p specified by BLANK sfr, to be visible at 1 by SPI.
SM9	PGA1F	1 = PGA1 output is saturated high or low. This signal requires to be synchronized and filtered to avoid spike in MCLK domain: this signal must stay at 1 for at least some MCLK_p specified by BLANK sfr, to be visible at 1 by SPI.

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SM10	PGA2F	1 = PGA2 output is saturated high or low. This signal requires to be synchronized and filtered to avoid spike in MCLK domain: this signal must stay at 1 for at least some MCLK_p specified by BLANK sfr, to be visible at 1 by SPI.
SM11	NECLK	1 = ECLK is missing or is invalid. In case of this error the chip cannot guarantee the correct synchronization between SPI clock and MCLK, so we will have the following behavior of the SPI which lets the user able to detect the problem. When this flag is set at 1, this means there is an error condition on the ECLK received by the chip, so by SPI access it is possible only to read the status register addressed by $02 command and the ID number $01. All the other reading operations return 0. This reading answer is forced by the SPI block.
SM12	CBF	1 = Current Buffer output is out of range high. This signal requires to be synchronized and filtered to avoid spike in MCLK domain: this signal must stay at 1 for at least some MCLK_p specified by BLANK sfr, to be visible at 1 by SPI.
SM13	PS	

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Safety Mechanism

SM1 REGF

The safety mechanism REGF is monitoring the voltage on the Regulator. If the target is above the defined higher and lower voltage limit, the sensor provides an error Flag REGF=1

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
REGF_L	Detection threshold low		3.0	3.15	3.3	V
REGF_H	Detection threshold high		3.6	3.8	4	V
FTTI_REGF	Reaction time			150		us

SM2 BPFF

The safety mechanism BPFF is monitoring the voltage of the Band-pass filter. If the target is above the defined higher and lower voltage limit, the sensor provides an error Flag BPFF=1

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BPFF_L	Detection threshold low		0.25	0.3	0.33	V
BPFF_H	Detection threshold high		CVDD-0.33	CVDD-0.3	CVDD-0.25	V
FTTI_BPFF	Reaction time				100	ns

SM3 OCSLD

The safety mechanism OSCLD is monitoring output current of the shield driver. If the target is above the defined higher limit, the sensor provides an error Flag OCSLD=1

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OCSLD	Threshold		7	8.5	10	mA
FTTI_OCSLD	Reaction time				Depending on the load	us

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SM4 OCSEN

The safety mechanism OCSEN is monitoring output current of the sensor driver. If the target is above the defined higher limit, the sensor provides an error Flag OCSEN=1

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OCSEN	Threshold		7	8.5	10	mA
FTTI_OCSEN	Reaction time				Depending on the load	us

SM6 OTPF

A signature check is performed on all the OTP content after each OTP reset pulse, this happens also at power on. In case of signature error and until the signature calculation execution a diagnostic bit OTPF = 1 is latched in the SPI Status Register. The signature bits are calculated based on the OTP content using a formula provided by the factory. The signature implemented is based on 8 bits signature analysis Multiple Input Signature Register, (MISR).

SM7 TX1F

The safety mechanism TX1F is monitoring the voltage on the sensor driver output. If the target is above or below the defined higher and lower voltage limit, the sensor provides an error Flag TX1F=1

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TXF1_H2	Threshold high (TXV=2)		1.85	1.95	2.05	V
TXF1_H1	Threshold high (TXV=1)		1.61	1.70	1.79	V
TXF1_L1	Threshold low (TXV=1)		0.75	0.80	0.85	V
TXF1_L2	Threshold low (TXV=2)		0.46	0.50	0.54	V
TXF1_MP	Margin between threshold high and TX positive peak		30			mVdc
TXF1_MN	Margin between TX negative peak and threshold low		30			mVdc
FTTI_TXF1	Reaction time				100	ns

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SM8 TX2F

The safety mechanism TX2F is monitoring the voltage on the shield driver output. If the target is above or below the defined higher and lower voltage limit, the sensor provides an error Flag TX2F=1

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TXF2_H2	Threshold high (TXV=2)		1.85	1.95	2.05	V
TXF2_H1	Threshold high (TXV=1)		1.61	1.70	1.79	V
TXF2_L1	Threshold low (TXV=1)		0.75	0.80	0.85	V
TXF2_L2	Threshold low (TXV=2)		0.46	0.50	0.54	V
TXF2_MP	Margin between threshold high and TX positive peak		30			mVdc
TXF2_MN	Margin between TX negative peak and threshold low		30			mVdc
FTTI_BPFF	Reaction time				100	ns

SM9 PGA1F

The safety mechanism PGA1 is monitoring the voltage of the PGA output. If the target is above the defined higher and lower voltage limit, the sensor provides an error Flag PGA=1

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PGA1F_L	Detection threshold low		0.2	0.25	0.28	V
PGA1F_H	Detection threshold high		CVDD-0.28	CVDD-0.25	CVDD-0.2	V
FTTI_PGA1F	Reaction time				100	ns

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SM10 PGA2F

The safety mechanism PGA2F is monitoring the voltage of the PGA output. If the target is above the defined higher and lower voltage limit, the sensor provides an error Flag PGA2F=1

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PGA2F_L	Detection threshold low		0.2	0.25	0.28	V
PGA2F_H	Detection threshold high		CVDD-0.28	CVDD-0.25	CVDD-0.2	V
FTTI_PGA2F	Reaction time				100	ns

SM11 NECLK

The missing ECLK diagnostic monitors the 4MHz system clock MCLK to ensure that it is running and therefore ECLK is coming from the microprocessor. If ECLK is not running, the NECLK bit is set in the SPI Status register.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ECLKD_F	Frequency for flag		0.35	1	2	MHz
FTTI_ECLKD	Reaction time				100	ns

SM12 CBF

The safety mechanism CBF is monitoring the voltage of the buffer of the current sensor. If the target is above the defined higher and lower voltage limit, the sensor provides an error Flag CBF=1

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CBF_L	Detection threshold low		0.25	0.3	0.33	V
CBF_H	Detection threshold high		CVDD-0.33	CVDD-0.3	CVDD-0.25	V
FTTI_CBF	Reaction time				100	ns

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SM13 PPSF

The Pin-to-Pin Short diagnostic (pins 13-23) is realized with a pin-to-pin DC resistance measurement. For the pair of pins being tested, the main MUX is set to MODE=0 (open). Two diagnostic Muxes can route any of the 11 tested pins (SHIELD and SEN[9:0] to a comparator (programmed by PLUS[3:0] and MINUS[3:0], referenced by a resistive divider.In case the resitance is to high, the PPSF Flag is going high.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PPSF_R	Threshold resistance		10	20	30	kΩ
PPSF_VOS	Comparator offset				15	mV
PPSF_Rext	External resistance Pin to VSS		200			kΩ
FTTI_BPFF	Reaction time				Depending on the load	ns

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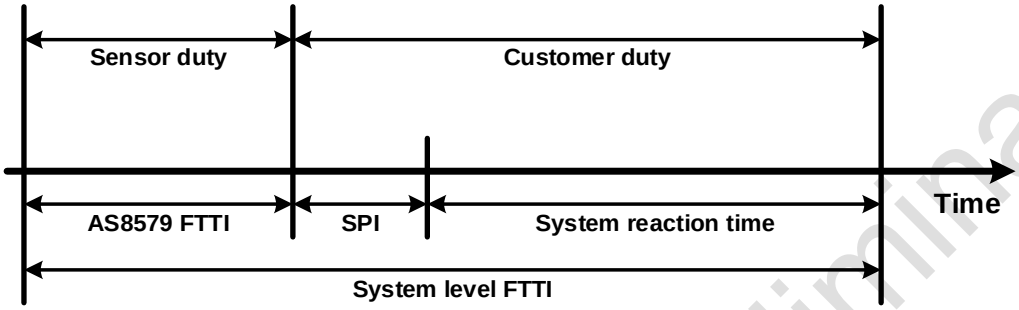
Fault Tolerant Time Interval (FTTI)

The FTTI is the time between a failure that could rise a hazardous event and the time which is needed for counter reactions to prevent the hazardous event. The build-up of the FTTI is shown below in Figure.



Safety Mechanism	FTTI AS8579 Safety Mechanism	Interface time based o 8Mhz	comment
SM1 - REGF	150us ± 5%	+ 6us	System reaction time is missing and shall be added by the customer
SM2 – BPFF	100ns	+ 6us	
SM3 – OSCLD	Depending on the load	+ 6us	
SM4 – OSCEN	Depending on the load	+ 6us	
SM6 – OTPF	100ns	+ 6us	
SM7 – TX1F	100ns	+ 6us	
SM8 – TX2F	100ns	+ 6us	
SM9 – PGA1F	100ns	+ 6us	
SM10 – PGA2F	100ns	+ 6us	
SM11 – NECLK	100ns	+ 6us	
SM12 – CBF	100ns	+ 6us	
SM13 – PPSF	Depending on the load	+ 6us	

Preliminary

Register description

Volatile register description

Figure 15: Memory Register Description

c	Name	Default	Description
0x01	Sensor ID	0xA431	ID of the Sensor
0x02	Status Reg	0x0000	Error Register
0x03	I_DATA	0x0000	I Data Information
0x04	Q_DATA	0x0000	Q Data Information
0x05	ADC_Status	0x0000	Bit is set when the ADC has completed
0x20/0x30	EDIV	0x0000	ECLK Divider selection
0x21/0x31	FREQ	0x0000	Frequency Selection
0x22/0x32	TXV	0x0000	Transmitter Voltage Selection
0x23/0x33	SEN/MODE	0x0000	MUX control for the connected SENx Pins
0x27/0x37	PGA	0x0000	Command sets the PGA voltage Gain. Adjusts the input voltage to the ADC to optimize its conversion resolution
0x28/0x38	OFFSET_I PGA	0x0000	Command is used to program the offset DAC to compensate parasitic offsets.
0x29/0x39	OFFSET_Q PGA	0x0000	Command is used to program the offset DAC to compensate parasitic offsets.
0x2A/0x3A	ADCTL	0x0000	Controls the ADC converter cycles
0x2B/0x3B	BLANK	0x003F	This Register is used to program the 6-Bit register up/down counter used for blanking faults.
0x2C/0x3C	PLUS/MINUS	0x00FF	Control the pin-to-pin short diagnostic MUX.

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Sensor ID

The 0x01 command is used to read the ID Register. Reading this register will always return 0xA431. This is used by the microprocessor to validate the SPI communication to the ASIC. ID must be in SPI domain, the command 0x01 will return 0, until the MCLK logic domain will be under POR reset.

Figure 16: Sensor ID (0x01)

ASIC ID [15:0] binary	Read/Write	Default value
1010 0100 0011 0001	R	0xA431

Status Register

The 0x02 command is used to read the Status Register. The data is returned in the second and third bytes of transfer as follows:

Figure 17: Status Register (0x02)

Name	Bit Position	Read/Write	Description
EDIV	15:13	R	Less significant part of the Value programmed into EDIV sfr.
OTPF	12	R	OTP Fault: 1 = Signature Calculation error of OTP content. The signature check is executed each time the OTP receive a reset pulse, that is at every Power on and after each EDIV update. Blanking not needed.
PPSF	11	R	Pin-to-Pin short fault: 1 = Pins under test are shorted together. Blanking not needed.
BPFF	10	R	BPFF Fault: 1 = Output is out of range in BPF. This signal requires to be synchronized and filtered to avoid spike in MCLK domain: this signal must stay at 1 for at least some MCLK_p specified by BLANK sfr, to be visible at 1 by SPI.
REGF	9	R	Regulator Voltage Detected Fault: 1 = Low Voltage or High Voltage Detected on 3.3V regulator. Blanking not needed.
OCSLD	8	R	Over Current on Shield Driver: 1 = Over current condition on the Shield Driver. This signal requires to be synchronized and filtered to avoid spike in MCLK domain: this signal must stay at 1 for at least some MCLK_p specified by BLANK sfr, to be visible at 1 by SPI.
OCSEN	7	R	Over Current for Sensor Driver: 1 = Over current condition on the Shield Driver. This signal requires to be synchronized and filtered to avoid spike in MCLK domain: this signal must stay at 1 for at least some MCLK_p specified by BLANK sfr, to be visible at 1 by SPI.

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TESTON	6	R	Test Mode ON: 1 = Test Mode is enabled: the chip is in the analog test mode or in digital test mode. Blanking not needed.
TX1F	5	R	Sensor Driver Fault: 1 = Sensor Driver output voltage outside operating range. This signal requires to be synchronized and filtered to avoid spike in MCLK domain: this signal must stay at 1 for at least some MCLK_p specified by BLANK sfr, to be visible at 1 by SPI.
TX2F	4	R	Shield Driver Fault: 1 = Shield Driver output voltage outside operating range. This signal requires to be synchronized and filtered to avoid spike in MCLK domain: this signal must stay at 1 for at least some MCLK_p specified by BLANK sfr, to be visible at 1 by SPI.
PGA1F	3	R	PGA1 Output Fault: 1 = PGA1 output is saturated high or low. This signal requires to be synchronized and filtered to avoid spike in MCLK domain: this signal must stay at 1 for at least some MCLK_p specified by BLANK sfr, to be visible at 1 by SPI.
PGA2F	2	R	PGA2 Outputfault: 1 = PGA2 output is saturated high or low. This signal requires to be synchronized and filtered to avoid spike in MCLK domain: this signal must stay at 1 for at least some MCLK_p specified by BLANK sfr, to be visible at 1 by SPI.
NECLK	1	R	No ECLK: 1 = ECLK is missing or is invalid. In case of this error the chip cannot guarantee the correct synchronization between SPI clock and MCLK, so we will have the following behavior of the SPI which lets the user able to detect the problem. When this flag is set at 1, this means there is an error condition on the ECLK received by the chip, so by SPI access it is possible only to read the status register addressed by 0x02 command and the ID number 0x01. All the other reading operations return 0. This reading answer is forced by the SPI block.
CBF	0	R	Current Buffer Fault: 1 = Current Buffer output is out of range high. This signal requires to be synchronized and filtered to avoid spike in MCLK domain: this signal must stay at 1 for at least some MCLK_p specified by BLANK sfr, to be visible at 1 by SPI.

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I-Channel Data

According to the register settings the Accumulated Data for the I-Channel.

Figure 18: Data Register I Channel (0x03)

Name	Bit string (13:0)	Read/Write	Description
ACCU I	XX00 0000 0000 0000	R	Data Register

Q-Channel Data

According to the register settings the Accumulated Data for the Q-Channel.

Figure 19: Data Register Q Channel (0x04)

Name	Bit string (13:0)	Read/Write	Measurement Data
ACCU Q	XX00 0000 0000 0000	R	Data Register

Quick read I and Q Data Register (0x03 and 0x04):

The 0x90 command allows for I and Q data to be read from the same sensor signal sample by doing a quick read on both I and Q data registers. This command links the I and Q registers together into a 32-bit word. This data is read back using a 40-bit word in this order: command byte, I data word, Q data word. I/Q data matching is guaranteed using the Quick Read command (i.e. – I and Q data will be from a matched sample). The I and Q data registers are reset to 0x00 after reading.

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ADC Status Register

The 0x05 command is used to read the “ADC Complete” status bit (LSB of the 16-bit returned data). This bit is set when the ADC has completed the accumulation of the programmed samples of both the I and Q data signals and placed the data in the SPI output registers. The bit is cleared upon reading the combined data registers (0x90 command) or when a new ADC cycle is initiated (0x3A0001 or 0x3A0002). The “ADC complete” bit can also be reset by the 0x3A0000 command

Figure 20: ADC Status (0x05)

Name	Bit Position	Read/Write	Measurement Data
ADC complete	0	R	Bit is set (1) when ADC has completed accumulation.

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ECLK Divider Selection

The 0x30 command controls the division factor (EDIV [3:0]) applied to ECLK to generate the internal system clock. The division factor is programmable from 1 to 12. Default value at power-up is 12. The 0x20 command is used to read the current value of EDIV.

Figure 21: ECLK Selection (0x20/0x30)

EDIV [3:0] binary	Read/Write	ECLK frequency Dividing factor
0000	R/W	12
0001	R/W	11
0010	R/W	10
0011	R/W	9
0100	R/W	8
0101	R/W	7
0110	R/W	6
0111	R/W	5
1000	R/W	4
1001	R/W	3
1010	R/W	2
1011	R/W	1
1100	R/W	1
1101	R/W	1
1110	R/W	1
1111	R/W	1

The clock obtained by the frequency division of the ECLK is called MCLK and is used to clock all the digital part except the SPI interface. SPI communication is guaranteed if $F_{SCLK} \leq 2*F_{MCLK}$, where $F_{MCLK} = F_{ECLK}$ /EDIV. When $F_{SCLK} > 2*F_{MCLK}$, only limited set of SPI functions are guaranteed: Writing EDIV and reading Status Register. The first command sent to the chip is $30 to set the proper F_{MCLK} =4MHz. Each time there is an EDIV change, an automatic OTP reset is generated to clean up the memory from possible timing error if the previous selected MCLK was higher than 4MHz. The reload of the OTP memory takes less than 8190 MCLK clock cycles, during the reload phase it is possible to have SPI communication, but not possible to start sensing.

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Frequency Selection

The 0x31 command is used to select the Programmable Sine Wave Generator frequency. This is a 2-bit number (FREQ) that is decoded as follows. At power-up, FREQ defaults to 0x0. The $21 command is used to read the current value of FREQ.

Figure 22: Frequency Selection (0x21/0x31)

FREQ [1:0] binary	Read/Write	Frequency [kHz]
00	R/W	45.45
01	R/W	71.4
10	R/W	100
11	R/W	125

Transmitter Voltage Selection

The 0x32 command sets the transmitter output AC voltage (TXV). At power-up, TXV defaults to 0x0. The 0x22 command is used to read the current value of TXV. The TXV can update the SFR value (0x22/0x32) only at the zero – crossing of P[4:0], i.e. when zc_en at 1 is detected. TXF1 and TXF2 fault bits are not valid when TXV=0. This is a 2-bit number (TXV) that is decoded as follows:

Figure 23: Transmitter Voltage Selection (0x22/0x32)

TXV [1:0] binary	Read/Write	Output Voltage peak-peak [V]
00	R/W	0
01	R/W	0.5
10	R/W	1.0
11	R/W	0

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MUX Control

The 0x33 command controls the ten 3-channel MUXES connected to the SENx pins. It also controls the 2-channel MUX connected to the SHIELD pin. The reset condition is all SENx pins and SHIELD disconnected. The command is made out of two control values: SEN [3:0] and MODE [1:0]. These bits are decoded as shown below. The 0x23 command reads the current data in the channel select control register.

Figure 24: SENx Selection setting

SENx	MUX Selected
0000	SEN0
0001	SEN1
0010	SEN2
0011	SEN3
0100	SEN4
0101	SEN5
0110	SEN6
0111	SEN7
1000	SEN8
1001	SEN9
1010	None
1011	SHIELD
1100	None

Figure 25: Mode selection settings

MODE	SENx Connected to
00	Open
01	Sensor Driver
10	Common Mode through 5kΩ resistor
11	Leave current state

Figure 26: Mode selection (0x23/0x33)

Name	Bit number	Read/Write	Measurement Data
Mode	0:1	R/W	Mode Selection
SEN	2:5	R/W	Channel selection

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PGA Voltage Gain Control

The 0x37 command sets the in PGA voltage gain. This 3-bit number (PGA [2:0]) adjusts the input voltage level to the ADC to optimize its conversion resolution. The 0x27 command reads the PGA value. At power-up, PGA defaults to 0x00.

Figure 27: Gain Control (0x27/0x37)

PGA [2:0] binary	Read/Write	PGA Gain
000	R/W	36
001	R/W	24
010	R/W	16
011	R/W	10.67
100	R/W	7.11
101	R/W	4.74
110	R/W	3.16
111	R/W	2.11

PGA Offset Control (0x28&29/0x38&39)

The 0x38 and 0x39 command are used to program the offset DACs that for the I/Q PGAs. 0x38 programs the I PGA offset DAC (OFFSET1) and 0x39 programs the Q PGA offset DAC (OFFSET2). This offset compensates for the parasitic offsets in the sensor system and allows to shift DC operating point in order to maximize the ADC range. The 0x28 and 0x29 command read the current values of OFFSET1 and OFFSET21. DAC outputs can be set to 256 settings between VSS and VDD.

The Offset DAC is used to change the DC operating point of the ADC input. Increasing the Offset DAC value one count will decrease the ADC input by 80 counts before the accumulation.

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ADC Control

The 0x3A command controls the ADC converter cycles. The ADCTL [7:0] sfr is decoded as shown below. The following tables are calculated by taking in account a MCLK frequency of 4MHz.

ADCTL [7:6]: Selects how many MCLK clock cycles are used to define the settling phase for the AFE.

Figure 28: Settling Time selection

ADCTL [7:6] binary	System settling time in periods	Time [µs]
00	1600 MCLK_p	400
01	2304 MCLK_p	576
10	2656 MCLK_p	664
11	1600 MCLK_p	400

ADCTL [5:4]: Selects how many samples are accumulated for each I and Q channel.

Figure 29: Accumulation I&Q-Channel

ADCTL [5:4] binary	Number of samples calculated for I and Q Channel
00	4
01	8
10	16
11	4

ADCTL [3:2]: Select the ADC clock frequency.

Figure 30: ADC Clock selection

ADCTL [3:2] binary	System settling time in periods	ADCLK frequency [kHz]
00	16 * MCLK_p	250
01	8 * MCLK_p	500
10	4 * MCLK_p	1000
11	16 * MCLK_p	250

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Figure 30: ADC State

ADCTL [1:0] binary	ADC State
00	RESET of DSP and ADC stop
01	Start single conversion
10	Start continuous conversions
11	Stop current conversions

Figure 31: ADCTL (0x2A/3A)

Name	Bit number	Read/Write	Description
TS	6:7	R/W	Time Selection
ACCU	4:5	R/W	Accumulation setting
CS	2:3	R/W	Clock Selection
ADC State	0:1	R/W	ADC State selection

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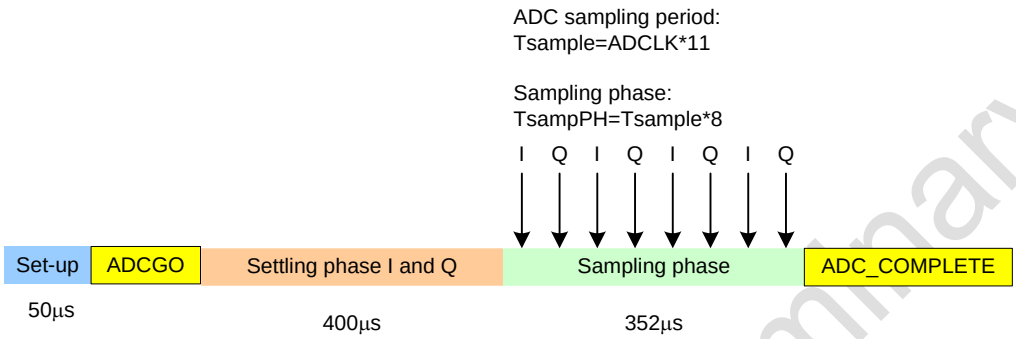
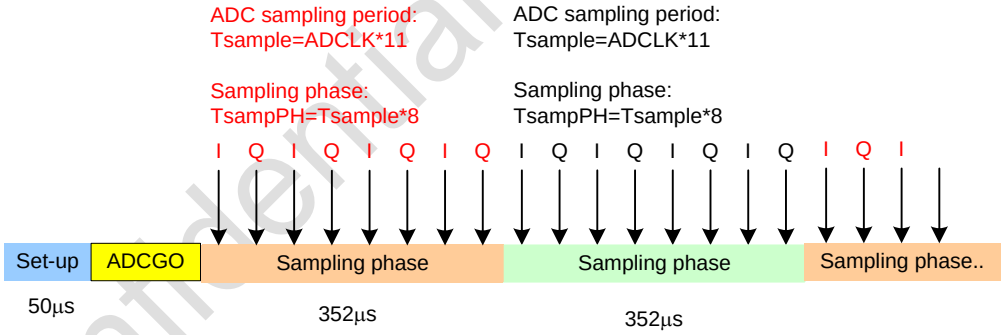
“Single Conversion” causes the ADC to wait for the “system settling time" before starting sampling and then to accumulate the number of samples, specified in the register ADCTL [5:4]. I and Q samples arrive interleaved. The DSP control logic will provide the analog part the signal IQMUX to switch the ADC analog input between I channel and Q channel.
Once completed, I and Q results are moved to the SPI output registers and the “ADC_COMPLETE” bit in register 0x05 is set. Before another “Single Conversion” can be started, the ADC must be reset by either performing a Quick Read (0x90), or by issuing the “ADC Reset” command.

Figure 32: Measurement Cycle



“Continuous Conversion” mode causes the ADC to take successive samples accumulations of I and Q, again the number of samples taken is specified by ADCTL [5:4] SFR.
The ADC is time multiplexed between the I and Q channels (I and Q samples are interleaved). Each data point stored to the SPI output register is the accumulation of a programmed number of 10-bit ADC values, for each I and Q. Data is stored to the SPI as a complete I & Q set (data synchronicity is guaranteed by the Control Logic).

Figure 33: Measurement Cycle



Before changing a parameter of the ADCTL [7:0] the ADC and accumulators have to be reset, this operation is done by writing ADCTL [1:0] = 0, this put under reset the DSP : ACCUM_I and ACCUM_Q = 0. This condition is called “ADC reset condition”. In a next SPI access the command start of conversion are sent. The ADCTL [1:0] = 0 forces the DSP into the above described “ADC reset condition” the operation are immediately interrupted.

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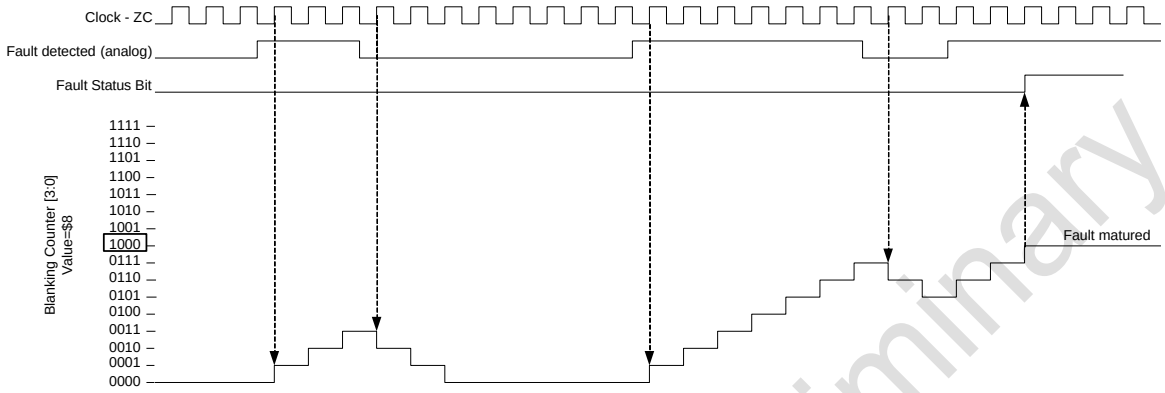
BLANK

The 0x3B command is used to program the 6-bit register up/down counter used for blanking faults. A fault is not reported in the Status Register until the Up/Down Counter has reached the programmed terminal value (BLANK).

Figure 34 Example Fault Maturity Using Blanking



Each fault has its own Up/Down Counter (individually blanked). See Section 7.6.4.3 for details on which faults having blanking. The $2B command is used to read the current value of the BLANK register. The counters are clocked from a signal synchronous with the zero crossing (ZC) of the transmitter sine wave (e.g. related to P[2] signal). Effectively each fault is looked for at the counter input ONCE per sine cycle. SPI fault bits do not clear with the analog fault disappearing. They are latched in the SPI register until the Status Register is read through the SPI. The fault pulses from analog comparators are latched and the latches are reset when they are read. The comparator pulses over ride the latch reset. Only when the status register with the fault bit set at one, has been read, the status bit is reset and the blanking counter can start again from 0, to count up/down.

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Pin-to-Pin Short Diagnostic MUX Control

The 0x3C command is used to control the pin-to-pin short diagnostic MUX. This register is made up of two 4-bit registers PLUS[3:0] and MINUS[3:0]. PLUS controls the pin connected to the positive side of the comparator, MINUS to the negative side. The default value at POR is 0x00FF (all pin-to-pin short MUXes are OFF). The data is decoded as follows:

Figure 35: Transmitter Voltage Selection (0x22/0x32)

PLUS/MINUS [3:0] binary	Read/Write	Pin Connected to Comparator
0000	R/W	SEN0
0001	R/W	SEN1
0010	R/W	SEN2
0011	R/W	SEN3
0100	R/W	SEN4
0101	R/W	SEN5
0110	R/W	SEN6
0111	R/W	SEN7
1000	R/W	SEN8
1001	R/W	SEN9
1010	R/W	NONE
1011	R/W	SHIELD
1100	R/W	NONE
1101	R/W	NONE
1110	R/W	NONE
1111	R/W	NONE

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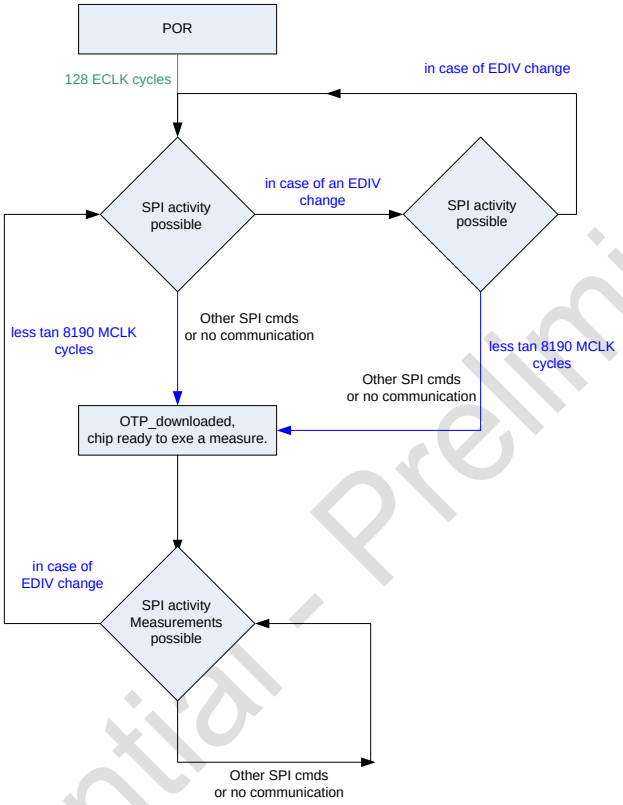
Flow chart of functional behavior

After POR, in general at every OTP reset pulse, the OTP fused data are transferred into the SFR memory. This operation takes less than 8190 MCLK cycles, after that operation the DSP is enabled and the chip can perform measurements. The chip is able to process SPI commands after 128 MCLK cycles from the POR, that is the OTP download and the SPI access can work in parallel.

Figure 36: Flow chart



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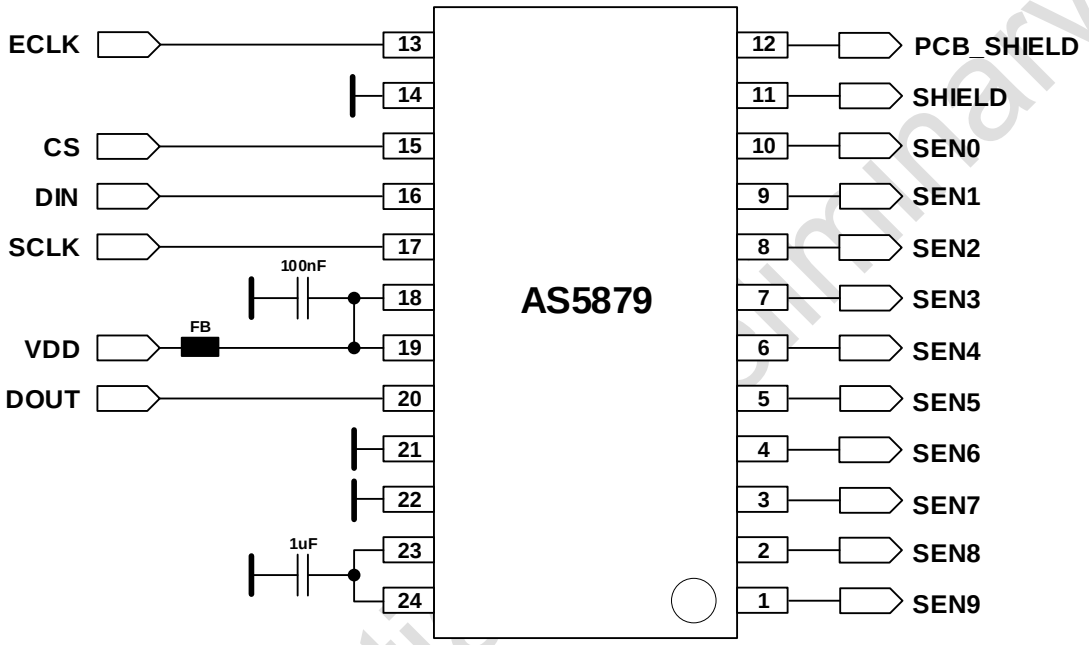
Application Information

Recommended Application Diagrams and Built-In Capacitors

Figure 37: Application schematic for AS8579



Confidential Summary

System Timing vs. ADCTL setting

ADCTL			Selected Settings			System Timing		
Settling [7:6]	Samples [5:4]	Freq [3:2]	Settling Time (µs)	Number of I/Q Samples	ADC I/Q Sample Rate (kHz)	Settling Time (µs)	ADC Sampling Time (µs)	Total Time (µs)
00	00	00	400	4	11,36	400	352	752
00	00	01	400	4	22,73	400	176	576
00	00	10	400	4	45,45	400	88	488
00	01	00	400	8	11,36	400	704	1104
00	01	01	400	8	22,73	400	352	752
00	01	10	400	8	45,45	400	176	576
00	10	00	400	16	11,36	400	1408	1808
00	10	01	400	16	22,73	400	704	1104
00	10	10	400	16	45,45	400	352	752
01	00	00	576	4	11,36	576	352	928
01	00	01	576	4	22,73	576	176	752
01	00	10	576	4	45,45	576	88	664
01	01	00	576	8	11,36	576	704	1280
01	01	01	576	8	22,73	576	352	928
01	01	10	576	8	45,45	576	176	752
01	10	00	576	16	11,36	576	1408	1984
01	10	01	576	16	22,73	576	704	1280
01	10	10	576	16	45,45	576	352	928
10	00	00	664	4	11,36	664	352	1016
10	00	01	664	4	22,73	664	176	840
10	00	10	664	4	45,45	664	88	752
10	01	00	664	8	11,36	664	704	1368
10	01	01	664	8	22,73	664	352	1016
10	01	10	664	8	45,45	664	176	840
10	10	00	664	16	11,36	664	1408	2072
10	10	01	664	16	22,73	664	704	1368
10	10	10	664	16	45,45	664	352	1016

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Package Drawings and Markings

Figure 38: AS8579 Packaging Outline Drawing

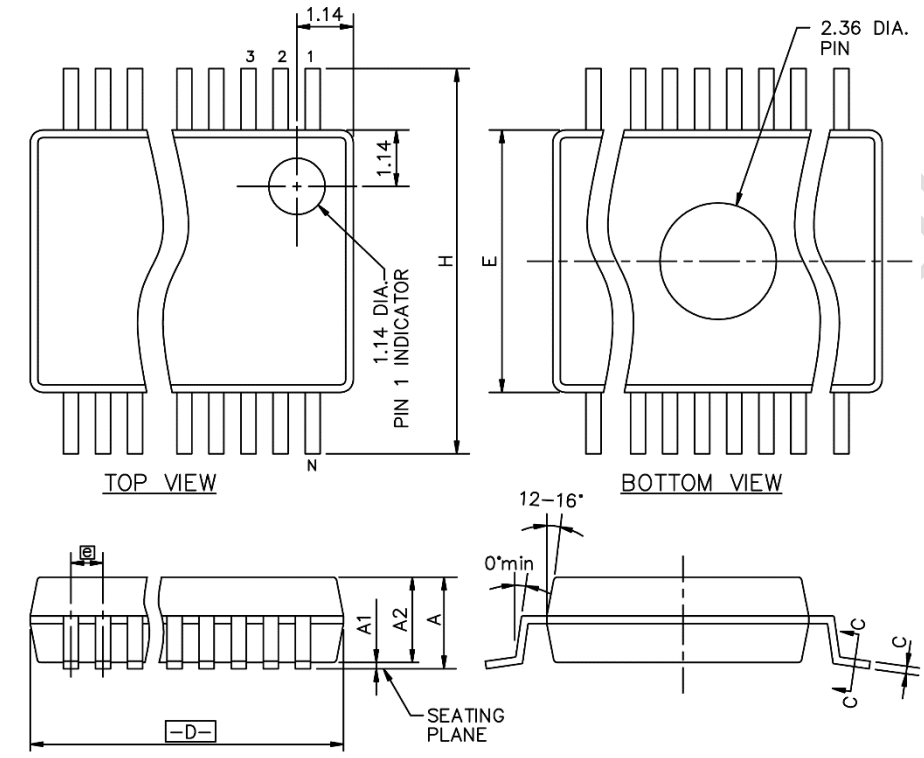

TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE	NOTE VARIATIONS	1 D MIN.	NOM.	MAX.	2 N
A	1.73	1.86	1.99			2.87	3.00	3.13	8
A_1	0.05	0.13	0.21		AA	6.07	6.20	6.33	14
A_2	1.68	1.73	1.78		AB	6.07	6.20	6.33	16
B	0.25	–	0.38		AC	7.07	7.20	7.33	20
B1	0.25	0.30	0.33		AD	8.07	8.20	8.33	24
C	0.09	–	0.20		AE	10.07	10.20	10.33	28
C1	0.09	0.15	0.16		AF	10.07	10.20	10.33	30
D	SEE VARIATIONS			1					
E	5.20	5.30	5.38						
e	0.65 BSC								
H	7.65	7.80	7.90						
L	0.63	0.75	0.95						
L1	1.25 REF.								
N	SEE VARIATIONS			2					
α	0°	4°	8°						
R	0.09	0.15	–						

NOTE:
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.20mm on D PER SIDE.

RoHS
Green

Figure 39: Packaging Code

YY	WW	I	ZZ
Last two digits of the current year	Manufacturing week	Plant identifier	Free choice/traceability code

Figure 40: Packaging Code

XXX / XXXX
Encoded datecode year

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RoHS Compliant and ams Green Statement

RoHS: The term RoHS compliant means that ams products fully comply with current RoHS directives. Our semiconductor products do not contain any chemicals for all 6 substance categories, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, RoHS compliant products are suitable for use in specified lead-free processes.

ams Green (RoHS compliant and no Sb/Br): ams Green defines that in addition to RoHS compliance, our products are free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

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Ordering & Contact Information

Figure 41: Ordering Information

Ordering Code	Package	Marking	Delivery Form	Delivery Quantity

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