GANE350-650FBA

650 V, 350 mOhm Gallium Nitride (GaN) FET in a DFN 5 mm x 6 mm package

13 March 2025 | Product data sheet

1. General description

The GANE350-650FBA is a general purpose 650 V, 350 mΩ Gallium Nitride (GaN) FET in a DFN 5 mm x 6 mm surface mount package. It is a normally-off e-mode device offering superior performance.

2. Features and benefits

- Enhancement mode - normally-off power switch
- Ultra high frequency switching capability
- No body diode
- Low gate charge, low output charge
- Qualified for standard applications
- ESD protection
- RoHS, Pb-free, REACH-compliant
- High efficiency and high power density

3. Applications

- High power density and high efficiency power conversion
- AC-to-DC converters, totem pole PFC
- DC-to-DC converters
- Fast battery charging, mobile phone, laptop, tablet and USB type-C chargers
- Datacom and telecom (AC-to-DC and DC-to-DC) converters
- Motor drives
- Solar (PV) inverters
- Class D audio amplifiers, TV PSU and LED drivers

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	-55 °C ≤ T_j ≤ 150 °C		-	-	650	V
V_{TDS}	transient drain to source voltage	t_p < 200 µs	[1]	-	-	800	V
I_D	drain current	V_{GS} = 6 V; T_{mb} = 25 °C; Fig. 2	[2]	-	-	6	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	65	W
T_j	junction temperature			-55	-	150	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 6 V; I_D = 2.2 A; T_j = 25 °C; Fig. 12; Fig. 13; Fig. 14		-	270	350	mΩ
		V_{GS} = 6 V; I_D = 2.2 A; T_j = 150 °C; Fig. 12; Fig. 15		-	580	-	mΩ

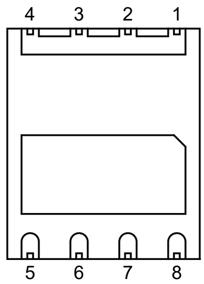
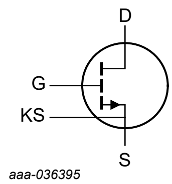
nexperia

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_G	gate resistance	f = 5 MHz; T_j = 25 °C; open drain		-	9	-	Ω
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 2.2 A; V_{DS} = 400 V; V_{GS} = 6 V; T_j = 25 °C; Fig. 16; Fig. 17		-	0.5	-	nC
$Q_{G(tot)}$	total gate charge			-	1.5	-	nC
Q_{oss}	output charge	V_{GS} = 0 V; V_{DS} = 400 V; T_j = 25 °C; Fig. 22	[3]	-	13	-	nC

[1] Intended for non-repetitive events
[2] Limited by device saturation
[3] Q_r is not specified separately from Q_{oss} for e-mode GaN FETs, since $Q_r = Q_{oss} + Q_D$, and Q_D = 0. (Q_D is charge associated with diffusion of minority carriers. Since there is no body diode, no minority carriers in excess of Q_{oss} have to be transferred for e-mode GaN FETs.)

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
7	KS	kelvin source	 Transparent top view **DFN5060-5 (SOT8075-1)**	
8	G	gate		
1-4	D	drain		
5,6	S	source		
mb	S	source		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
GANE350-650FBA	DFN5060-5	plastic thermal enhanced small outline package; no leads; 5 terminals; body: 5 × 6 × 0.9 mm	SOT8075-1

7. Marking

Table 4. Marking codes

Type number	Marking code
GANE350-650FBA	350IFBA

8. Limiting values

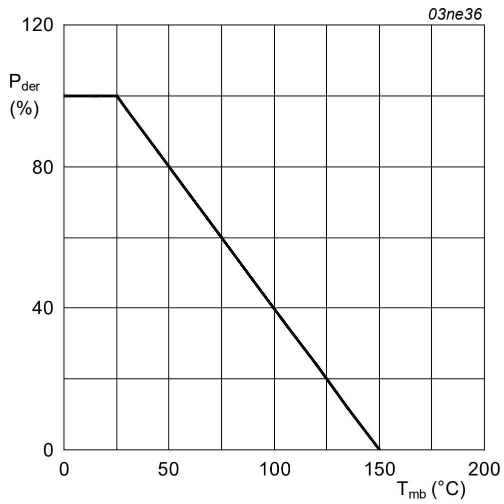
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	-55 °C ≤ T_j ≤ 150 °C		-	650	V

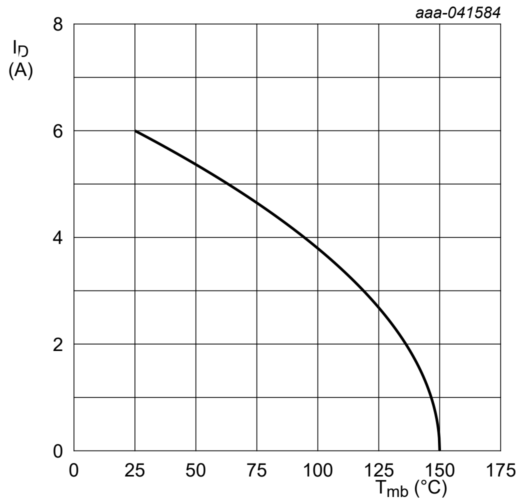
Symbol	Parameter	Conditions		Min	Max	Unit
V_{TDS}	transient drain to source voltage	t_p < 200 µs	[1]	-	800	V
V_{GS}	gate-source voltage		[2]	-1.4	7	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	65	W
I_D	drain current	V_{GS} = 6 V; T_{mb} = 25 °C; Fig. 2	[3]	-	6	A
I_{DM}	peak drain current	pulsed; t_p = 10 µs; T_{mb} = 25 °C; Fig. 3	[4]	-	10	A
		pulsed; t_p = 10 µs; T_{mb} = 125 °C; Fig. 4	[4]	-	6	A
T_{stg}	storage temperature			-55	150	°C
T_j	junction temperature			-55	150	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C

[1] Intended for non-repetitive events
[2] The minimum V_{GS} is clamped by ESD protection circuit
[3] Limited by device saturation
[4] Limit was extracted from characterization test, not measured during production



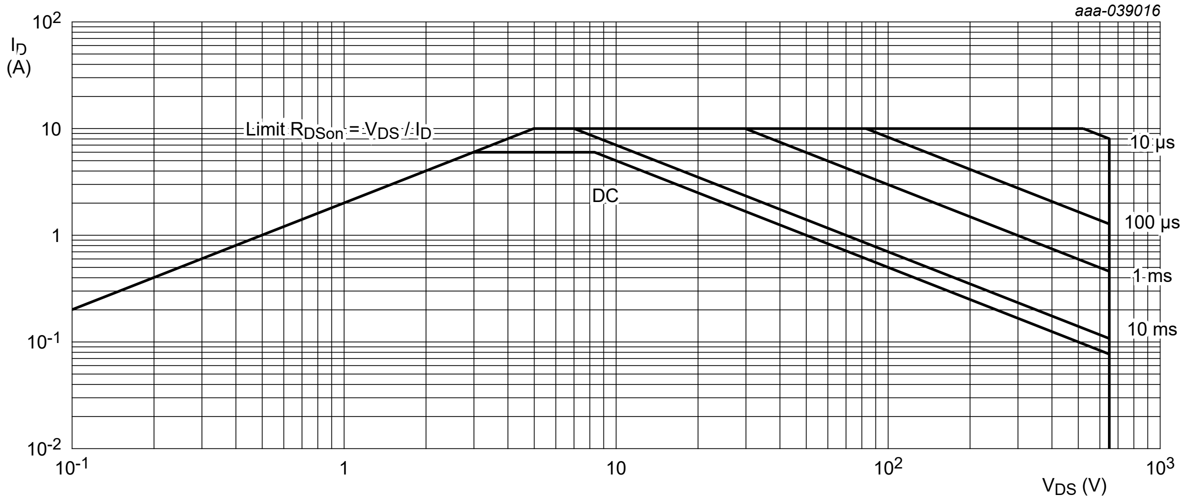
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



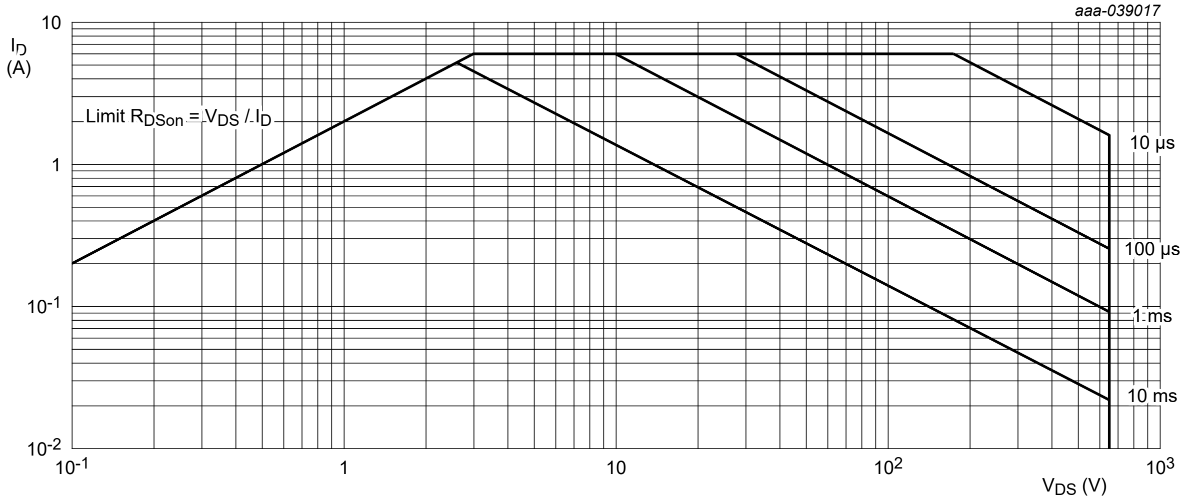
V_{GS} ≥ 6 V

Fig. 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



T_{mb} = 125 °C; I_{DM} is a single pulse

Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	-	1.9	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	-	37.1	K/W

[1] $R_{th(j-a)}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

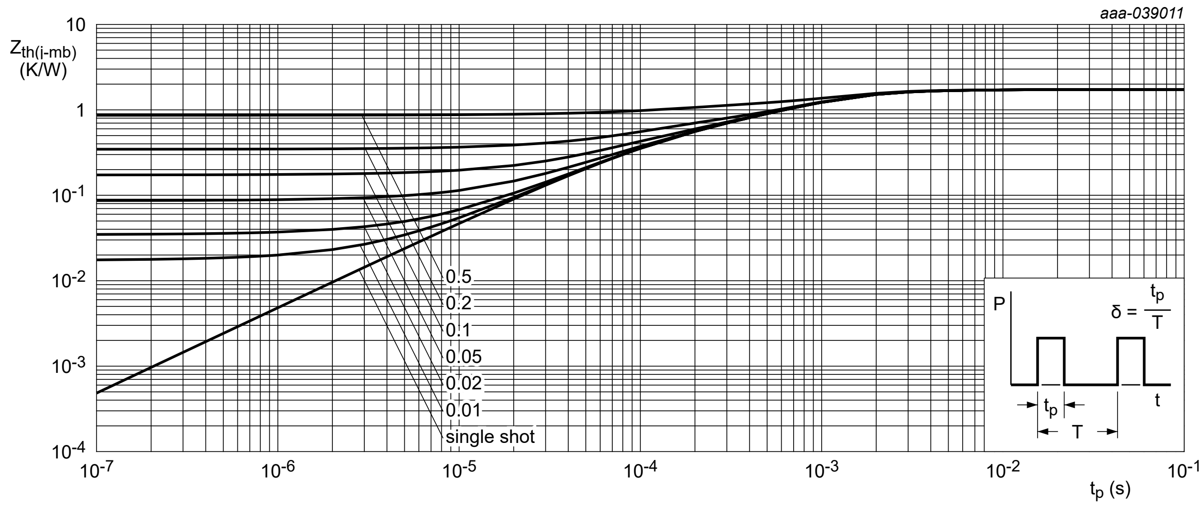


Fig. 5. Transient thermal impedance from junction to case as a function of pulse duration

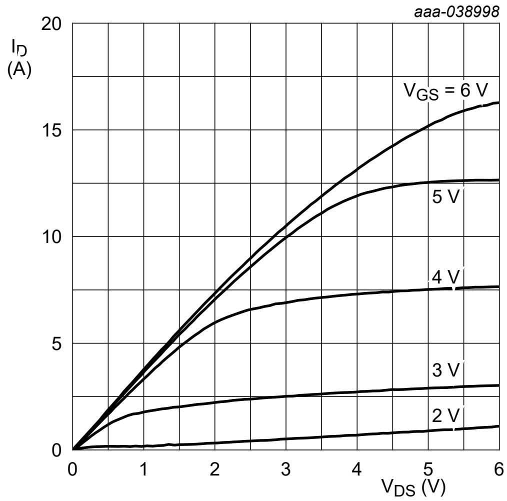
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{GS(th)}$	gate-source threshold voltage	I_D = 6.6 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 9		1.2	1.7	2.5	V
		I_D = 6.6 mA; V_{DS}=V_{GS}; T_j = 125 °C; Fig. 9		-	1.7	-	V
I_{DSS}	drain leakage current	V_{DS} = 650 V; V_{GS} = 0 V; T_j = 25 °C; Fig. 10		-	0.6	12	µA
		V_{DS} = 650 V; V_{GS} = 0 V; T_j = 150 °C; Fig. 10		-	5	-	µA
I_{GSS}	gate leakage current	V_{GS} = 6 V; V_{DS} = 0 V; T_j = 25 °C; Fig. 11		-	30	-	µA
R_{DSon}	drain-source on-state resistance	V_{GS} = 6 V; I_D = 2.2 A; T_j = 25 °C; Fig. 12; Fig. 13; Fig. 14		-	270	350	mΩ
		V_{GS} = 6 V; I_D = 2.2 A; T_j = 150 °C; Fig. 12; Fig. 15		-	580	-	mΩ
R_G	gate resistance	f = 5 MHz; T_j = 25 °C; open drain		-	9	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 2.2 A; V_{DS} = 400 V; V_{GS} = 6 V; T_j = 25 °C; Fig. 16; Fig. 17		-	1.5	-	nC
Q_{GS}	gate-source charge			-	0.15	-	nC
Q_{GD}	gate-drain charge			-	0.5	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 2.2 A; V_{DS} = 400 V; T_j = 25 °C; Fig. 17		-	2.2	-	V
C_{iss}	input capacitance	V_{DS} = 400 V; V_{GS} = 0 V; f = 100 kHz; T_j = 25 °C; Fig. 18		-	50	-	pF
C_{oss}	output capacitance			-	15	-	pF
C_{rss}	reverse transfer capacitance			-	0.2	-	pF
$C_{o(er)}$	effective output capacitance, energy related	0 V ≤ V_{DS} ≤ 400 V; V_{GS} = 0 V; T_j = 25 °C; Fig. 19	[1]	-	20	-	pF

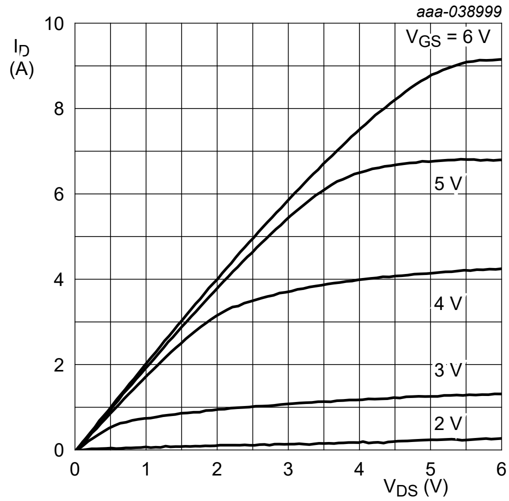
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$C_{o(tr)}$	effective output capacitance, time related	0 V ≤ V_{DS} ≤ 400 V; V_{GS} = 0 V; T_j = 25 °C	[2]	-	28	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 400 V; V_{GS} = 6 V; I_D = 4.4 A; L = 318 μH; R_{on} = 10 Ω; R_{off} = 2 Ω; Fig. 20; Fig. 21		-	0.9	-	ns
t_r	rise time			-	3.5	-	ns
$t_{d(off)}$	turn-off delay time			-	1.2	-	ns
t_f	fall time			-	6.1	-	ns
Q_{oss}	output charge	V_{GS} = 0 V; V_{DS} = 400 V; T_j = 25 °C; Fig. 22	[3]	-	13	-	nC
Source-drain characteristics							
V_{SD}	source-drain voltage	I_S = 2.2 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 23; Fig. 24; Fig. 25; Fig. 26		-	2.6	-	V

[1] $CO_{(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V
[2] $CO_{(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V
[3] Q_r is not specified separately from Q_{oss} for e-mode GaN FETs, since $Q_r = Q_{oss} + Q_D$, and Q_D = 0. (Q_D is charge associated with diffusion of minority carriers. Since there is no body diode, no minority carriers in excess of Q_{oss} have to be transferred for e-mode GaN FETs.)



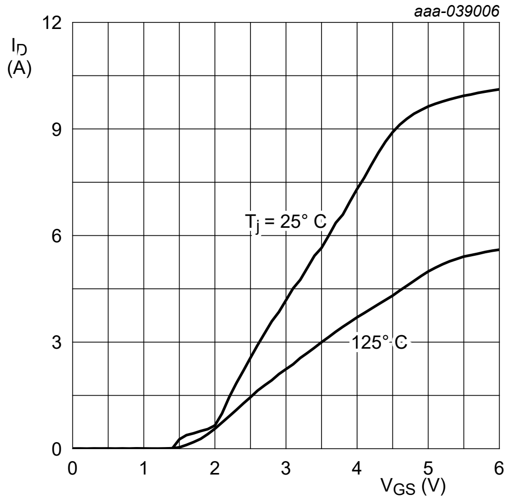
T_j = 25 °C

Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values



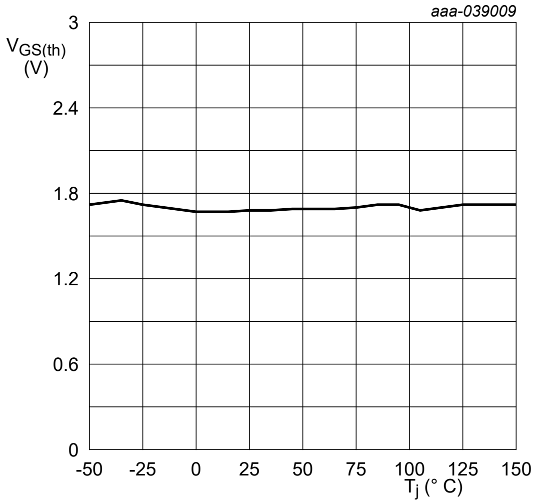
T_j = 125 °C

Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values



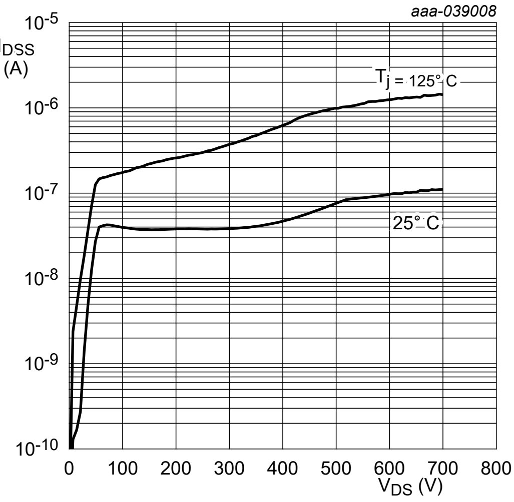
V_{DS} = 3 V

Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values



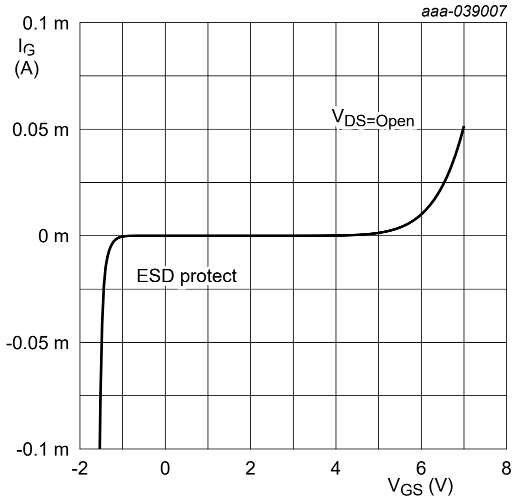
I_D = 6.6 mA ; V_{DS} = V_{GS}

Fig. 9. Gate-source threshold voltage as a function of junction temperature; typical values



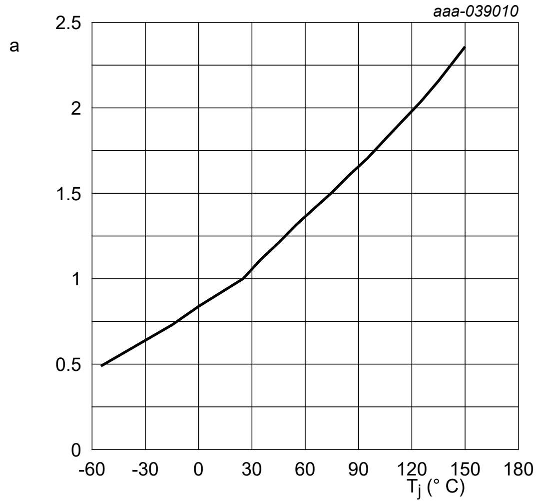
V_{GS} = 0 V

Fig. 10. Drain-source current as a function of drain-source voltage; typical values



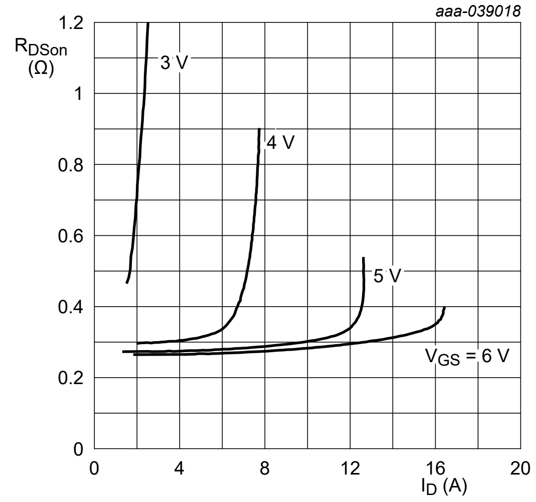
Ig reverse turn on by ESD unit

Fig. 11. Gate-source current as a function of gate-source voltage; typical values



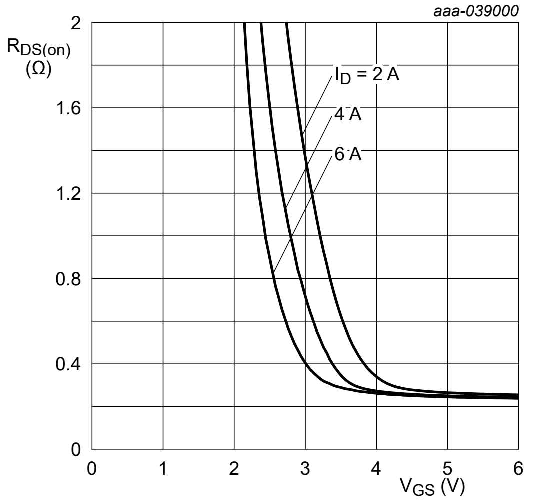
$$a = \frac{R_{DSon}}{R_{DSon\,(25°C)}}$$

Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature



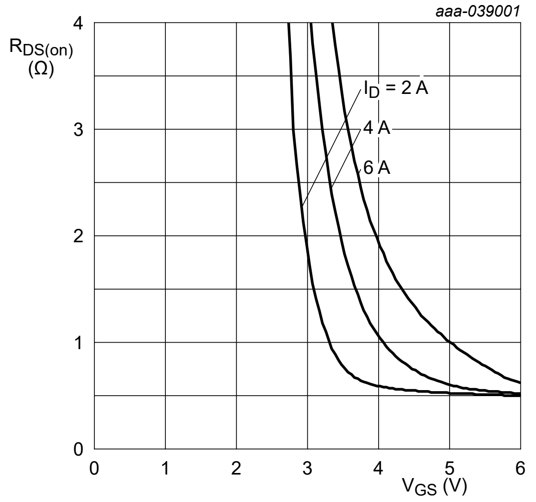
T_j = 25 °C

Fig. 13. Drain-source on-state resistance as a function of drain current ; typical values



T_j = 25 °C

Fig. 14. Drain-source on-state resistance as a function of gate-source voltage; typical values



T_j = 125 °C

Fig. 15. Drain-source on-state resistance as a function of gate-source voltage; typical values

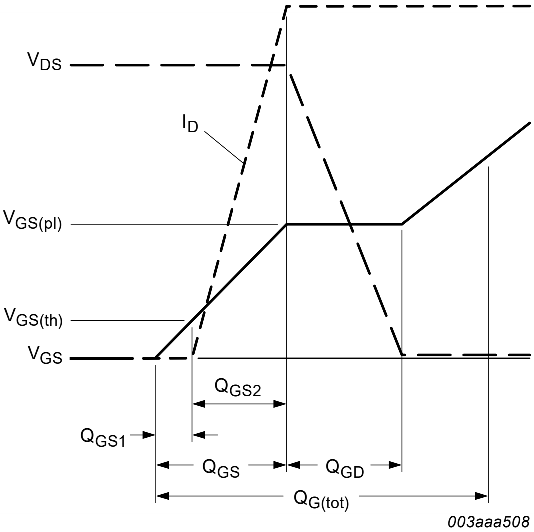
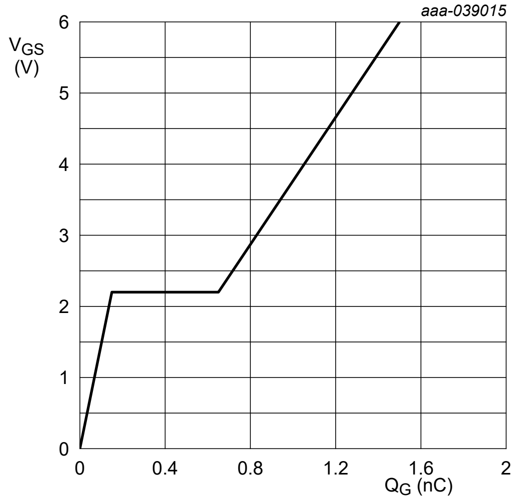
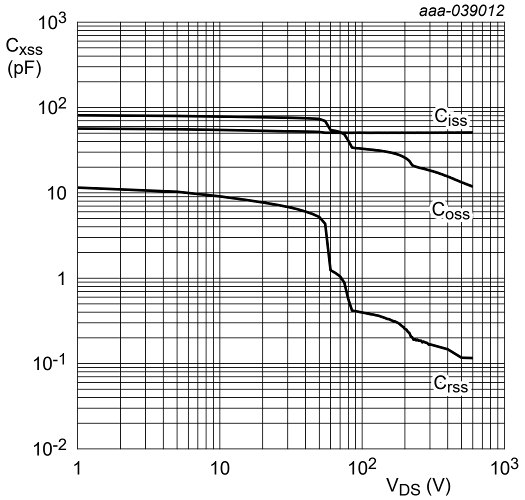


Fig. 16. Gate charge waveform definitions



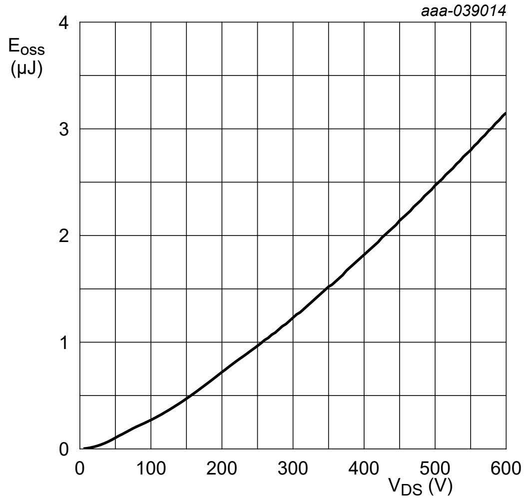
T_J = 25 °C ; I_D = 2.2 A

Fig. 17. Gate-source voltage as a function of gate charge; typical values



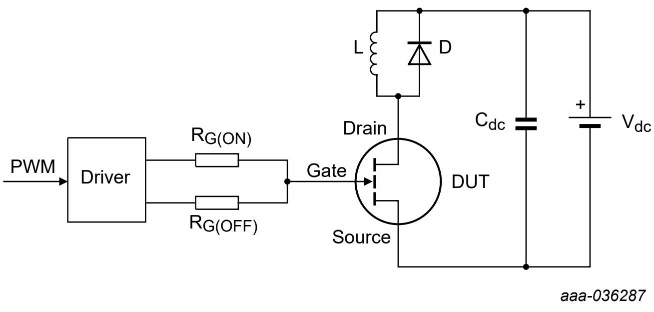
V_{GS} = 0 V; f = 100 kHz

Fig. 18. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



Freq. = 100 kHz

Fig. 19. COSS stored energy as a function of drain-source voltage; typical values



V_{DS} = 400 V; I_D = 4.4 A; L = 318 µH; V_{GS} = 6 V; R_{on} = 10 Ω; R_{off} = 2 Ω

Fig. 20. Switching time test circuit with inductive load

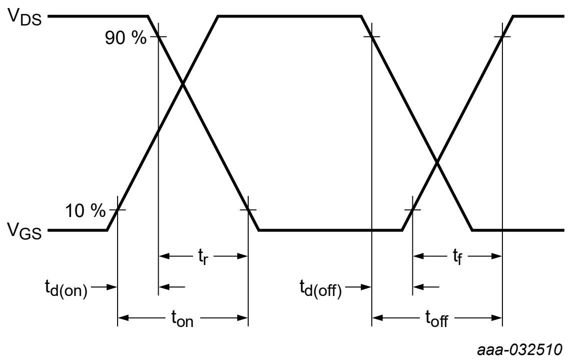
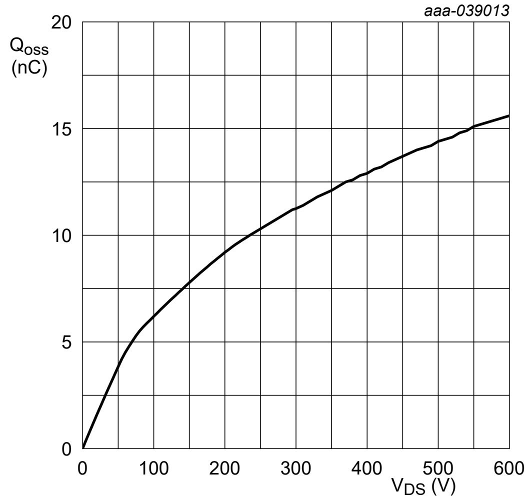
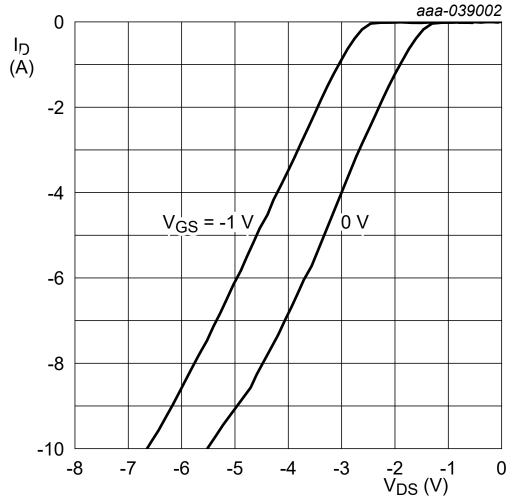


Fig. 21. Switching time waveform



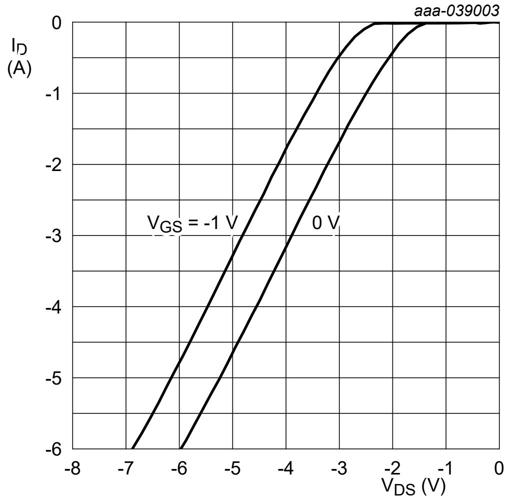
Freq. = 100 kHz

Fig. 22. Output charge as a function of drain-source voltage; typical values



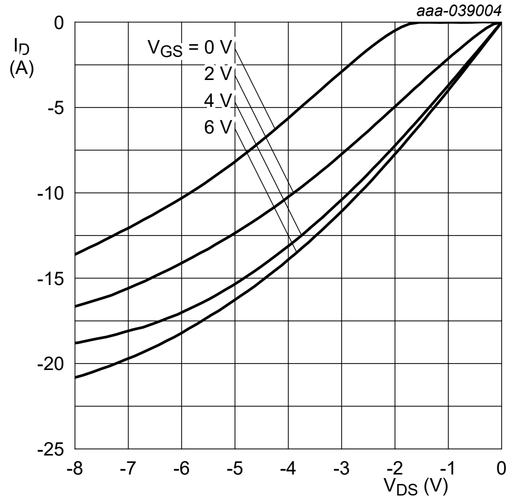
T_j = 25 °C

Fig. 23. Source current as a function of source-drain voltage; typical values



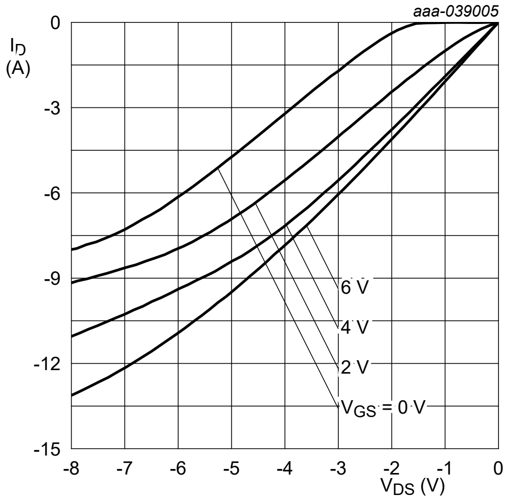
T_j = 125 °C

Fig. 24. Source current as a function of source-drain voltage; typical values



T_j = 25 °C

Fig. 25. Source current as a function of source-drain voltage; typical values

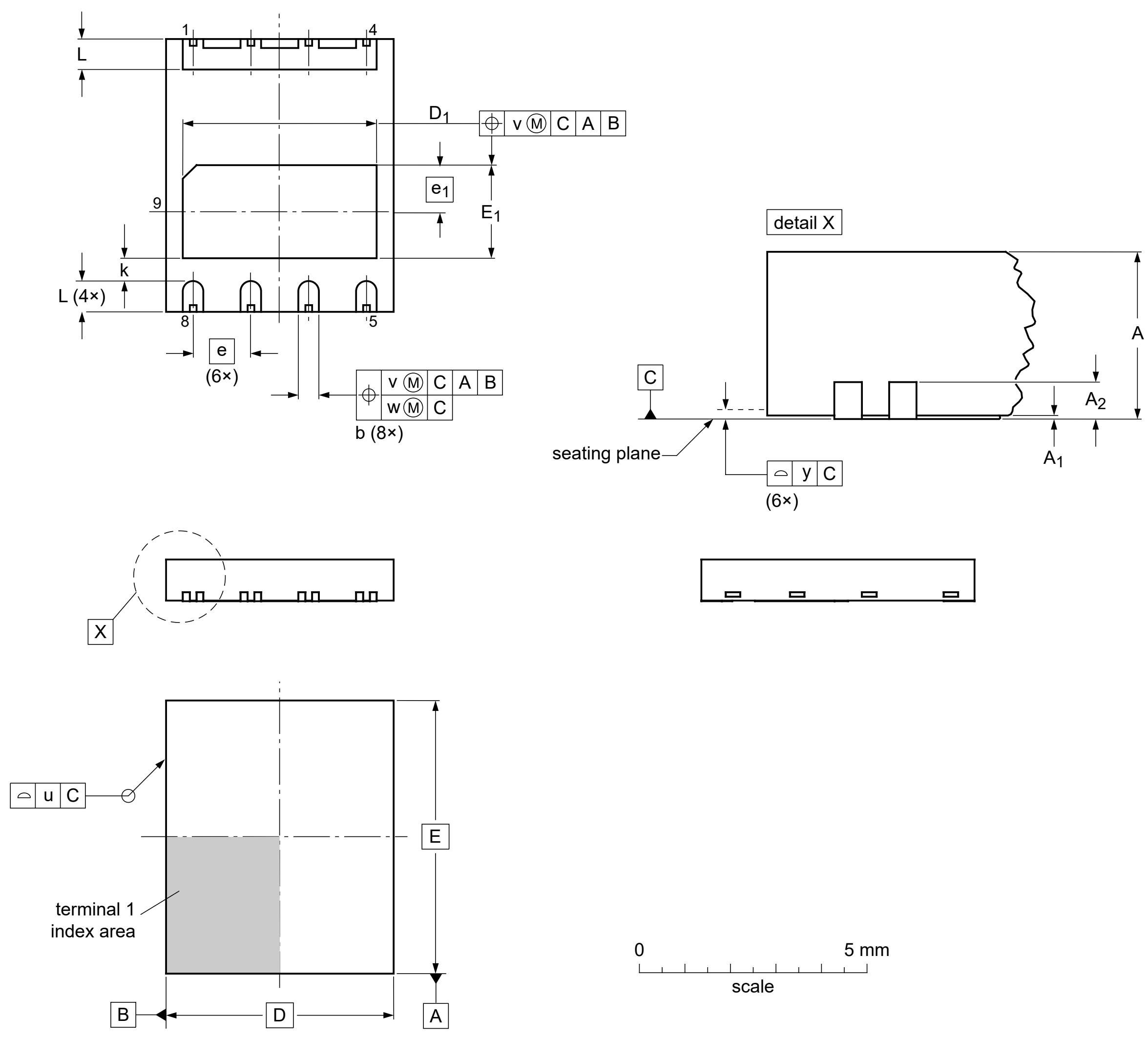


T_j = 125 °C

Fig. 26. Source current as a function of source-drain voltage; typical values

11. Package outline

DFN5060-5: plastic thermal enhanced small outline package; no leads; 5 terminals; body: 5 × 6 × 0.9 mm **SOT8075-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	D_1	E	E_1	e	e_1	k	L	u	v	w	y
	max	1.0	0.05		0.50		4.36		2.15				0.775				
mm	nom	0.9	0.02	0.203 REF	0.45	5 BSC	4.26	6 BSC	2.05	1.27 BSC	0.8 BSC	0.5 REF	0.675	0.1	0.1	0.05	0.1
	min	0.8	0.00		0.40		4.16		1.95				0.575				

sot8075-1_po

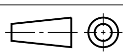
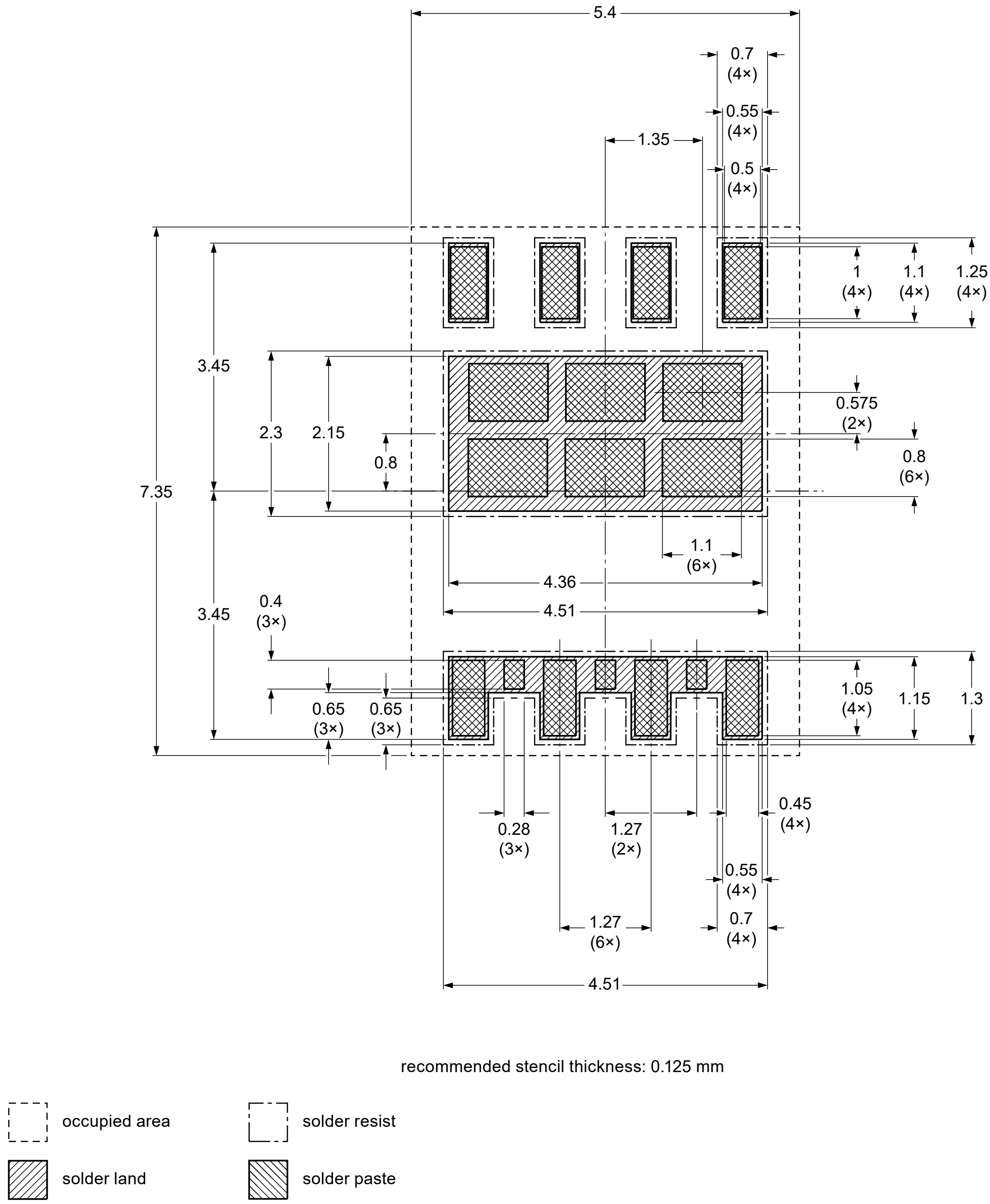
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8075-1		MO-229 compatible				23-03-03

Fig. 27. Package outline DFN5060-5 (SOT8075-1)

12. Soldering

Footprint information for reflow soldering of DFN5060-5 package **SOT8075-1**



Dimensions in mm

Issue date 23-03-17

sot8075-1_fr

Fig. 28. Reflow soldering footprint for DFN5060-5 (SOT8075-1)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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