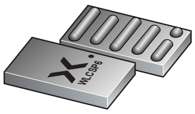

# GANE7R0-100CBA

## 100 V, 7.0 mOhm Gallium Nitride (GaN) FET in a 2.5 mm x 1.5 mm Wafer Level Chip-Scale Package (WLCSP)

13 March 2025 Product data sheet

## 1. General description

The GANE7R0-100CBA is a a general purpose 100 V, 7.0 mΩ Gallium Nitride (GaN) FET in a Wafer Level Chip-Scale Package (WLCSP). It is a normally-off e-mode device offering superior performance and very low on-state resistance.

## 2. Features and benefits

- Enhancement mode - normally-off power switch
- Ultra high frequency switching capability
- No body diode
- Low gate charge, low output charge
- Qualified for standard applications
- RoHS, Pb-free, REACH-compliant
- High efficiency and high power density
- Wafer Level Chip-Scale Package (WLCSP) 2.5 mm x 1.5 mm

## 3. Applications

- High power density and high efficiency power conversion
- AC-to-DC converters, (secondary stage)
- High frequency DC-to-DC converters in 48 V systems
- 400 V to 48 V LLC converters, secondary (rectification) side
- Fast battery charging, mobile phone, laptop, tablet and USB type-C chargers
- Datacom and telecom (AC-to-DC and DC-to-DC) converters
- Motor drives
- LiDAR (non-automotive)
- Class D audio amplifiers

## 4. Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | -40 °C ≤ $T_j$ ≤ 150 °C | | - | - | 100 | V |
| $I_D$ | drain current | $V_{GS}$ = 5 V; $T_{mb}$ = 25 °C | [1] | - | - | 29 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 1 | | - | - | 182 | W |
| $T_j$ | junction temperature | | | -40 | - | 150 | °C |
| **Static characteristics** | | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 5 V; $I_D$ = 16 A; $T_j$ = 25 °C; Fig. 8; Fig. 9; Fig. 10 | | - | 5.5 | 7 | mΩ |
| | | $V_{GS}$ = 5 V; $I_D$ = 16 A; $T_j$ = 150 °C; Fig. 8; Fig. 11 | | - | 11.8 | - | mΩ |
| $R_G$ | gate resistance | f = 5 MHz; open drain | | - | 1.9 | - | Ω |

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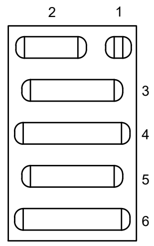
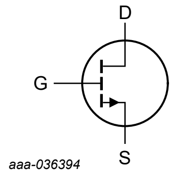
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Dynamic characteristics** | | | | | | | |
| $Q_{GD}$ | gate-drain charge | $I_D$ = 16 A; $V_{DS}$ = 50 V; $V_{GS}$ = 5 V; $T_j$ = 25 °C; Fig. 12; Fig. 13 | | - | 0.8 | - | nC |
| $Q_{G(tot)}$ | total gate charge | | | - | 4.5 | - | nC |
| $Q_{oss}$ | output charge | $V_{GS}$ = 0 V; $V_{DS}$ = 50 V; Fig. 16 | [2] | - | 25 | - | nC |

[1] Limited by package
[2] $Q_r$ is not specified separately from $Q_{oss}$ for e-mode GaN FETs, since $Q_r = Q_{oss} + Q_D$, and $Q_D$ = 0. ($Q_D$ is charge associated with diffusion of minority carriers. Since there is no body diode, no minority carriers in excess of $Q_{oss}$ have to be transferred for e-mode GaN FETs.)

## 5. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | G | gate |  Transparent top view **WLCSP6 (WLCSP6_SOT8090)** |  |
| 2,4,6 | S | source | | |
| 3,5 | D | drain | | |

## 6. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| GANE7R0-100CBA | WLCSP6 | WLCSP6: wafer level chip-size package; 6 bumps | WLCSP6_SOT8090 |

## 7. Marking

**Table 4. Marking codes**

| Type number | Marking code |
|---|---|
| GANE7R0-100CBA | 7R0DCBA |

## 8. Limiting values

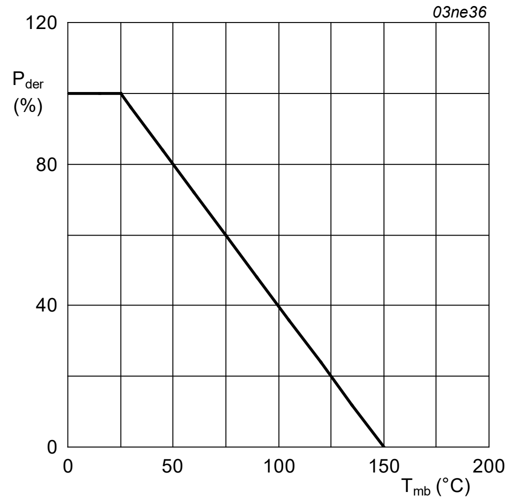
**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | -40 °C ≤ $T_j$ ≤ 150 °C | | - | 100 | V |
| $V_{GS}$ | gate-source voltage | | | -4 | 6 | V |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 1 | | - | 182 | W |
| $I_D$ | drain current | $V_{GS}$ = 5 V; $T_{mb}$ = 25 °C | [1] | - | 29 | A |
| $I_{DM}$ | peak drain current | pulsed; $t_p$ = 100 µs; $T_{mb}$ = 25 °C; Fig. 2 | | - | 125 | A |

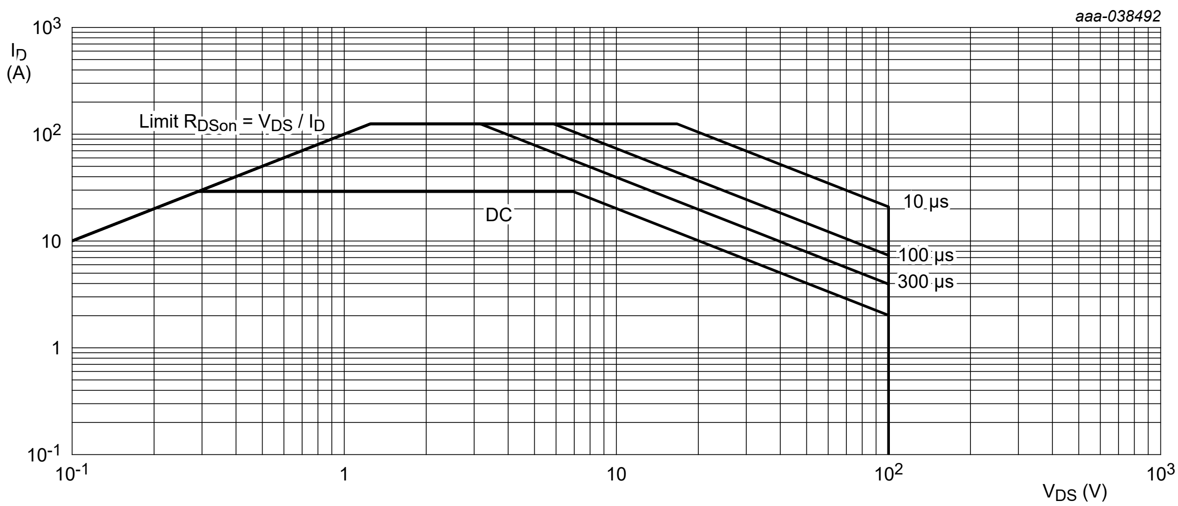
| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $T_{stg}$ | storage temperature | | | -40 | 150 | °C |
| $T_j$ | junction temperature | | | -40 | 150 | °C |
| $T_{sld(M)}$ | peak soldering temperature | | | - | 260 | °C |

[1] Limited by package




$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

**Fig. 1. Normalized total power dissipation as a function of mounting base temperature**




$T_{mb}$ = 25 °C; $I_{DM}$ is a single pulse

**Fig. 2. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

# 9. Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-c)}$ | thermal resistance from junction to case | Fig. 3 | | - | - | 0.62 | K/W |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | | | - | - | 1.98 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | | [1] | - | - | 62.76 | K/W |

[1] $R_{th(j-a)}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

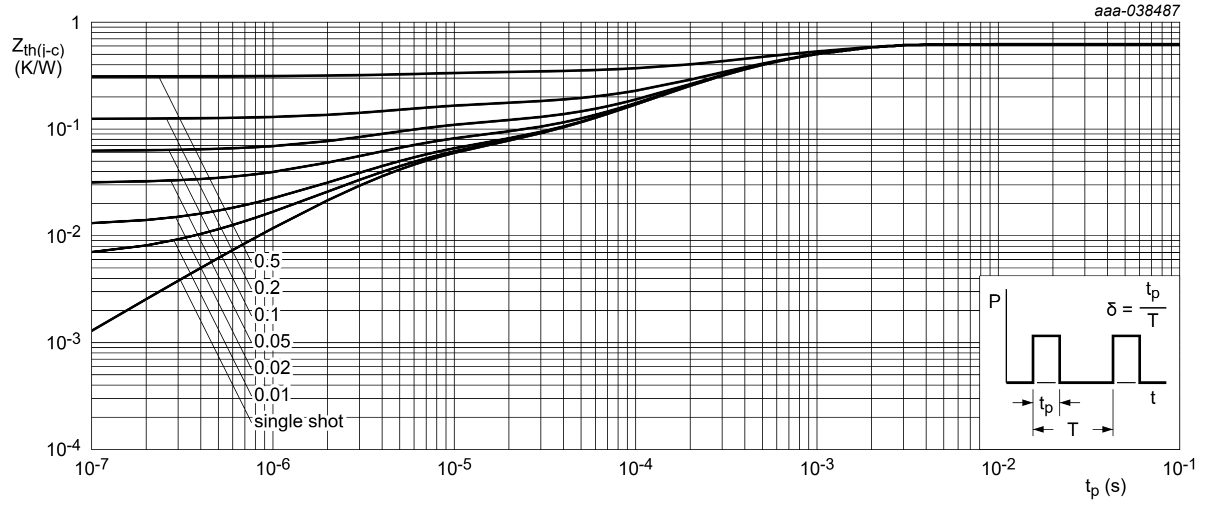



**Fig. 3. Transient thermal impedance from junction to case as a function of pulse duration**

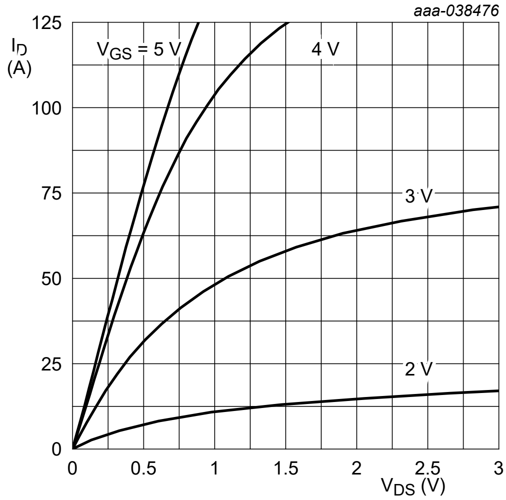
## 10. Characteristics

**Table 7. Characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 4.3 mA; $V_{DS}$=$V_{GS}$; $T_j$ = 25 °C; Fig. 7 | | 0.8 | 1.1 | 2.5 | V |
| | | $I_D$ = 4.3 mA; $V_{DS}$=$V_{GS}$; $T_j$ = 150 °C; Fig. 7 | | - | 1 | - | V |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 80 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | - | 1.5 | 14 | µA |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = 5 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | 1 | 15 | µA |
| | | $V_{GS}$ = 5 V; $V_{DS}$ = 0 V; $T_j$ = 125 °C | | - | 50 | 1000 | µA |
| | | $V_{GS}$ = -4 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | 0.1 | 0.5 | µA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 5 V; $I_D$ = 16 A; $T_j$ = 25 °C; Fig. 8; Fig. 9; Fig. 10 | | - | 5.5 | 7 | mΩ |
| | | $V_{GS}$ = 5 V; $I_D$ = 16 A; $T_j$ = 150 °C; Fig. 8; Fig. 11 | | - | 11.8 | - | mΩ |
| $R_G$ | gate resistance | f = 5 MHz; open drain | | - | 1.9 | - | Ω |
| **Dynamic characteristics** | | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D$ = 16 A; $V_{DS}$ = 50 V; $V_{GS}$ = 5 V; $T_j$ = 25 °C; Fig. 12; Fig. 13 | | - | 4.5 | - | nC |
| $Q_{GS}$ | gate-source charge | | | - | 1 | - | nC |
| $Q_{GD}$ | gate-drain charge | | | - | 0.8 | - | nC |

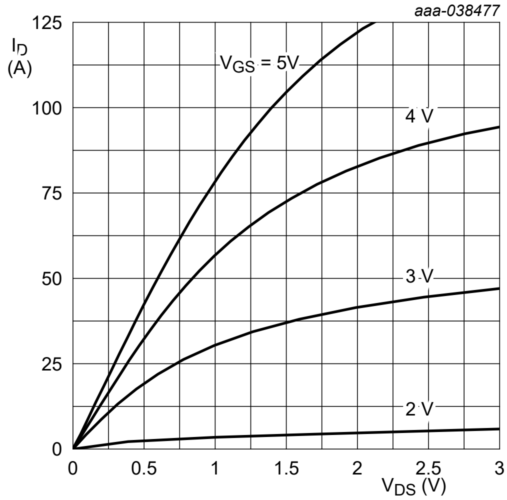
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $C_{iss}$ | input capacitance | $V_{DS}$ = 50 V; $V_{GS}$ = 0 V; f = 100 kHz; $T_j$ = 25 °C; Fig. 14 | | - | 485 | - | pF |
| $C_{oss}$ | output capacitance | | | - | 220 | - | pF |
| $C_{rss}$ | reverse transfer capacitance | | | - | 3.5 | - | pF |
| $C_{o(er)}$ | effective output capacitance, energy related | $V_{DS}$ = 50 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C; Fig. 15 | [1] | - | 340 | - | pF |
| $C_{o(tr)}$ | effective output capacitance, time related | $V_{DS}$ = 50 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | [2] | - | 500 | - | pF |
| $Q_{oss}$ | output charge | $V_{GS}$ = 0 V; $V_{DS}$ = 50 V; Fig. 16 | [3] | - | 25 | - | nC |
| **Source-drain characteristics** | | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 0.5 A; $V_{GS}$ = 0 V; $T_j$ = 25 °C; Fig. 17; Fig. 18; Fig. 19; Fig. 20 | | - | 1.4 | - | V |

[1] $C_{O(er)}$ is the fixed capacitance that gives the same stored energy as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 50 V
[2] $C_{O(tr)}$ is the fixed capacitance that gives the same charging time as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 50 V
[3] $Q_r$ is not specified separately from $Q_{oss}$ for e-mode GaN FETs, since $Q_r = Q_{oss} + Q_D$, and $Q_D$ = 0. ($Q_D$ is charge associated with diffusion of minority carriers. Since there is no body diode, no minority carriers in excess of $Q_{oss}$ have to be transferred for e-mode GaN FETs.)



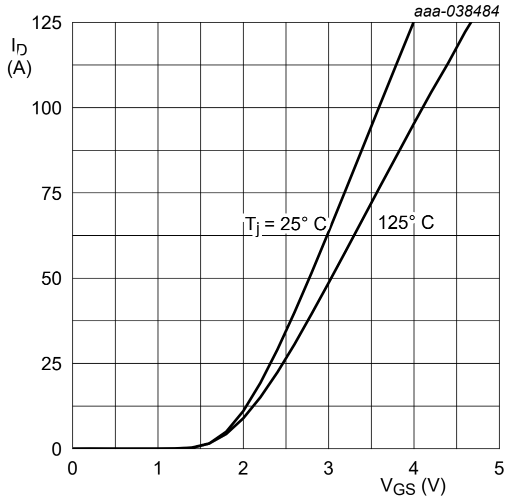

$T_j$ = 25 °C

**Fig. 4. Output characteristics: drain current as a function of drain-source voltage; typical values**



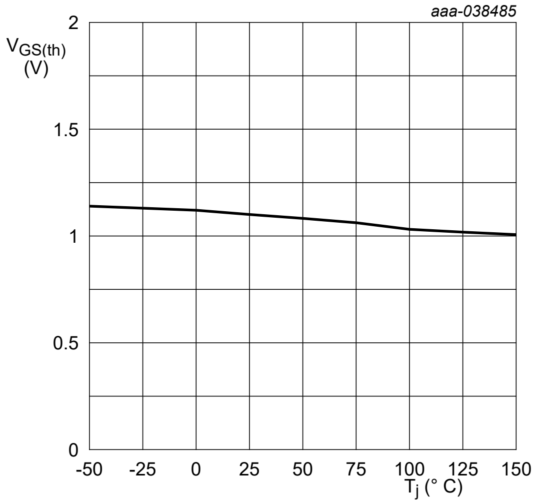

$T_j$ = 125 °C

**Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values**



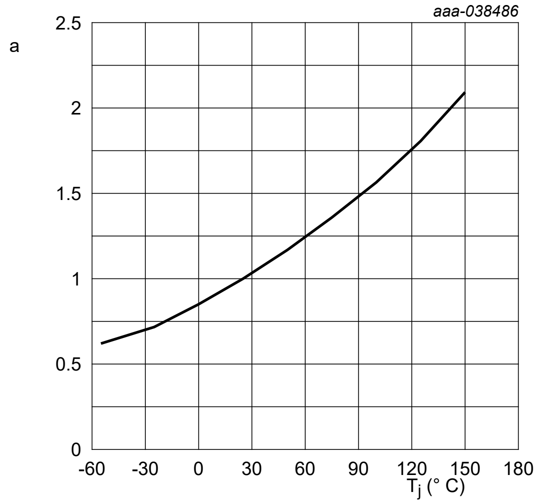

$V_{DS}$ = 3 V

**Fig. 6. Transfer characteristics; drain current as a function of gate-source voltage; typical values**



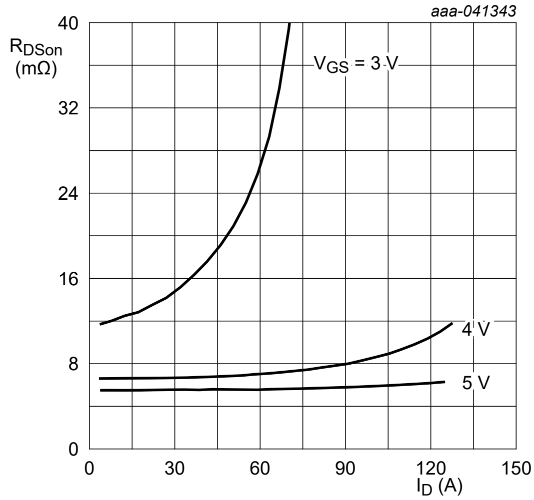

$I_D$ = 4.3 mA ; $V_{DS}$ = $V_{GS}$

**Fig. 7. Gate-source threshold voltage as a function of junction temperature; typical values**



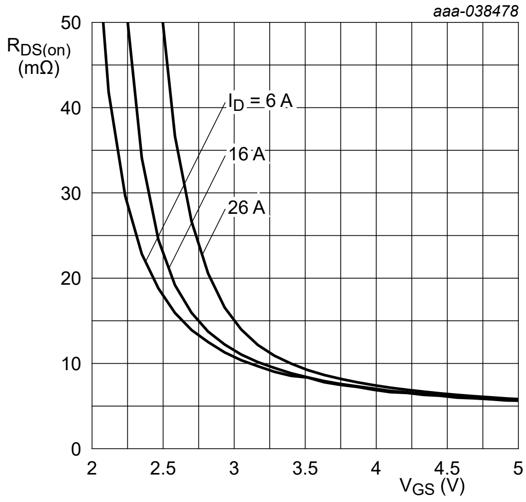

$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

**Fig. 8. Normalized drain-source on-state resistance factor as a function of junction temperature**



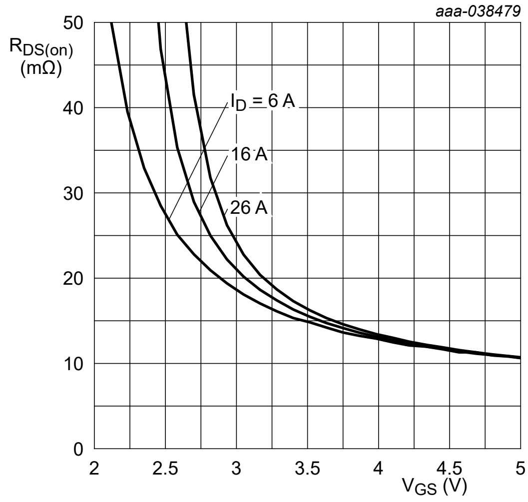

$T_j$ = 25 °C

**Fig. 9. Drain-source on-state resistance as a function of drain current ; typical values**




$T_j$ = 25 °C

**Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values**




$T_j$ = 125 °C

**Fig. 11. Drain-source on-state resistance as a function of gate-source voltage; typical values**

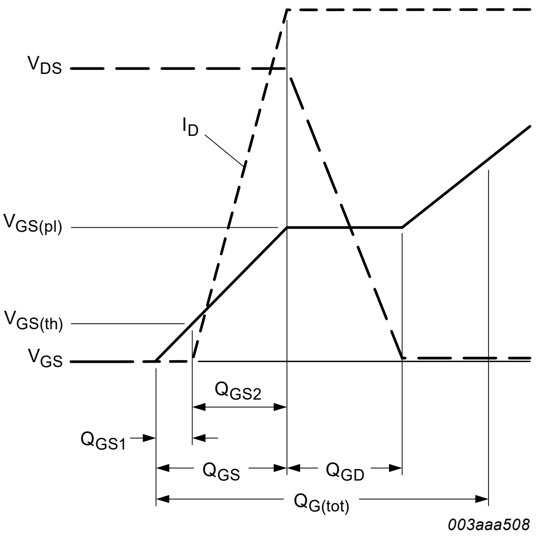
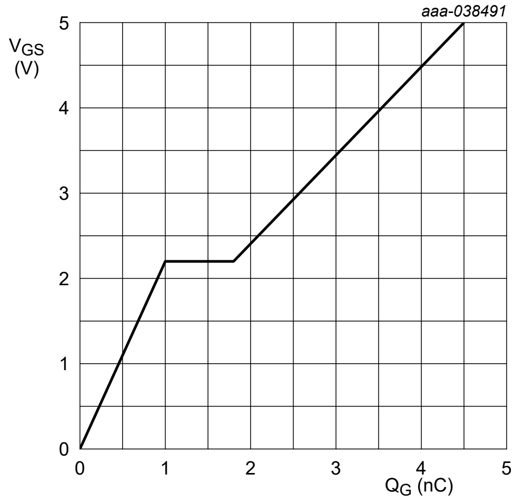
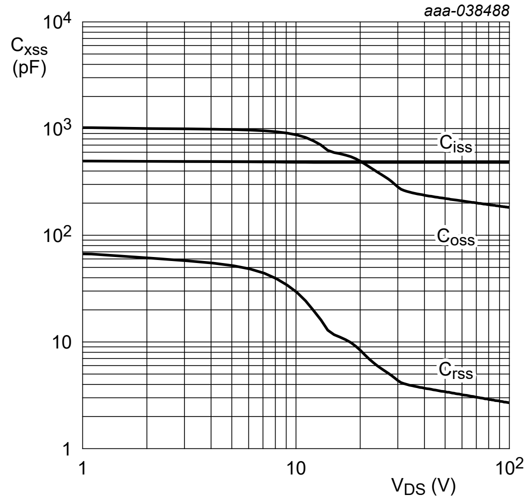



**Fig. 12. Gate charge waveform definitions**



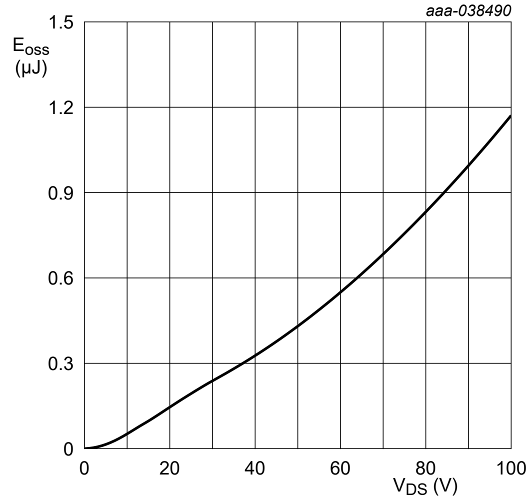

$T_J$ = 25 °C ; $I_D$ = 16A

**Fig. 13. Gate-source voltage as a function of gate charge; typical values**



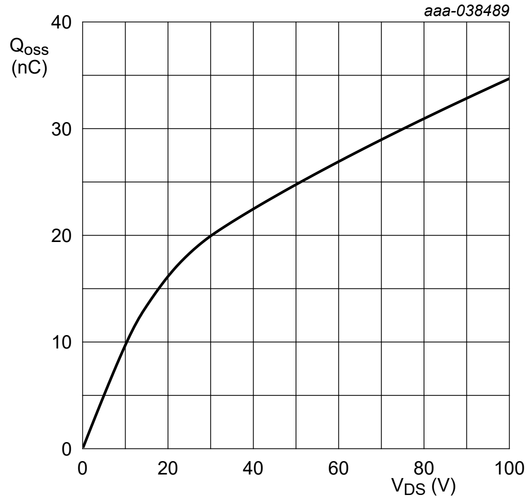

$V_{GS}$ = 0 V; f = 100 kHz

**Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



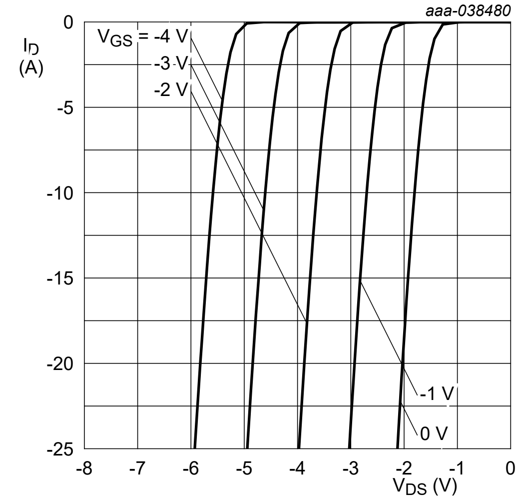

Freq. = 100 kHz

**Fig. 15. COSS stored energy as a function of drain-source voltage; typical values**



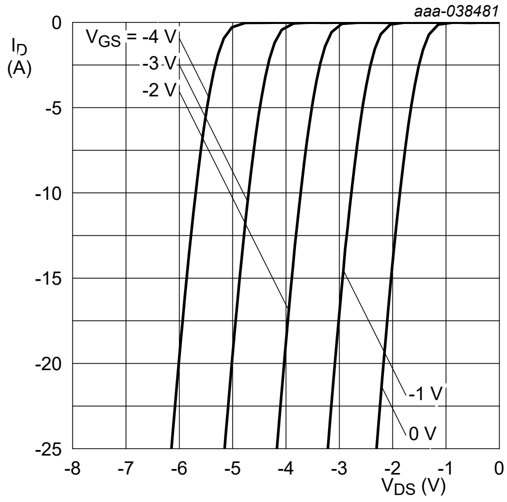

Freq. = 100 kHz

**Fig. 16. Output charge as a function of drain-source voltage; typical values**



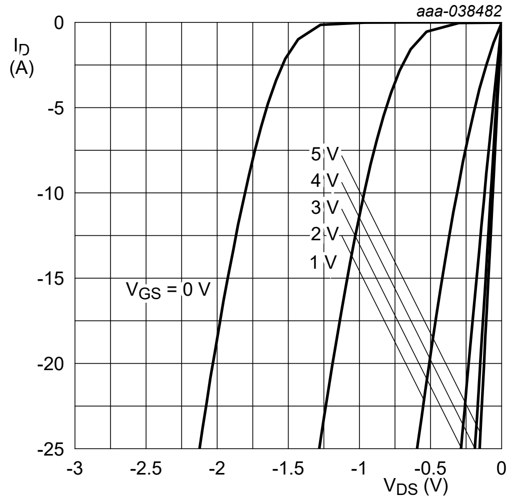

$T_j$ = 25 °C

**Fig. 17. Source current as a function of source-drain voltage; typical values**



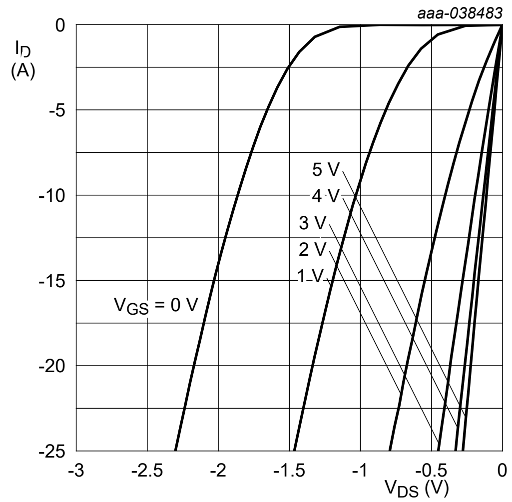

$T_j$ = 125 °C

Fig. 18. Source current as a function of source-drain voltage; typical values




$T_j$ = 25 °C

Fig. 19. Source current as a function of source-drain voltage; typical values

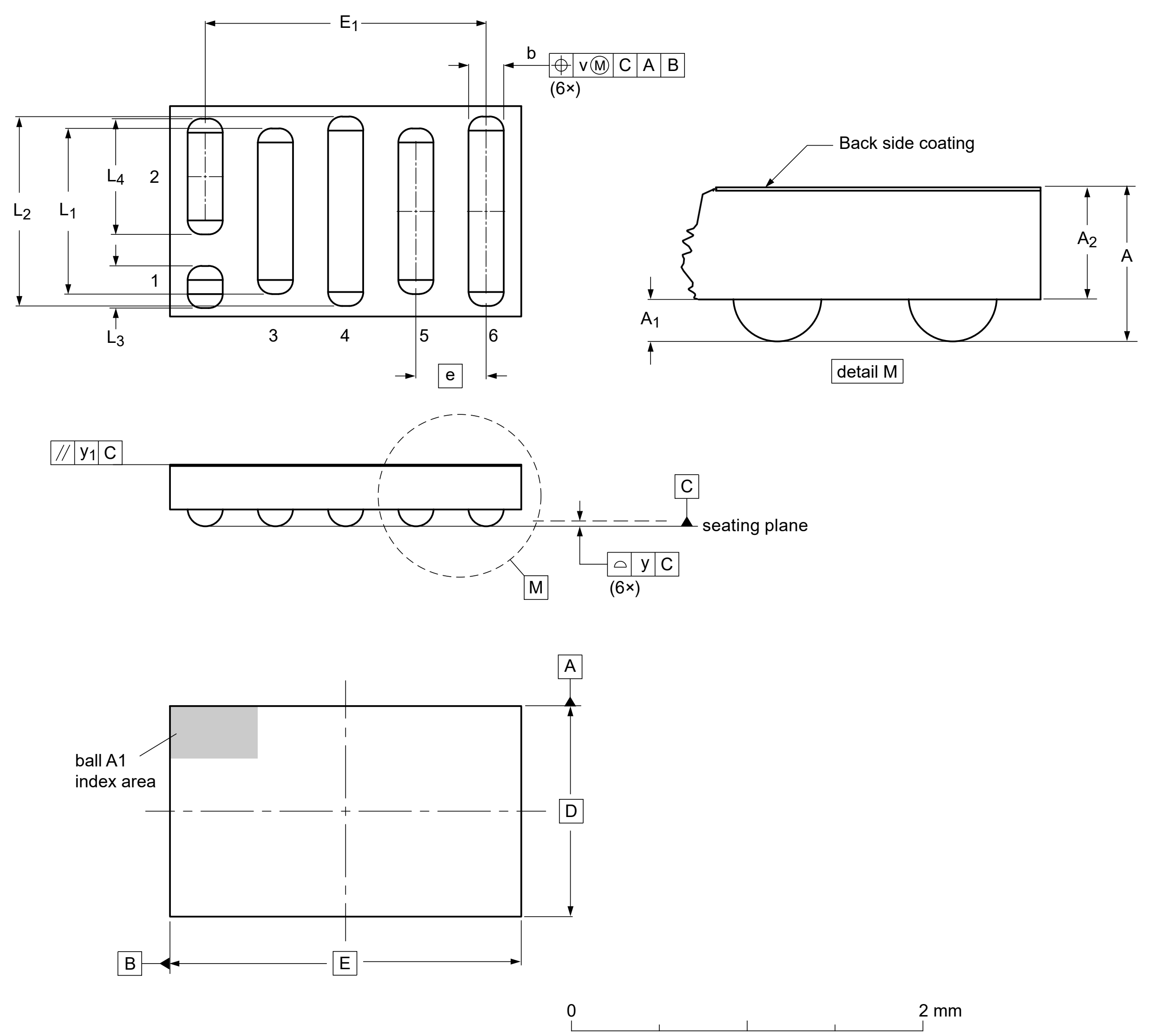



$T_j$ = 125 °C

Fig. 20. Source current as a function of source-drain voltage; typical values

## 11. Package outline

**WLCSP6: wafer level chip-size package; 6 bumps** **WLCSP6_SOT8090**




Dimensions (mm are the original dimensions)

| Unit(1) | | A | $A_1$ | $A_2$ | b | D | E | $E_1$ | e | $L_1$ | $L_2$ | $L_3$ | $L_4$ | v | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 0.465 | | 0.365 | 0.27 | 1.525 | 2.525 | | | 1.195 | 1.37 | 0.32 | 0.845 | | | |
| | nom | | | | 0.25 | 1.500 | 2.500 | 2.00 BSC | 0.5 BSC | 1.175 | 1.35 | 0.30 | 0.825 | 0.05 | 0.05 | 0.1 |
| | min | | 0.10 | | 0.23 | 1.475 | 2.475 | | | 1.155 | 1.33 | 0.28 | 0.805 | | | |

*wlcsp6_sot8090_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| WLCSP6_SOT8090 | | | | | | 25-01-08 |

**Fig. 21. Package outline WLCSP6 (WLCSP6_SOT8090)**

# 12. Soldering

**Footprint information for reflow soldering of WLCSP6 package** **SOT8090-1**

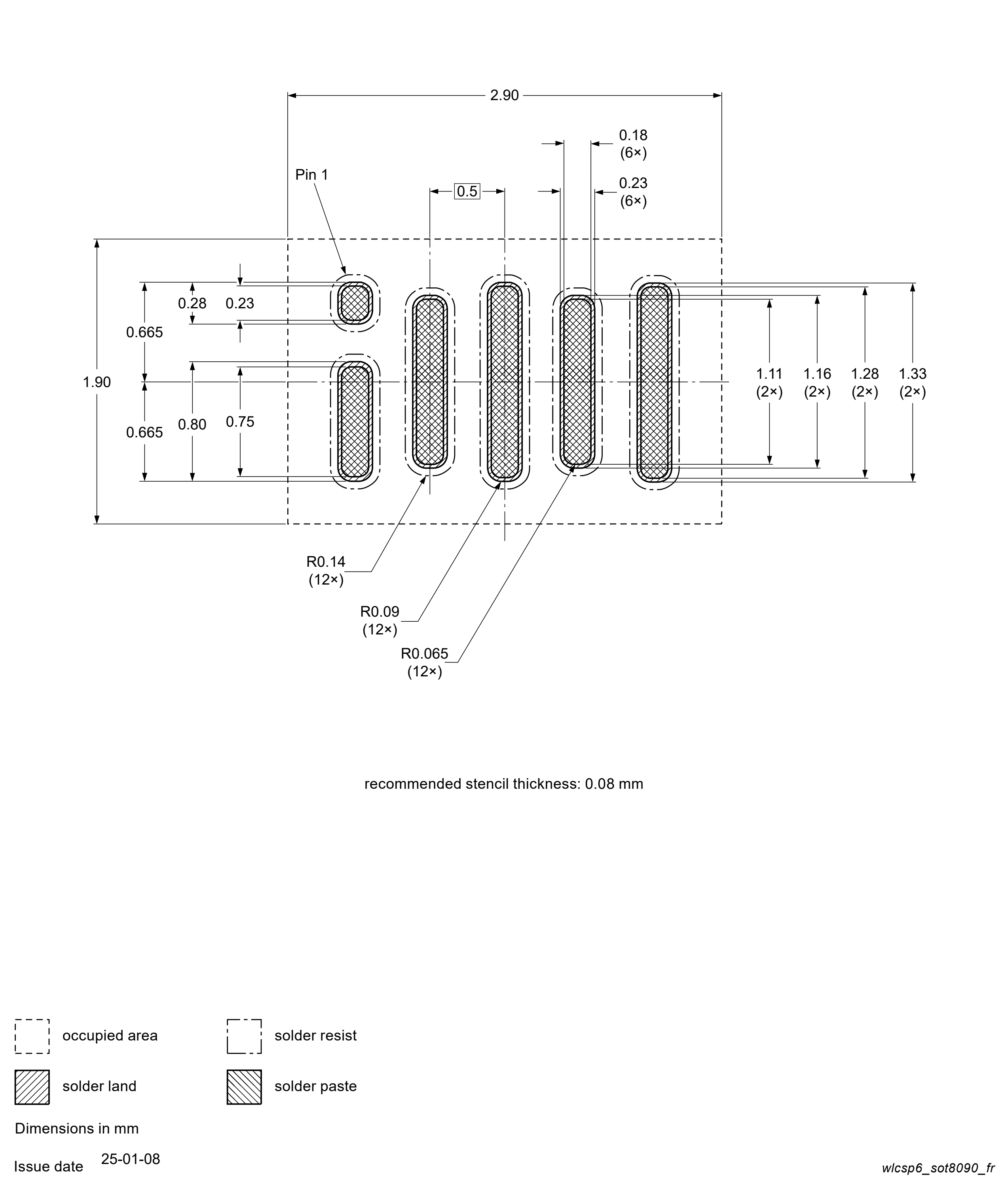



**Fig. 22. Reflow soldering footprint for WLCSP6 (WLCSP6_SOT8090)**

# 13. Legal information

### Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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# Contents





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