Mask Set Errata for Mask 0N97Y

This report applies to mask 0N97Y for these products:

- MIMXRT1011DAE5A
- MIMXRT1011CAE4A

Table 1. Errata and Information Summary

Erratum ID	Erratum Title
ERR050143	CCM: SoC will enter low power mode before the ARM CPU executes WFI when improper low power sequence is used
ERR006223	Failure to resume from WAIT/STOP mode with power gating
ERR011377	FlexSPI: DLL lock status bit not accurate due to timing issue
ERR050130	PIT: Temporary incorrect value reported in LMTR64H register in lifetimer mode
ERR050327	SWRESET on flexspi keyblob fetching state machine will impact software driver

Table 2. Revision History

Revision	Changes
0	Initial revision

ERR050143: CCM: SoC will enter low power mode before the ARM CPU executes WFI when improper low power sequence is used

Description: When software tries to enter the low power mode with the following sequence, SoC enters the low power mode before the ARM CPU executes the WFI instructions.

- Set CCM_CLPCR[1:0] to 2’b00
- ARM CPU enters WFI

- ARM CPU wakes up from an interrupt event, which is masked by GPC or not visible to GPC, such as an interrupt from local timer.
- Set CCM_CLPCR[1:0] to 2’b01 or 2’b10
- ARM CPU executes WFI

Before the last step, SoC enters the WAIT mode if CCM_CLPCR[1:0] is set to 2’b01, or enters the STOP mode if CCM_CLPCR[1:0] is set to 2’b10.

Workaround: Software workaround

1) Trigger IRQ #41 (IOMUX), which is always pending by setting IOMUX_GPR1_GINT bit

2) Unmask IRQ #41 in GPC before setting the CCM low power mode

3) Mask IRQ #41 right after the CCM low power mode is set (set bit0-1 of CCM_CLPCR)

ERR006223: Failure to resume from WAIT/STOP mode with power gating

Description: When entering WAIT/STOP mode with power gating of the core(s), if an interrupt arrives during the power down sequence, the system could enter an unexpected state and fail to resume.

Workaround: Use REG_BYPASS_COUNTER (RBC) to hold off interrupts when the PGC unit is in the middle of power down sequence. The counter needs to be set/cleared only when no interrupts pending. To use the work around effectively, the counter needs to be enabled as close to WFI as possible.

Following equation can be used to aid determination of RBC counter value.

RBC_COUNT * (1 / 32K RTC Frequency) >= (25 + PDNSCR_SW2ISO) * (1 / IPG_CLK Frequency)

PDNSCR_ISO2SW = PDNSCR_ISO = 1 (counts in IPG_CLK clock domain)

ERR011377: FlexSPI: DLL lock status bit not accurate due to timing issue

Description: After configuring DLL and the lock status bit is set, still may get wrong data if immediately read/write from FLEXSPI based external flash due to timing issue

Workaround: Adding a delay time (100 NOP) after the DLL lock status is set.

ERR050130: PIT: Temporary incorrect value reported in LMTR64H register in lifetimer mode

Description: When the Programmable interrupt timer (PIT) module is used in lifetimer mode, timer 0 and timer 1 are chained and the timer load start value (LDVAL0[TSV] and LDVAL1[TSV]) are set according to the application need for both timers. When timer 0 current time value (CVAL0[TVL]) reaches 0x0 and subsequently reloads to LDVAL0[TSV], then timer 1 CVAL1[TVL] should decrement by 0x1.

However this decrement does not occur until one cycle later, therefore a read of the PIT upper lifetime timer register (LTMR64H) is followed by a read of the PIT lower lifetime timer register (LTMR64L) at the instant when timer 0 has reloaded to LDVAL0[TSV] and timer 1 is yet to be decremented in next cycle then an incorrect timer value in LTMR64H[LTH] is expected.

Workaround: In lifetimer mode if the read value of LTMR64L[LTL] is equal to LDVAL0[TSV] then read both LTMR64H and LTMR64L registers one additional time to obtain the correct lifetime value.

ERR050327: SWRESET on flexspi keyblob fetching state machine will impact software driver

Description: In this version, OTFAD keyblob done/error bit can be cleared by flexspi SWRESET.

When keyblob done/error status bit is 0, AHB bus access can be blocked since FlexSPI needs to wait OTFAD finishes its key blob processing.

But in some software drivers, SW reset is used after every flash erase/program. This makes FlexSPI lost its keyblob processing result and AHB bus error shows up in following AHB bus access.

Workaround: Using AHBCR[CLRAHBXBUF] instead of SW reset after page program or erase.

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