IS43DR00-001.AN

ISSI DDR2 SDRAM Design Considerations Guide

1. Introduction

This is a general board design considerations guideline for ISSI DDR2 SDRAM, especially for point to point applications. Chipset companies may have their own application notes for designing using DDR2 DRAM. ISSI recommends following the chipset company's guidelines first.

2. PCB Layout Guidelines

50–60Ω impedance (ZO) is recommended for all traces. FR-4 is commonly used for the dielectric material. The board thickness and trace width and thickness should be adjusted to match the impedance. Trace lengths are also influential, and they should be determined by simulation for each signal group and verified in test.

In general, ISSI recommends the minimum rules for traces in the board as shown below for the minimization of crosstalk. These rules are based on the assumption of a signal slew rate of 1V/1ns. In slower applications, cross-talk generally is not a factor, and closer spacing may be allowed.

1. Signals from the same net group should be routed on the same layer.
2. Signals from Byte group, such as DQS, DM and 8 bits of DQ, must be routed in the same layer
3. The deviation of signal propagation delay is dependent on the timing budget on the application. The following values in the table are good examples at the start of a design.

Signals on Net	Maximum deviation of signal propagation difference.	Maximum deviation of trace length.
All data, address and command signals must be followed within this variation.	±50ps	±6.635mm(261mil)
Between CK and CK#. Between DQSn and DQS#n	±2 ps	±0.254mm (10mil)
Between one clock pair and another clock pair, eg) CK/CK# and DQSn/DQS#n	±5 ps	±0.635mm(25mil)
Between signals within byte group(DQS,DM,8bits of DQ)	±10ps	±1.270mm(50mil)

4. Minimum trace width is 0.13mm (5mil).
5. Intranet spacing, the distance between two adjacent traces within a net, is 0.2mm (7mil).
6. Internet spacing, the distance between the two outermost signals of different signal group is 15mil. The same rule applies between one clock pair and another clock pair.
7. Differential clocks should be routed in parallel and keep the trace length short.
8. Differential clocks must be routed on the same layer and placed on an internal layer minimize the noise.
9. Keep the internet spacing rule between CKE and CK/CK#

3. V$_{REF}$ control

Setup and hold time margin could be reduced if VREF has noise. VREF integrity should be provided by the user to optimize noise margin in the system. The VREF level is expected to track variations in VDDQ , and the peak-to-peak noise should be met with specification:

1. 1KΩ±1%/1KΩ±1%/ from VDDQ power panel

2. Place a 0.1uF capacitor between VREF and VDDQ

3. Place a 0.1uF capacitor between VREF and VSSQ

4. VREF should have a minimum trace to reduce inductance

5. VREF should keep a distance from other signals to reduce the potential of a decoupling effect

4. EMI and Termination

The DDR2 SDRAM offers full drive strength and reduced drive strength, as recommended by JEDEC. They are controlled by EMRS setting, during initialization. The full drive has an output impedance of about 18Ω and the reduced drive has an output impedance of about 40Ω. Selecting the drive strength should be based on the simulation result.

DDR2 SDRAM offers ODT features for DM, DQS and DQs pins. With a short trace length (less than 5cm), it may not required. Matching impedance by using a serial resistor can also improve the performance, but ODT control is generally recommended for better signal integrity. If a serial resistor is used, 10-33Ω serial resistor can be used and located to the middle portion of the trace.

For the command and address inputs, typically, 10~33Ω serial resistor termination is used and closely located to the transmitting device, if it is required.

For clock inputs, ISSI doesn't recommend any termination, except adding 100~120Ω between differential clocks. The trace needs to be as short as possible to reduce noise.

If any signal trace is longer than 5cm, R$_{TT}$ to V$_{TT}$ will be recommended.

5. Power Supply and Decoupling Capacitors

In most cases, to specifically decouple the DRAM, it is popular and effective to use one or two 10uF or 4.7uf bulk capacitors near LDO and several 0.1uF decoupling capacitors close to the DDR2. However, this recommendation may not be sufficient to cover the wide variety of applications using DDR2 today. Because of this, ISSI recommends comprehensive board simulations to ensure the optimal power supply conditions in DDR2 memory applications.

DDR2 datasheets specify VDD, VDDQ, and VDDL condition as 1.8V+-100mV. This specification is a DC condition for the device that assumes ideal voltage conditions without current deficiencies. VDD and VDDQ often share the same power plane in the board, which can result in level shifts on VDD. This condition is caused by DDR2 high frequency I/O switching (VDDQ) which consumes a large amount of current vs VDD requirements. In typical DDR2 applications, most voltage variations are caused by current limitations, which are the result dynamic power requirements that change over the course of the various operational modes of the DRAM.

The following charts illustrate current deficiencies and voltage drop(s) caused by a change in the operating mode from standby to active. Major factors that contribute to current deficiencies in DDR2 applications are inductances and power supply design methodologies.

Inductances are resistive to current changes, acting as a constraint to the amount of instantaneous current that is available when operating modes change. When the device transitions from standby to active mode, the current demand increases rapidly (Fig 1 - Green trace). If a board design has excessive supply path inductances, this sudden demand increase can easily exceed the capability of the power supply to provide the needed current. The current deficiency resulting from the high inductance is highlighted by the red triangle. The lack of current is visible in the voltage drop (Fig 1 - Yellow trace) until the power supply can provide enough current to meet the active power requirements. Because of this potential phenomenon, supply path inductances should be minimized and voltage drops should not exceed 50mV (duration must be < 20us), nor should they exceed 70mV (duration must be < 10us).

[Fig 1.] Voltage dip caused by inductive supply paths resulting in VDD/VDDQ current deficiencies.
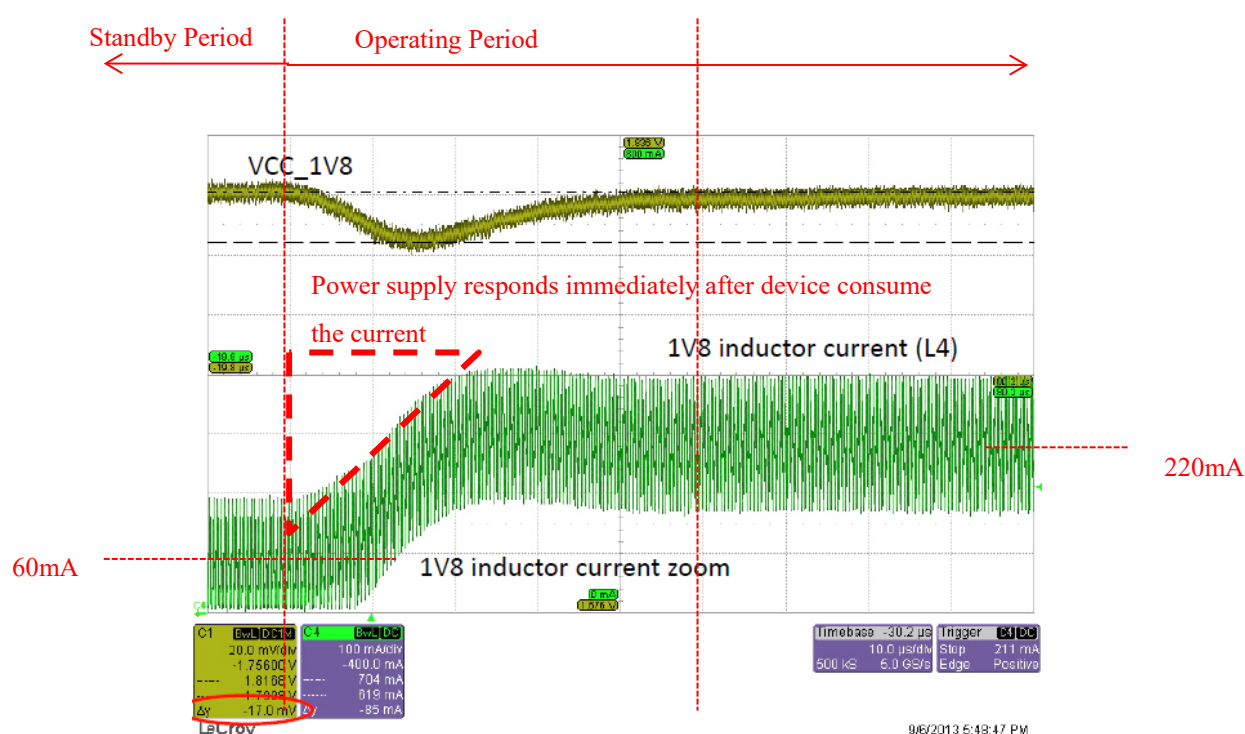
Power supply designs can also contribute to current deficiencies, if the response time of the supply is too slow to adjust to the dynamic needs of the power conditions. These dynamic conditions include the switching of the ODT function, refresh cycles, read cycles and write cycles. The following plot (Fig 2) illustrates that as the operating modes change, the power supply can't adjust its current source fast enough to satisfy the increased active power requirement. This produces a similar voltage drop to the inductive example (Fig 1) until the power supply senses the voltage deficiency and responds with additional current to support the active mode.

[Fig 2.] Voltage dip due to supply design causing the current deficiency.
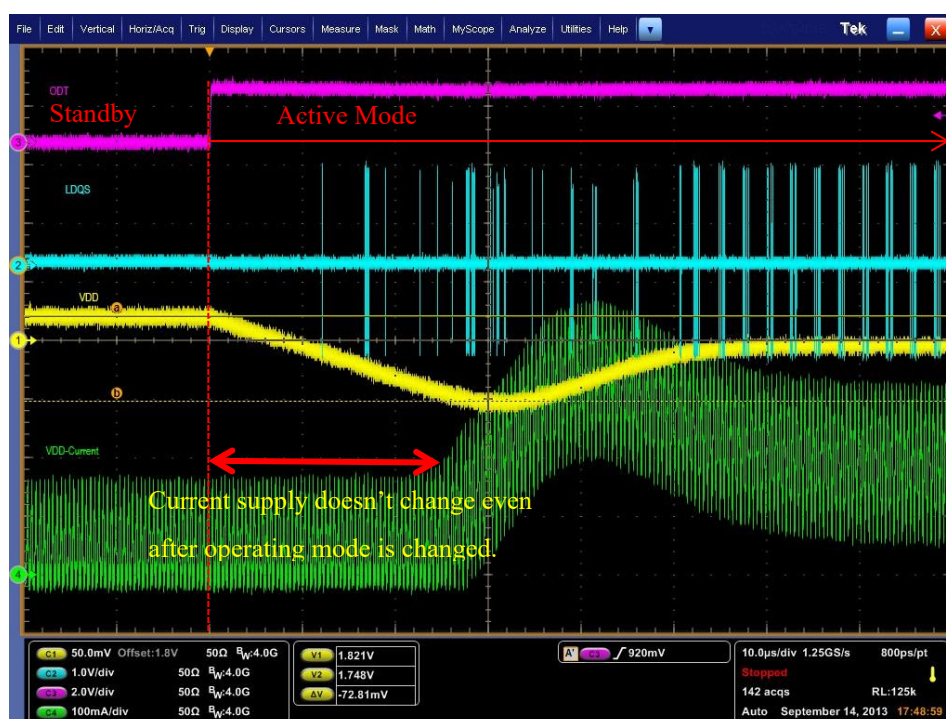
In Fig 3, a large capacitor is used to provide additional current when the operating mode is switched from standby to active mode. The additional current source (large capacitor) reduces the slope of the power supply voltage drop, but lengthens the reaction time of the supply to the increased active power requirements. While the additional capacitance provides a short term solution it does not resolve the overall power supply deficiency which requires further investigation.

[Fig 3.] Additional capacitance reduces the voltage dip but the supplies reaction time is slower.
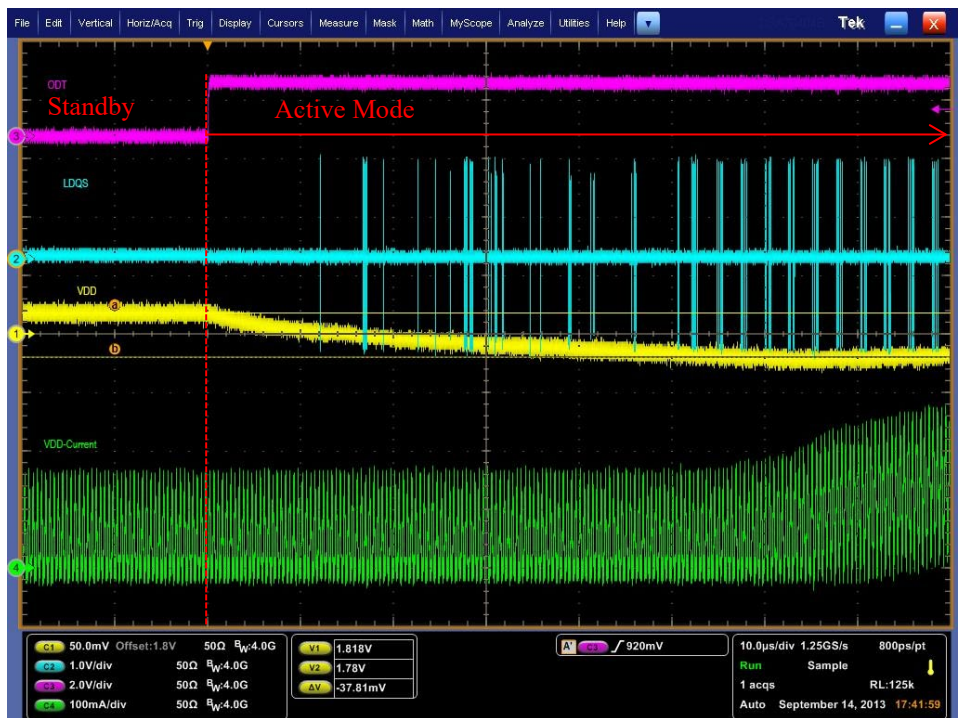
In the examples above, dynamic current deficiencies resulting from DDR2 operational mode changes can be reduced with optimal power supply selection, low inductance paths and careful selection decoupling capacitors to minimize the response times during peak current demand. In DDR2 applications, ISSI recommends that power supply dips should not exceed 50mV (duration must be less than 20us, nor should they exceed 70mV (duration must be less than 10us).

6. LAND pattern
Follow IPC-7351, keep size of land pattern to be equal to 80% of the ball size of BGA.

For any question, please contact the ISSI Application Team