MP18811

Isolated Single-Channel Gate Driver with Split Outputs

DESCRIPTION

The MP18811 is an isolated, single-channel gate driver solution with up to 4A of source and sink peak current capability. The gate driver is designed to drive power switching devices with a short propagation delay and minimal pulse-width distortion. By utilizing MPS's proprietary capacitive-based isolation technology, the driver can provide up to $3kV_{RMS}$ withstand voltage (per UL 1577). It can also provide a common-mode transient immunity (CMTI) rating above 100kV/µs between the input side and output driver. These advanced features enable high efficiency, high power density, and robustness in a wide variety of power applications.

The MP18811 provides primary on/off control and split outputs that can control source and sink driving capability individually. A wide primary-side VDDI supply voltage (V_{DDI}) range makes the driver suitable to be interfaced with 3.3V and 5V digital controllers. The secondary-side driver can accept up to a 30V supply. All of the supply voltage pins feature multiple under-voltage lockout (UVLO) protection options.

The MP18811 is available in an SOIC-8 NB (narrow-body) package.

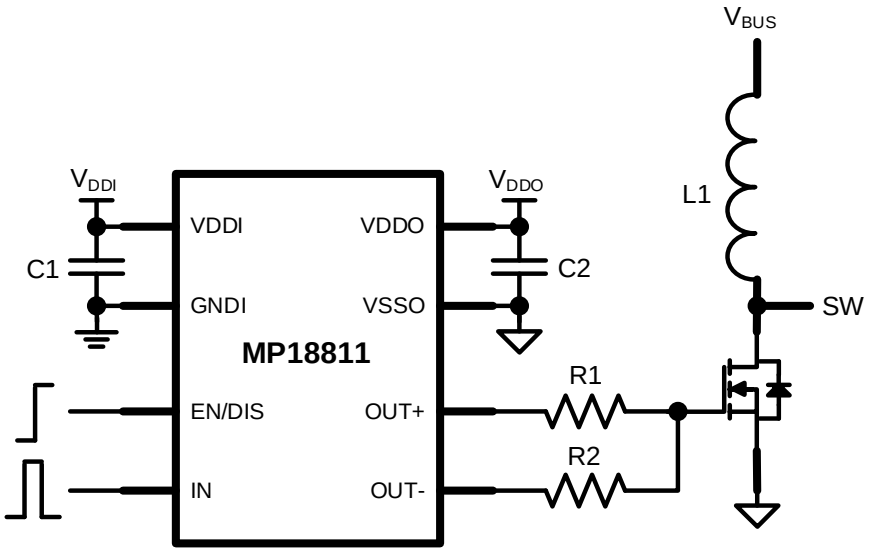
FEATURES

- Single-Channel Gate Driver
- Up to $3kV_{RMS}$ Input to Output Isolation
- Common-Mode Transient Immunity (CMTI) >100kV/µs
- 2.8V to 5.5V Input VDDI Voltage (V_{DDI}) Range to Interface with TTL and CMOS-Compatible Inputs
- Up to 30V Output Drive Supply with Several Under-Voltage Lockout (UVLO) Options
- 4A Source, 4A Sink Peak Current Output
- Primary On/Off Control
- Split Source and Sink Outputs
- 50ns Typical Propagation Delay
- -40°C to +125°C Operating Temperature Range
- UL 1577 Certified:
  - SOIC-8 NB: $3kV_{RMS}$ Isolation for 60s
- DIN EN IEC 60747-17 (VDE 0884-17): 2021-10 Certified
- TUV SUD Certification per IEC/EN/UL/CSA 62368-1, 60950-1, 61010-1
- CQC Certification per GB4943.1-2022

APPLICATIONS

- Half/Full-Bridge Converters
- Isolated DC/DC Converters
- Offline Isolated AC/DC Converters
- DC/AC Inverters

TYPICAL APPLICATION



SELECTION GUIDE

Part Number	Peak Output Current (A)	Output UVLO (V)	On/Off Logic	Input Logic	Configuration	Package Type
MP18811-4A	4	3	EN	IN	Single	SOIC-8 NB
MP18811-4B		5				
MP18811-4C		8				
MP18811-4D		10				
MP18811-4E		12				
MP18811-A4A	4	3	DIS	IN	Single	SOIC-8 NB
MP18811-A4B		5				
MP18811-A4C		8				
MP18811-A4D		10				
MP18811-A4E		12				

ORDERING INFORMATION (1)

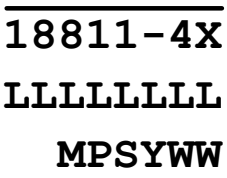
Part Number*	Package	Top Marking	MSL Rating
MP18811-4AGS	SOIC-8 NB	*See Below*	2
MP18811-4BGS			
MP18811-4CGS			
MP18811-4DGS			
MP18811-4EGS			
MP18811-A4AGS	SOIC-8 NB		
MP18811-A4BGS			
MP18811-A4CGS			
MP18811-A4DGS			
MP18811-A4EGS			

* For Tape & Reel, add suffix -Z (e.g. MP18811-4AGS-Z).

Note:

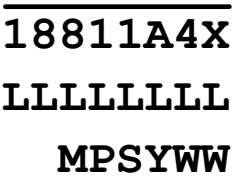
1) Contact MPS sales or our distributors to check the latest availability status for the ordering part numbers.

TOP MARKING (MP18811-4x)



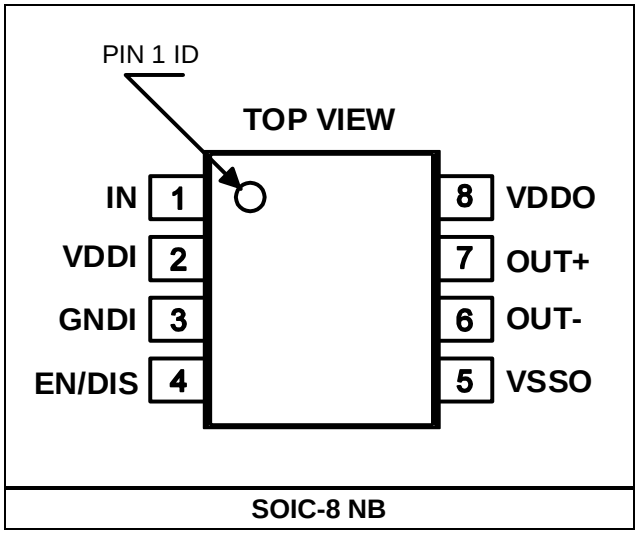
18811-4X: Part number
X: UVLO level code, where X = A, B, C, D, or E
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

TOP MARKING (MP18811-A4x)



18811A4X: Part number
X: UVLO level code, where X = A, B, C, D, or E
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE



SOIC-8 NB

PIN FUNCTIONS

Pin #	Name	Description
1	IN	**Non-inverting logic control signal input.** The IN pin can accept a TTL/CMOS level compatible input logic. This pin is pulled down internally to GNDI. A logic high signal on IN forces OUT+ to go high and OUT- into a high-impedance (Hi-Z) state. A logic low signal on IN or leaving the pin open forces OUT- low and OUT+ into a Hi-Z state.
2	VDDI	**Input-side power supply input.** The VDDI pin supplies power to the primary-side control circuitry. This pin is locally decoupled to GNDI using a low-ESR/ESL bypass capacitor. Place the capacitor as close to the chip as possible.
3	GNDI	**Input-side ground.** Reference ground for all input-side signal and internal control blocks.
4	EN/DIS	**Enable/disable control input.** The EN/DIS pin can be driven by an external TTL/CMOS level compatible input logic signal to enable/disable the chip. EN/DIS can be configured for the EN or DIS function. EN: The EN pin is pulled high internally. Pull EN high or leave it open to enable the chip; pull EN low to shut down the driver output and disable the chip. DIS: The DIS pin is pulled low internally. Pull DIS low or leave it open to enable the chip; pull DIS high to shut down the driver output and disable the chip.
5	VSSO	**Output-side ground.** Reference ground for the output driver.
6	OUT-	**Gate drive pull-down output.** Connect the OUT- pin to the gate of the power device. When IN asserts a logic low signal or the pin is left open, OUT- pulls down the gate of the power device to switch it off. Pulling IN high forces OUT- into a Hi-Z state.
7	OUT+	**Gate drive pull-up output.** Connect the OUT+ pin to the gate of the power device. When IN asserts a logic high signal, OUT+ drives the power device to switch it on. Pull IN low or leave the pin open to force OUT+ into a Hi-Z state.
8	VDDO	**Output-side driver power supply input.** The VDDO pin supplies power to the secondary-side driver circuitry. It is locally decoupled to VSSO using a low-ESR/ESL bypass capacitor. Place the capacitor as close to the chip as possible.

ABSOLUTE MAXIMUM RATINGS (2)

V_{DDI} - V_{GNDI} .....-0.3V to +6.5V
V_{IN}, $V_{EN/DIS}$.....
..... (V_{GNDI} - 0.3V) to (V_{DDI} + 0.3V)
V_{IN}, $V_{EN/DIS}$ transient for 50ns.....
..... (V_{GNDI} - 5V) to (V_{DDI} + 0.3V)
V_{DDO} - V_{SSO} .....-0.3V to +35V
V_{OUT+}, V_{OUT-} ..... (V_{SSO} - 0.3V) to (V_{DDO} +0.3V)
V_{OUT+}, V_{OUT-} transient for 200ns.....
..... (V_{SSO} - 2V) to (V_{DDO} + 0.3V)
Continuous power dissipation (T_A = 25°C) (3)
SOIC-8 NB 1130mW
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) 4000V
Charged-device model (CDM) 2000V

Recommended Operating Conditions (4)

V_{DDI} - V_{GNDI} .....2.8V to 5.5V
V_{IN}, $V_{EN/DIS}$ ..... V_{GNDI} to V_{DDI}
V_{DDO} - V_{SSO}.....
..... 4.2V to 30V (3V UVLO option)
..... 6.5V to 30V (5V UVLO option)
..... 9.2V to 30V (8V UVLO option)
..... 12V to 30V (10V UVLO option)
..... 14.5V to 30V (12V UVLO option)
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (5)	θ_{JA}	θ_{JC}
SOIC-8 NB	110	45	°C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on the MP18811 evaluation board, a 2-layer PCB.

ELECTRICAL CHARACTERISTICS

2.8V ≤ V_{DDI} - V_{GNDI} ≤ 5.5V, V_{DDO} - V_{SSO} = 5V/12V/15V (6), T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, all voltages with respect to the corresponding ground(s), unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input-Side Supply Voltage						
V_{DDI} under-voltage lockout (UVLO) threshold	V_{DDI_UVLO}	(V_{DDI} - V_{GNDI}) falling	2.42	2.6	2.78	V
V_{DDI} UVLO hysteresis	$V_{DDI\_UVLO\_HYS}$		100	120	140	mV
Input-Side Supply Current						
VDDI shutdown current	I_{VDDI_SD}	V_{EN} = V_{GNDI} or V_{DIS} = V_{DDI}		1	1.3	mA
VDDI quiescent current	I_{VDDI_Q}	V_{EN} = V_{DDI} or V_{DIS} = V_{GNDI}, V_{IN} = V_{GNDI}		1	1.3	mA
VDDI operating current	I_{VDDI}	f_{SW} = 500kHz, 50% duty, C_{LOAD} = 100pF		1.3	2	mA
Logic Input (IN, EN/DIS)						
Logic input high threshold	V_{LI_H}	(V_{LI} - V_{GNDI}) rising		1.6	1.8	V
Logic input low threshold	V_{LI_L}	(V_{LI} - V_{GNDI}) falling	1	1.2		V
Logic input hysteresis voltage	V_{LI_HYS}		360	400	440	mV
Internal pull-up resistance	R_{LI_PU}	EN		200		kΩ
Internal pull-down resistance	R_{LI_PD}	IN, DIS		200		kΩ
Output-Side Supply Voltage						
V_{DDO} UVLO threshold when (V_{DDO} - V_{SSO}) is falling	V_{DDO_UVLO}	-A, 3V threshold	2.7	3.2	3.7	V
		-B, 5V threshold	5	5.5	6	V
		-C, 8V threshold	7.5	8	8.5	V
		-D, 10V threshold	9.3	10	10.7	V
		-E, 12V threshold	11	12	13	V
VDDO UVLO hysteresis	$V_{DDO\_UVLO\_HYS}$	-A/-B, 3V/5V threshold	200	300	400	mV
		-C, 8V threshold	420	520	620	mV
		-D/-E, 10V/12V threshold	0.8	1	1.2	V
Output-Side Supply Current						
VDDO shutdown current	I_{VDDO_SD}	V_{EN} = V_{GNDI} or V_{DIS} = V_{DDI}		1	1.3	mA
VDDO quiescent current	I_{VDDO_Q}	V_{EN} = V_{DDI} or V_{DIS} = V_{GNDI}, V_{IN} = V_{GNDI}		1	1.3	mA
VDDO operating current	I_{VDDO}	f_{SW} = 500kHz, C_{LOAD} = 100pF, V_{DDO} - V_{SSO} = 12V		2.5	3	mA
		f_{SW} = 500kHz, C_{LOAD} = 100pF, V_{DDO} - V_{SSO} = 15V		3	4.6	mA
Gate Driver						
Logic high output voltage	V_{OUT+_H}	I_{OUT+} = -10mA	V_{DDO} - 0.03	V_{DDO} - 0.01		V
Logic low output voltage	V_{OUT-_L}	I_{OUT-} = 10mA		V_{SSO} + 0.01	V_{SSO} + 0.03	V
Peak output source current (7)	I_{OUT+_SRC}	V_{DDO} - V_{SSO} = 15V, V_{OUT+} - V_{SSO} = 5V (5V Miller plateau), f_{SW} = 1kHz		-4		A

ELECTRICAL CHARACTERISTICS *(continued)*

2.8V ≤ V_{DDI} - V_{GNDI} ≤ 5.5V, V_{DDO} -V_{SSO} = 5V/12V/15V (6), T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, all voltages with respect to the corresponding ground(s), unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Peak output sink current (7)	I_{OUT-_SNK}	V_{DDO} - V_{SSO} = 15V, V_{OUT-} - V_{SSO} = 5V (5V Miller plateau), f_{SW} = 1kHz		4		A
Output source resistance	R_{OUT+}	I_{OUT+} = -10mA		1.3	2.5	Ω
Output sink resistance	R_{OUT-}	I_{OUT-} = 10mA		1	2	Ω
Switching (8)						
Output rise time	t_R	(V_{OUT+} - V_{SSO}) rising, C_{LOAD} = 1.8nF		10	20	ns
Output fall time	t_F	(V_{OUT-} - V_{SSO}) falling C_{LOAD} = 1.8nF		10	20	ns
Minimum pulse width	t_{PW_MIN}	Output pulse off if shorter than t_{PW_MIN}, C_{LOAD} = 0pF		23	35	ns
Propagation delay from IN high to the output rising edge	t_{PDLH}	V_{EN} = V_{DDI} or V_{DIS} = V_{GNDI}, C_{LOAD} = 0pF	35	50	65	ns
Propagation delay from IN low to the output falling edge	t_{PDHL}	V_{EN} = V_{DDI} or V_{DIS} = V_{GNDI}, C_{LOAD} = 0pF	35	50	65	ns
Propagation delay from enable true to the output rising edge	t_{PDEN}	V_{IN} = V_{DDI}, C_{LOAD} = 0pF	35	50	65	ns
Propagation delay from disable true to the output falling edge	t_{PDDIS}	V_{IN} = V_{DDI}, C_{LOAD} = 0pF	35	50	65	ns
Pulse-width distortion |t_{PDLH} - t_{PDHL}|	t_{PWD}	C_{LOAD} = 0pF		1	6	ns
Start-up delay from the input supply exiting UVLO to the output rising edge	t_{STU_VDDI}	V_{EN} = V_{DDI} or V_{DIS} = V_{GNDI}, V_{IN} = V_{DDI}, C_{LOAD} = 0pF	15	25	35	µs
Shutdown delay from the input supply entering UVLO to the output falling edge (7)	t_{SHD_VDDI}	V_{EN} = V_{DDI} or V_{DIS} = V_{GNDI}, V_{IN} = V_{DDI}, C_{LOAD} = 0pF		500		ns
Start-up delay from the output supply exiting UVLO to the output rising edge	t_{STU_VDDO}	V_{EN} = V_{DDI} or V_{DIS} = V_{GNDI}, V_{IN} = V_{DDI}, C_{LOAD} = 0pF	10	20	30	µs
Shutdown delay from the output supply entering UVLO to the output falling edge (7)	t_{SHD_VDDO}	V_{EN} = V_{DDI} or V_{DIS} = V_{GNDI}, V_{IN} = V_{DDI}, C_{LOAD} = 0pF		500		ns
Static common-mode transient immunity (CMTI) (7)	$CMTI_{STC}$	V_{EN} = V_{DDI} or V_{DIS} = V_{GNDI}, V_{IN} = V_{GNDI} or V_{DDI}, slew rate of V_{GNDI} vs. V_{SSO}, V_{CM} = 1500V	100			kV/µs
Dynamic CMTI (7)	$CMTI_{DYN}$	V_{EN} = V_{DDI} or V_{DIS} = V_{GNDI}, f_{SW} = 100kHz pulse at IN, slew rate of V_{GNDI} vs. V_{SSO}, V_{CM} = 1500V	100			kV/µs

Notes:

6) For the test conditions, V_{DDO} - V_{SSO} = 5V is used for 3V UVLO devices; V_{DDO} - V_{SSO} = 12V is used for 5V and 8V UVLO devices; and V_{DDO} - V_{SSO} = 15V is used for 10V and 12V UVLO devices.
7) Guaranteed by characterization. Not tested in production.
8) For more details, see Figure 1, Figure 2, and Figure 3 on page 16, as well as Figure 4 on page 17.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Parameters	Symbol	Condition	SOIC-8 NB	Units
External air gap (clearance) (9)	CLR	Shortest pin-to-pin distance through the air between the primary and secondary sides	>4	mm
External tracking (creepage) (9)	CPG	Shortest pin-to-pin distance across the package surface between the primary and secondary sides	>4	mm
Distance through insulation	DTI	Internal clearance	>20	μm
Comparative tracking index	CTI	According to IEC60112	>600	V
Material group		According to IEC 60664-1	I	
Overvoltage category per IEC 60664-1		Rated mains voltages ≤ 150V_{RMS}	I-IV	
		Rated mains voltages ≤ 300V_{RMS}	I-III	
		Rated mains voltages ≤ 600V_{RMS}	I-II	
UL 1577, 5th Edition				
Recognized under UL 1577 Component Recognition Program, Single Protection. File number: E322138				
Dielectric withstand insulation voltage	V_{ISO}	V_{TEST} = V_{ISO} for t = 60s (qualification), V_{TEST} = 1.2 x V_{ISO} for t = 1s (100% production)	3000	V_{RMS}
DIN EN IEC 60747-17 (VDE 0884-17): 2021-10 (10)				
Certified according to DIN EN IEC 60747-17 (VDE 0884-17): 2021-10; EN IEC 60747-17:2020+AC: 2021. Certification number: 40055265				
Maximum repetitive peak isolation voltage	V_{IORM}	AC voltage (bipolar)	630	V_{PK}
Maximum working isolation voltage	V_{IOWM}	AC voltage (sine wave), time dependent dielectric breakdown (TDDB) test method	450	V_{RMS}
		DC voltage	630	V_{DC}
Maximum transient isolation voltage	V_{IOTM}	V_{TEST} = V_{IOTM} for t = 60s (qualification), V_{TEST} = 1.2 x V_{IOTM} for t = 1s (100% production)	4242	V_{PK}
Apparent charge (11) measuring voltage	$V_{PD(M)}$	Method b1, at routine test (100% production), $V_{PD(INI)}$ = 1.2 x V_{IOTM}, t_{INI} = 1s, $V_{PD(M)}$ = 1.875 x V_{IORM}, t_M = 1s, partial discharge < 5pC	1181	V_{PK}
Maximum surge isolation voltage (12)	V_{IOSM}	Tested per IEC 62368-1 with 1.2/50μs pulse, V_{TEST} = 1.3 x V_{IOSM} (qualification)	4000	V_{PK}
Barrier capacitance (13)	C_{IO}	f_{SW} = 1MHz	~1	pF
Insulation resistance (13)	R_{IO}	V_{IO} = 500V, T_A = 25°C	>10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	>10^{11}	Ω
		V_{IO} = 500V, T_A = T_S = 150°C	>10^9	Ω
Pollution degree		Per DIN VDE 0110 Table 1	2	
Climatic category			40/125/21	
IEC/EN/UL/CSA 62368-1, 60950-1, 61010-1				
TUV SUD certification conformity. Certificate number: SG PSB-IV-07941, SG PSB-OF-07050, SG PSB-MS-00361, U10 113824 0011 Rev. 00, B 113824 0010 Rev. 00. Basic insulation, altitude ≤ 5000m, 125°C thermal cycling test passed, 660V_P/630V_{RMS} maximum working voltage				

INSULATION AND SAFETY-RELATED SPECIFICATIONS *(continued)*

GB 4943.1-2022
Certified according to CQC GB 4943.1-2022. File number: CQC23001376765. Basic insulation, altitude ≤ 5000m, 125°C thermal cycling test passed, 660V_P/630V_{RMS} maximum working voltage

Notes:

9) See the Package Information on page 26 for detailed dimensions. As an isolated solution, the recommended land pattern is helpful to ensure adequate safety creepage and clearance distances on a PCB.
10) This coupler is suitable for “basic electrical insulation” only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
11) Electrical discharge caused by a partial discharge in the coupler.
12) The surge test is carried out in oil.
13) The barrier’s primary-side and secondary-side terminals are connected, forming a two-terminal device. C_{IO} and R_{IO} are measured between the two terminals of the coupler.

SAFETY LIMITING VALUES (14)

Parameters	Symbol	Condition	SOIC-8 NB	Units
Maximum safety temperature (15)	T_S		150	°C
Maximum output safety current	I_{S_O}	V_{DDO} - V_{SSO} = 12V (16), T_J = 150°C, T_A = 25°C	92	mA
		V_{DDO} - V_{SSO} = 30V, T_J = 150°C, T_A = 25°C	37	mA
Safety power dissipation (17)	P_S	Input side	15	mW
		Output side	1115	mW
		Total	1130	mW

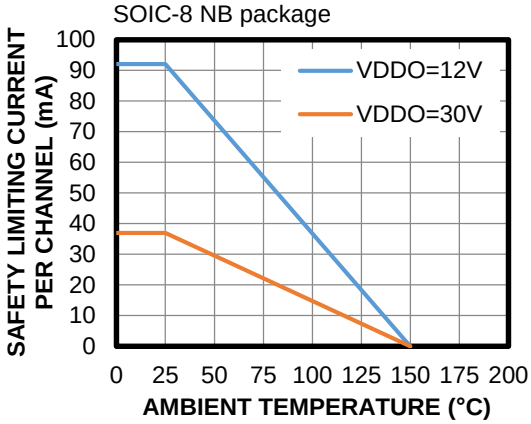
Notes:

14) Maximum value allowed in the event of a failure.
15) The maximum safety temperature (T_S) has the same value as the maximum junction temperature (T_J (MAX)) specified in the Absolute Maximum Ratings on page 6.
16) Tested for 5V and 8V UVLO devices.
17) Test conditions: V_{DDI} - V_{GNDI} = 5.5V, V_{DDO} - V_{SSO} = 30V, T_J = 150°C, T_A = 25°C. The safety power dissipation is a function of the maximum junction temperature (T_J (MAX)), the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A). This function can be calculated using the following equations:
$T_S = T_J (MAX) = T_A + (\theta_{JA} \times P_S)$
$P_S = I_S \times V_I$
Where V_I is the input voltage.

THERMAL DERATING CURVES FOR SAFETY LIMITING VALUES

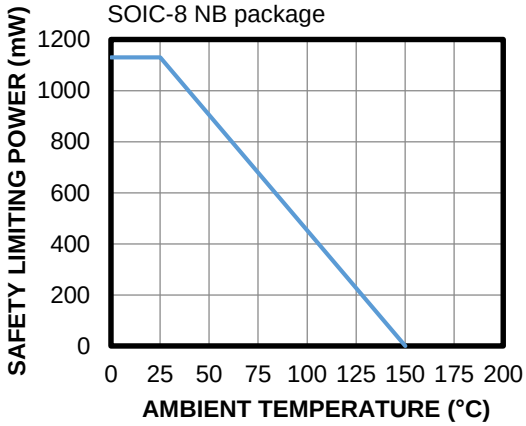
Thermal Derating Curve for Safety Limiting Current

SOIC-8 NB package



Thermal Derating Curve for Safety Limiting Power

SOIC-8 NB package

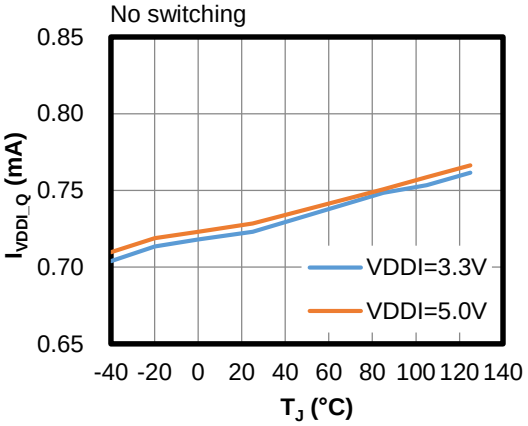


TYPICAL CHARACTERISTICS

V_{DDI} - V_{GNDI} = 5V, V_{DDO} - V_{SSO} = 12V, C_{LOAD} = 0pF, T_J = 25°C, all voltages with respect to the corresponding ground(s), unless otherwise noted.

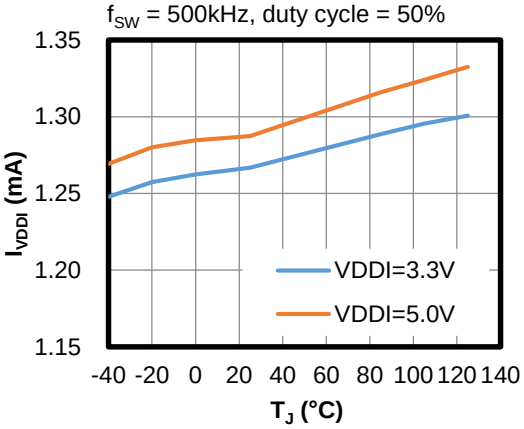
VDDI Quiescent Current vs. Junction Temperature

No switching



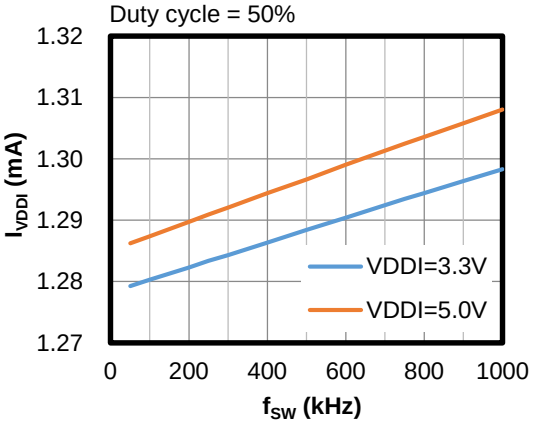
VDDI Operating Current vs. Junction Temperature

f_{SW} = 500kHz, duty cycle = 50%



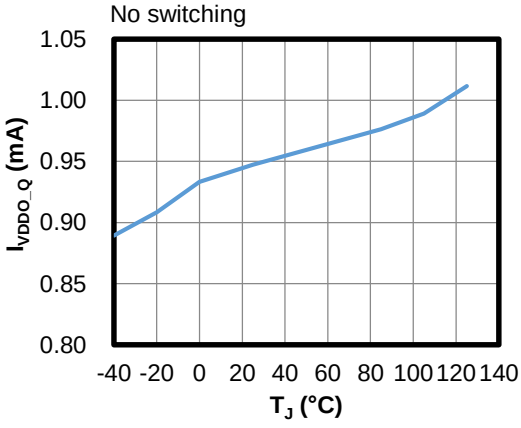
VDDI Operating Current vs. Switching Frequency

Duty cycle = 50%



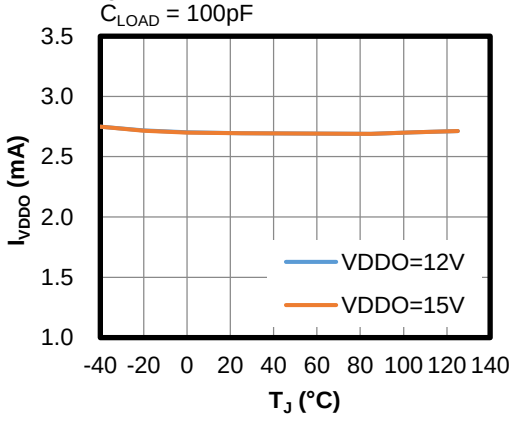
VDDO Quiescent Current vs. Junction Temperature

No switching



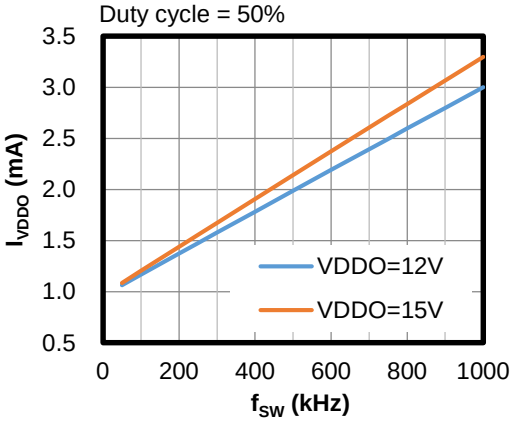
VDDO Operating Current vs. Junction Temperature

f_{SW} = 500kHz, duty cycle = 50%, C_{LOAD} = 100pF



VDDO Operating Current vs. Switching Frequency

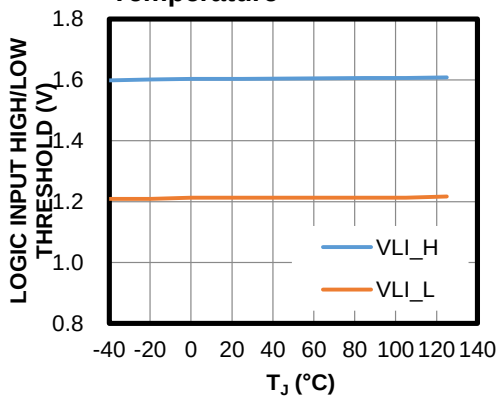
Duty cycle = 50%



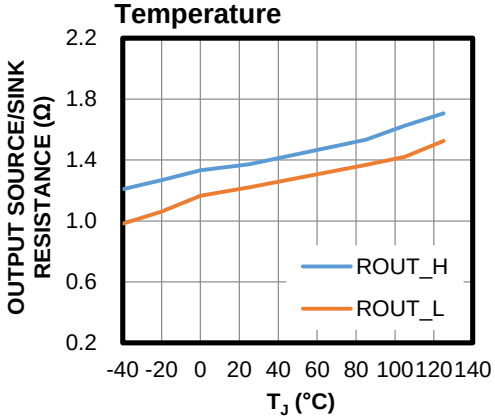
TYPICAL CHARACTERISTICS *(continued)*

V_{DDI} - V_{GNDI} = 5V, V_{DDO} - V_{SSO} = 12V, C_{LOAD} = 0pF, T_J = 25°C, all voltages with respect to the corresponding ground(s), unless otherwise noted.

Logic Input High/Low Threshold vs. Junction Temperature

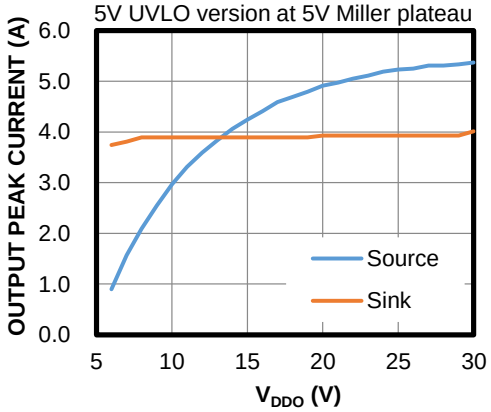


Output Source/Sink Resistance vs. Junction Temperature



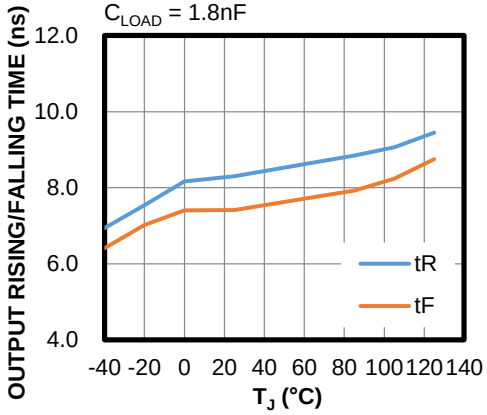
Output Peak Source/Sink Current vs. VDDO Supply Voltage

5V UVLO version at 5V Miller plateau

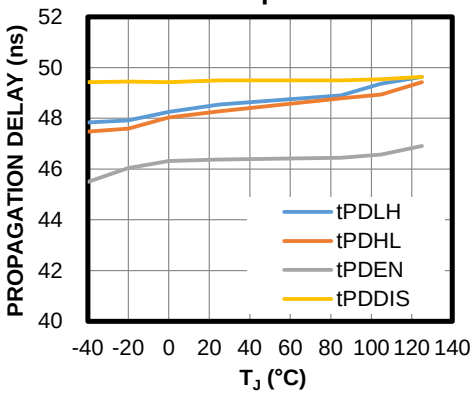


Output Rising/Falling Time vs. Junction Temperature

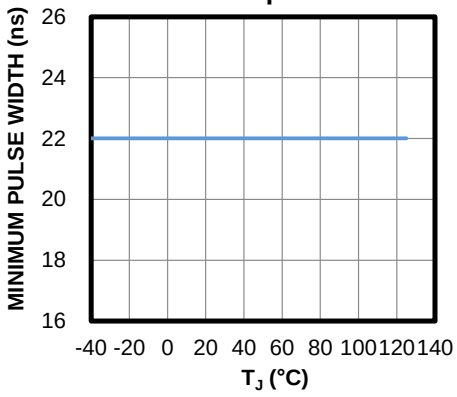
C_{LOAD} = 1.8nF



Propagation Delay vs. Junction Temperature



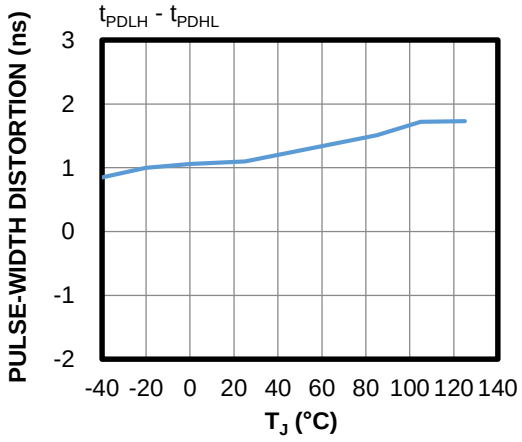
Minimum Pulse Width vs. Junction Temperature



TYPICAL CHARACTERISTICS *(continued)*

V_{DDI} - V_{GNDI} = 5V, V_{DDO} - V_{SSO} = 12V, C_{LOAD} = 0pF, T_J = 25°C, all voltages with respect to the corresponding ground(s), unless otherwise noted.

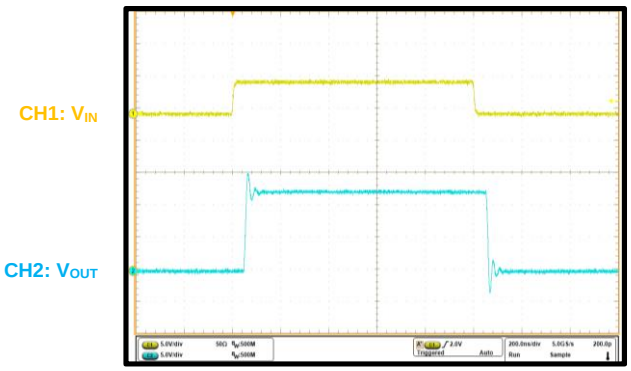
Pulse-Width Distortion vs. Junction Temperature



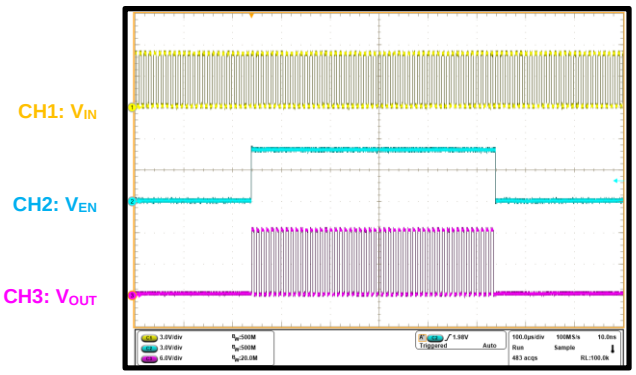
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board. V_{DDI} - V_{GNDI} = 5V, V_{DDO} - V_{SSO} = 12V, C_{LOAD} = 0pF, T_A = 25°C, all voltages with respect to the corresponding ground(s), unless otherwise noted.

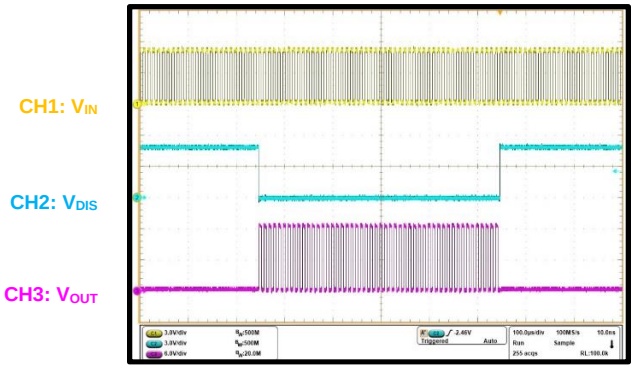
Typical Switching Waveforms



EN Control



DIS Control



DYNAMIC PARAMETERS DEFINITIONS

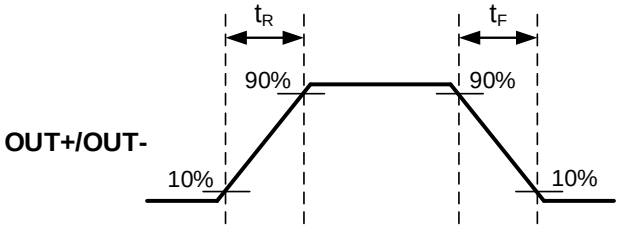


Figure 1: Output Rising and Falling Time

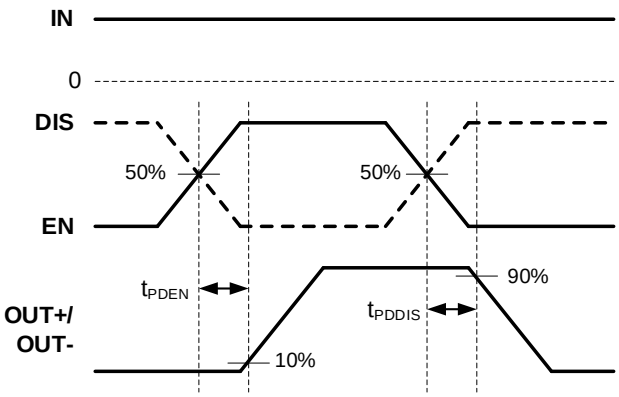


Figure 2: Enable/Disable Response Time

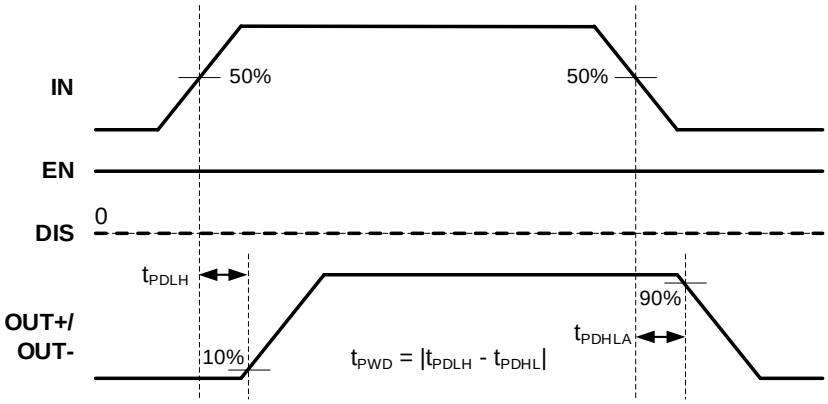


Figure 3: Propagation Delay from Input to Output

DEFINITIONS OF DYNAMIC PARAMETERS *(continued)*

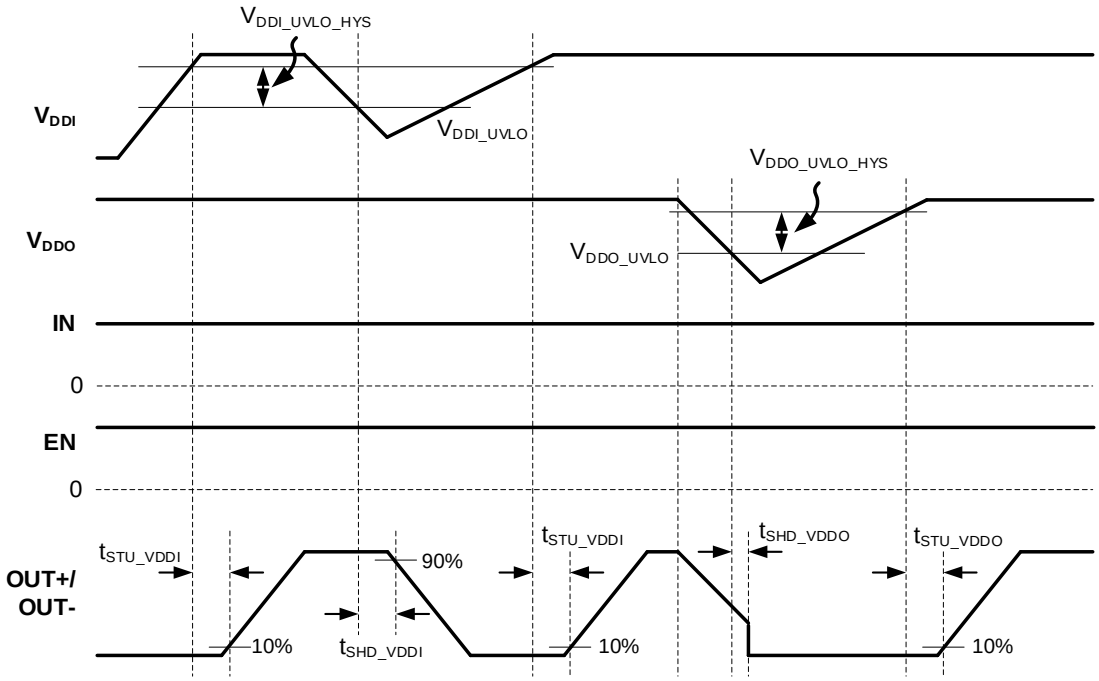


Figure 4: V_{DDI} and V_{DDO} Under-Voltage Lockout (UVLO)

DEVICE FUNCTIONAL MODES

Table 1: Logic Truth Table (18)

Inputs			Power Supply		Outputs		Notes
IN	EN	DIS	VDDI	VDDO	OUT+	OUT-	
H	H or O	L or O	P	P	H	Hi-Z	Normal operation
L or O	H or O	L or O	P	P	Hi-Z	L	
X	L	H	P	P	Hi-Z	L	The chip is disabled
X	X	X	UP	X	Hi-Z	L	VDDI is unpowered
X	X	X	P	UP	Hi-Z	L	VDDO is unpowered

Note:

18) L: Logic low, H: Logic high; O: Open; X: Not applicable, P: Powered, UP: Unpowered, UVLO condition.

FUNCTIONAL BLOCK DIAGRAMS

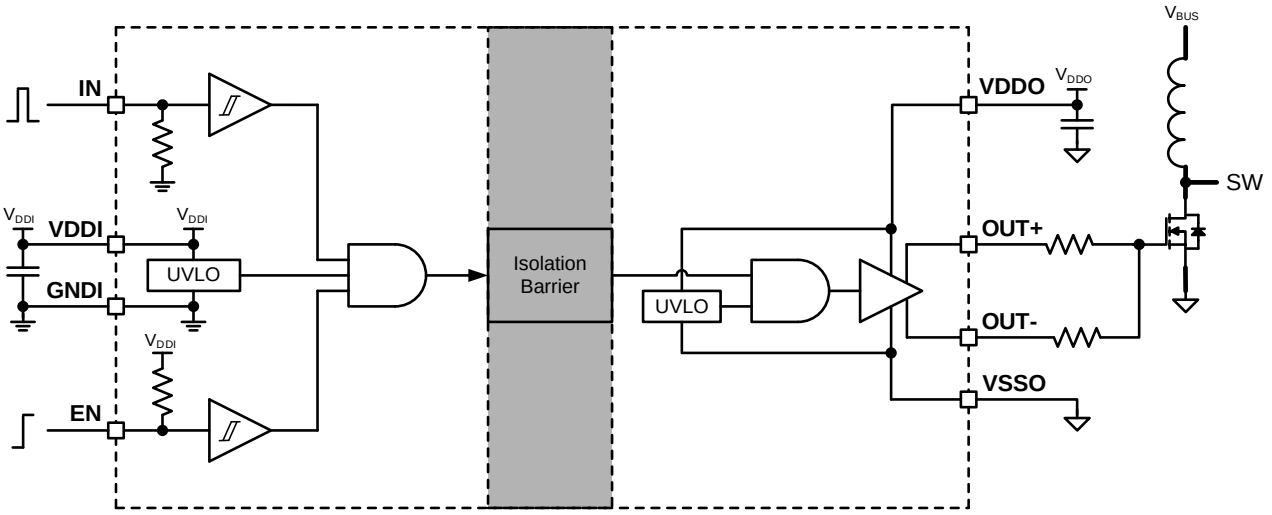


Figure 5: Functional Block Diagram (MP18811-4x, Enable Control Logic)

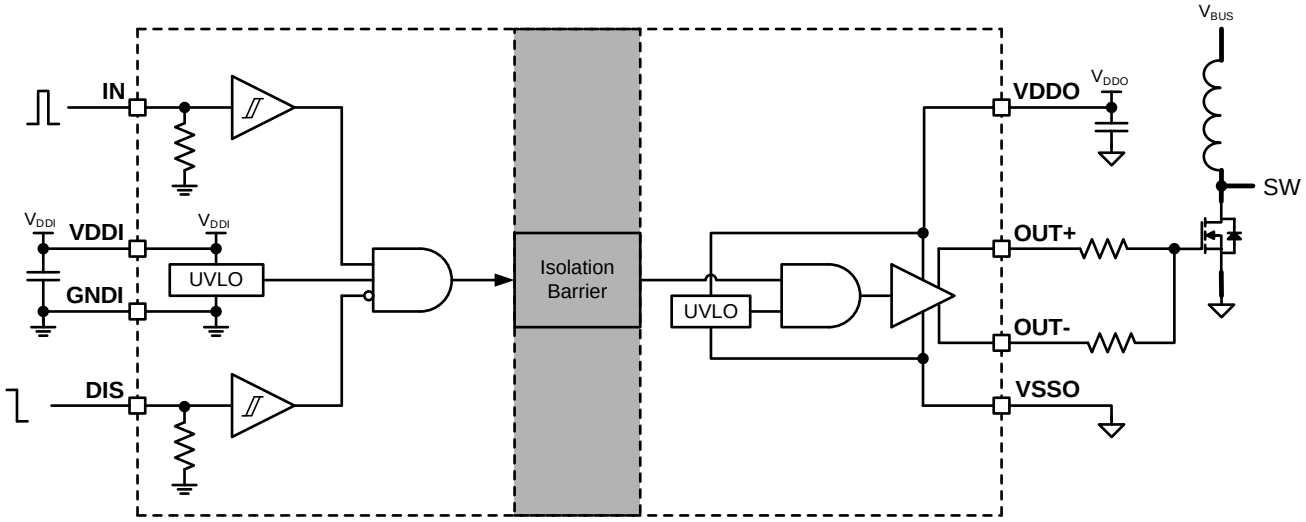


Figure 6: Functional Block Diagram (MP18811-A4x, Disable Control Logic)

OPERATION

The MP18811 is an isolated, single-channel gate driver solution with 4A peak output current capability. This IC is designed to drive power switching devices with a short propagation delay and minimal pulse-width distortion. These advanced features enable high efficiency, high power density, and robustness in a wide variety of power applications.

See Table 1 on page 18 for device functional modes.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to avoid the chip or certain blocks from operating at an insufficient supply voltage. The MP18811 incorporates internal UVLO comparators for all of the input and output supply circuit blocks to monitor the VDDI and VDDO voltages (V_{DDI} and V_{DDO}, respectively). Figure 4 shows the input and output supply UVLO time sequence diagram.

If the input bias voltage (V_{DDI}) is unpowered or below the UVLO threshold, the chip is not enabled, and the output stage does not receive the control signals from the input stage. UVLO holds the output low, regardless of the present logic levels of the input signals (including EN/DIS and IN).

If the output stage of the driver is unpowered or below the UVLO threshold, the driver's output is also pulled low. As long as the output is powered normally, the driver can accept the related control signal.

Input Stage and On/Off Control

All of the control input pins (EN/DIS and IN) accept a TTL/CMOS compatible logic input that is reliably isolated from each output. These control pins can easily be driven with common logic-level signals from a digital controller. However, any input signal applied to these control pins must never exceed the input stage supply (V_{DDI}). Therefore, it is recommended to connect VDDI to the same power supply as the control signal sources. The control logic for EN and IN is active high, while the control logic of DIS is active low.

If the IN input is left open, it is forced logic low via the internal pull-down resistor. This configuration ensures that the output remains low if the control input is not connected. It is recommended to connect the IN input to ground externally for better noise immunity and stable operation.

Similarly, for on/off control, the EN pin is connected to VDDI via the internal pull-up resistor, while the DIS pin is connected to GNDI via the internal pull-down resistor. Although leaving the EN/DIS pin floating allows the chip to operate normally after start-up, it is recommended to provide a stable external signal input for on/off control in real applications.

Output Stage

The MP18811's output stage is comprised of an upper P-channel MOSFET and a lower N-channel MOSFET (see Figure 7). The effective output pull-up source resistance (R_{OUT_H}) is the on resistance of the upper P-channel MOSFET, which delivers the large peak source current during the external power switch turn-on transition. The pull-down structure is an N-channel MOSFET, for which R_{OUT_L} is the output effective pull-down impedance when the device is driven low.

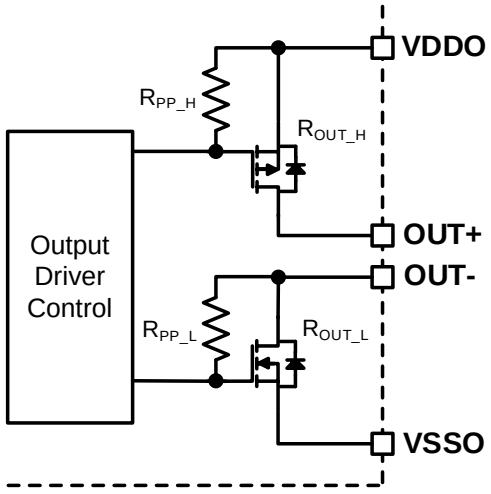


Figure 7: Output Stage with Active-Low Clamp Circuitry

The output stage is optimized to provide strong driving capacity to a power device during the Miller plateau interval of the on/off switching procedure.

The MP18811 is capable of delivering 4A peak source/sink current pulses. The rail-to-rail output ensures that the voltage switches between V_{DDO} and V_{SSO}, respectively.

Common-Mode Transient Immunity (CMTI)

Common-mode transient immunity (CMTI) is one of the key characteristics that determines an isolator's robustness, and is especially important in high-voltage applications that utilize devices with fast transient response (e.g. SiC/GaN FET). When a power device is switching, the high slew rate (dV/dt or dI/dt) transient noise can corrupt the signal transmission across the isolation barrier (see Figure 8 and Figure 9).

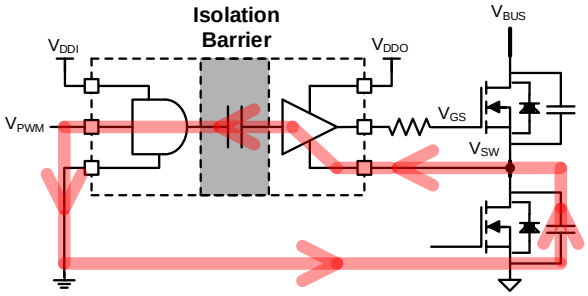


Figure 8: High Slew Rate Transient Noise Coupling Path

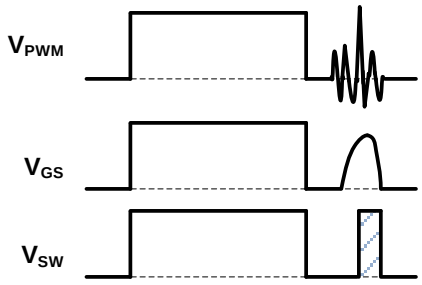


Figure 9: Abnormal Pulse Caused by Coupled Noise if dV/dt > CMTI

CMTI is defined as the maximum tolerable rate-of-rise (or fall) of a common-mode voltage applied between two isolated circuits, given in volts per second (V/ns or kV/µs). Below the maximum slew rate of a common-mode voltage, the isolator's output remains at the specified logic level and timing.

Figure 10 shows the CMTI test set-up to measure the CMTI of a coupler in both static and dynamic operation, under the specified common-mode pulse magnitude (V_{CM}), the specified slew rate for the common-mode pulse (dV_{CM}/dt), and other specified test or ambient conditions. The isolator's output must remain in the correct state while the pulse magnitude and slew rate meet the CMTI specifications.

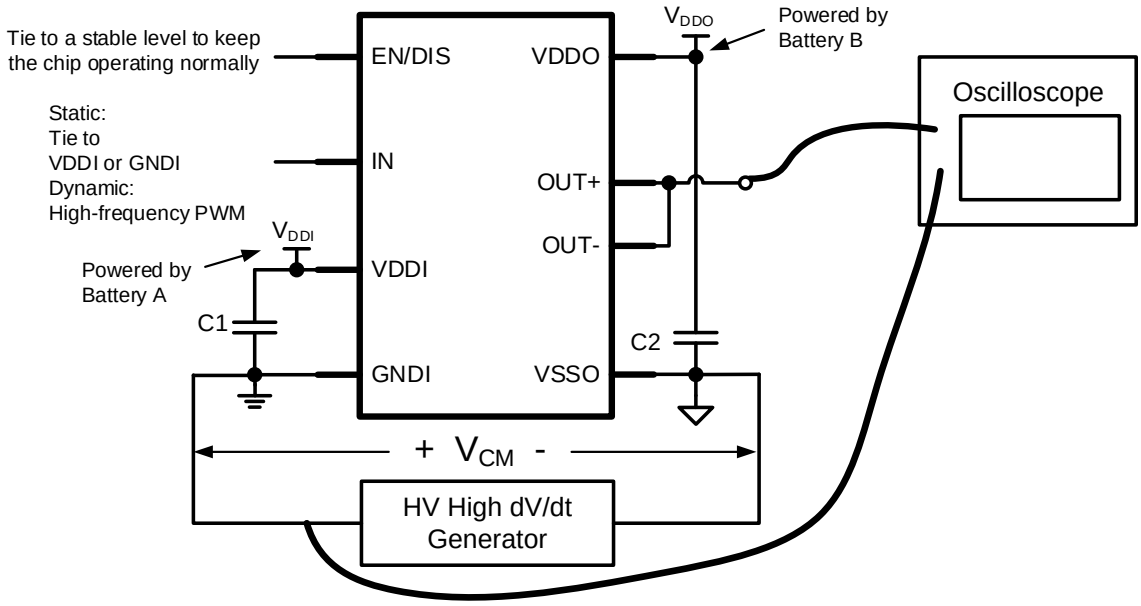


Figure 10: CMTI Test Set-Up

APPLICATION INFORMATION

Selecting the VDDI Capacitor

The VDDI capacitor reduces the surge current drawn from the input supply, and supports current consumption for the primary logic interface and transmitter block. Since the input side's operating current is only a few mA, a 100nF ceramic capacitor with X5R or X7R dielectrics is highly recommended because of its low ESR and small temperature coefficients. For most applications, if the real supply power is far away from the VDDI pin, then it is recommended to add a >1μF bypass capacitor in parallel with this 100nF ceramic capacitor.

Selecting the VDDO Capacitor

The VDDO capacitor is the bypass capacitor for the output gate driver. It supports current consumption for the driving control block, maintains a stable driving voltage, and supports up to 4A of transient source current.

Given that the allowable V_{DDO} voltage ripple is ΔV_{DDO}, and guarantees that the driver supply voltage cannot drop close to the UVLO threshold, the minimum VDDO capacitance (C_{VDDO}) can be calculated with Equation (1):

$$C_{VDDO} = \frac{I_{VDDO} \times \frac{1}{f_{SW}} + Q_G}{\Delta V_{DDO}} \quad (1)$$

Where I_{VDDO} is the VDDO operating current, f_{SW} is the switching frequency, and Q_G is the power device's gate charge.

Keep in mind that the loop resistance, voltage drop, and DC bias voltage ripple impact the supply voltage. A 10μF ceramic capacitor is typically selected. It is also recommended to place a secondary, high-frequency, 100nF bypass capacitor in parallel.

Selecting the Input Filter for IN

The IN input filter is not necessary in theory because the low-pass filter slows the PWM signal's rising/falling edge and affects the propagation delay. However, if there is significant high-frequency ringing introduced by the PCB traces, it is recommended to add a simple RC filter at the input, close to the IN pin.

To avoid increasing the input resistance, a resistor below 100Ω is typically recommended. When selecting the filter capacitor, ensure that the filter's cutoff frequency is at least ten times greater than f_{SW}, where a capacitance of dozens of pF is typically sufficient.

Selecting the External Driving Resistor

The external driving resistor can be applied to limit the ringing noise on the driving signal and adjust the switching speed to improve EMI performance. However, a higher driving resistance increases the switching losses, reduces system efficiency, and can introduce thermal issues.

The MP18811 provides split outputs that can control source and sink driving capability individually. Connect the source/sink resistor with OUT+ and OUT- ,respectively, and connect the other end of the resistors together using the device's gate.

The peak driving current can be used to evaluate the effect of the driving resistors. Without a driving resistor, the MP18811 can drive up to 4A of peak source and sink currents.

Considering the driving resistor, the peak source driving current for output (I_{OUT_SRC}) can be calculated with Equation (2):

$$I_{OUT\_SRC} = \frac{V_{DDO}}{R_{OUT\_H} + R_{G\_SRC} + R_{G(INT)}} \quad (2)$$

The peak sink driving current for output (I_{OUT_SNK}) can be calculated with Equation (3):

$$I_{OUT\_SNK} = \frac{V_{GS\_ON}}{R_{OUT\_L} + R_{G\_SNK} + R_{G(INT)}} \quad (3)$$

Where R_{G_SRC} is the external source resistor, R_{G_SNK} is the external sink resistor, $R_{G(INT)}$ is the power device's internal gate resistance, and V_{GS_ON} is the power device's stable gate-source voltage during the turn-on interval.

V_{GS_ON} should typically be close to V_{DDO}.

Since the driving current cannot exceed 4A, set the actual peak driving current to be the smaller value between the estimated I_{OUT_SRC} or I_{OUT_SNK} and 4A.

Estimated Gate Driver Power Loss

The total gate driver power loss is used to estimate the thermal performance. The MP18811 must operate under the safety limiting values (see the Safety Limiting Values section on page 10 for more details).

To estimate the gate driver power loss, first calculate the chip's operating power consumption (P_{OP}) with Equation (4):

$$P_{OP} = V_{DDI} \times I_{VDDI} + V_{DDO} \times I_{VDDO} \quad (4)$$

The gate driver's self-power consumption is related to f_{SW} and the supply voltage. For the relationship reference between the input and output channel's current consumption vs. the operating frequency, see the Typical Characteristics section on page 12.

Next, consider the gate driver power loss during switching operation. As a conventional totem-pole (TP) gate driver, the MP18811 charges and discharges the power device's gate capacitance once during every switching cycle. During the charging and the discharging period, the total energy is supplied by VDDO. If there is no external gate driver resistor, the power dissipation (P_{SW}) can be calculated with Equation (5):

$$P_{SW} = V_{DDO} \times \int_0^{t_{ON}} I_G(t)dt \times f_{SW} = V_{DDO} \times Q_G \times f_{SW} \quad (5)$$

Where t_{ON} is the turn-on time, and $I_G(t)$ is the driving current.

The behavior of the external source/sink resistors adds complexity to the dynamic power dissipation estimation.

If the driving current is not saturated to 4A within one switching cycle with external gate resistors, then P_{SW} is shared between the gate driver's internal source and sink resistances and the external gate driver resistors, based on the ratio of these series resistances. In this circumstance, P_{SW} can be calculated with Equation (6):

$$P_{SW} = \frac{V_{DDO} \times Q_G \times f_{SW}}{2} \times \left(\frac{R_{OUT\_H}}{R_{OUT\_H} + R_{G\_SRC} + R_{G(INT)}} + \frac{R_{OUT\_L}}{R_{OUT\_L} + R_{G\_SNK} + R_{G(INT)}} \right) \quad (6)$$

In some conditions, the MP18811 outputs the saturated 4A current at the beginning of the turn-on/off interval. During this saturation time, the power loss (P_{SW_SAT}) can be calculated with Equation (7):

$$P_{SW\_SAT} = 4A \times \int_0^{t_{ON\_SAT}} \left(V_{DDO} - V_{GS}(t)\right)dt + 4A \times \int_0^{t_{OFF\_SAT}} V_{GS}(t)dt \quad (7)$$

Where t_{ON_SAT/OFF_SAT} is the turn-on/off time with a saturated 4A current output, and $V_{GS}(t)$ is the power device's gate voltage during this saturation time.

The actual power loss is the sum of Equation (4) and Equation (5). Therefore, the total power loss dissipated in the MP18811 (P_{LOSS}) can be calculated with Equation (8):

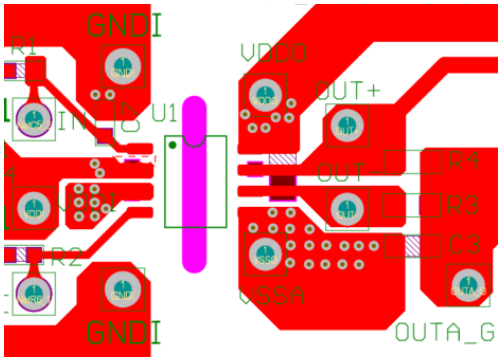
$$P_{LOSS} = P_{OP} + P_{SW} \quad (8)$$

Multiply P_{LOSS} by the junction-to-ambient thermal resistance (θ_{JA}) to determine the junction temperature rise above the ambient temperature. Ensure that the junction temperature (T_J) is below the maximum safety temperature (T_S).

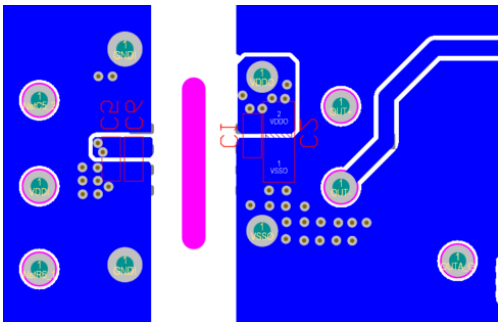
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 11 and follow the guidelines below:

1. Place the bypass/decoupling capacitors as close as possible to the VDDI and VDDO supply pins and the corresponding grounds. For each supply pin, it is recommended to add a low-ESR/ESL, high-frequency, 100nF bypass capacitor.
2. If an input RC filter is used, it is recommended to place this filter close to the corresponding control pin.
3. Place the high-current paths (e.g. the supply path, drive path, and the connection between the external power device source and the VSSO pin) very close to the driver chip with short, direct, and wide traces to minimize the parasitic inductance and avoid large transients and ringing noise.
4. It is strongly recommended to place large power and ground planes (or multiple ground layers) to help dissipate heat from the gate driver chip to the PCB and improve the thermal performance. Be careful when splitting the traces or coppers to allow sufficient insulation distance between the different low-/high-voltage planes.
5. Keep the driving loop from OUT+/OUT- to the power device's gate-to-source to VSSO short and with minimal area. Avoid placing the driving trace across different PCB layers through vias, as it can introduce parasitic inductance. Place the driver IC as close as possible to the power device.
6. Use the recommended land pattern design for each package type to ensure adequate insulation space between the primary and secondary sides. Avoid placing any components, tracks, or copper below the chip's body in any PCB layer.
7. A board cutout under the chip is recommended to extend the creepage distance on the PCB surface.



Top Layer



Bottom Layer

Figure 11: Recommended PCB Layout (19)

Note:

19) This example uses a 2-layer PCB layout.

TYPICAL APPLICATION CIRCUIT

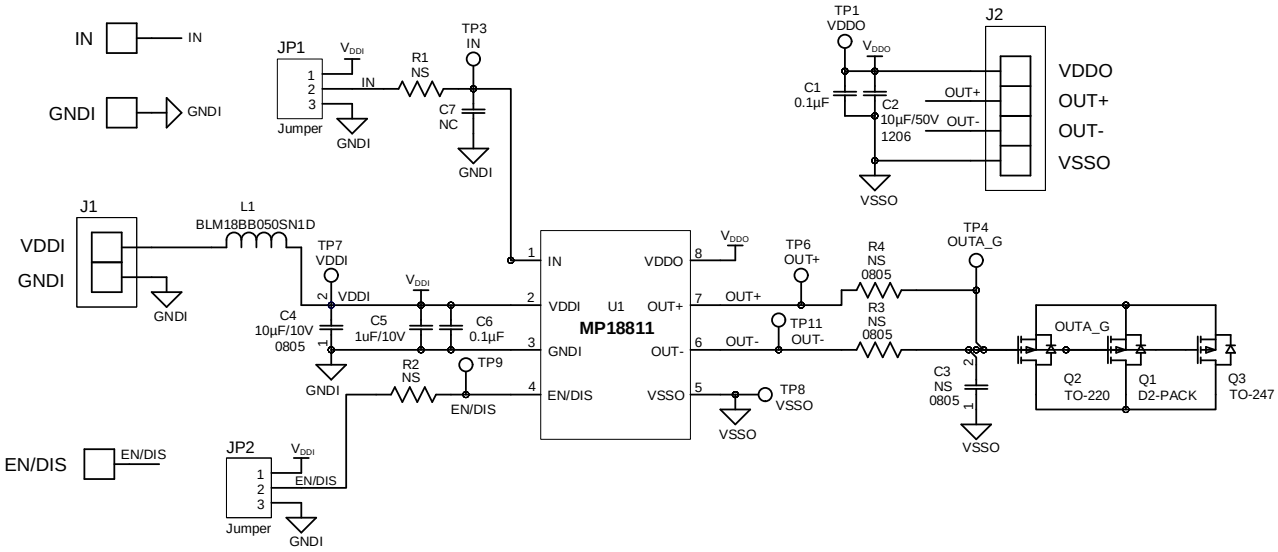
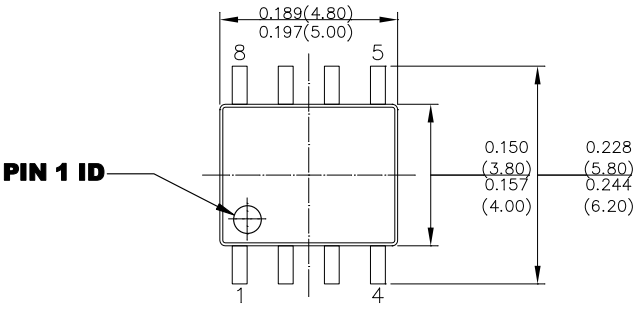


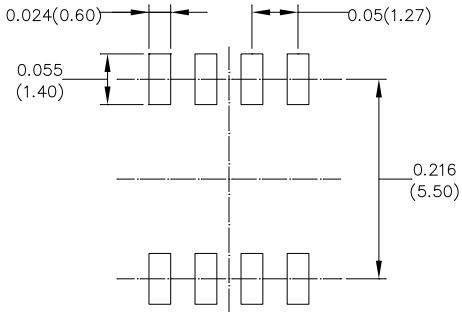
Figure 12: Typical Application Circuit

PACKAGE INFORMATION

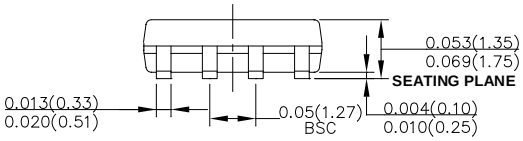
SOIC-8 NB (HV ISOLATION)



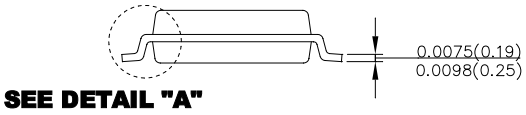
TOP VIEW



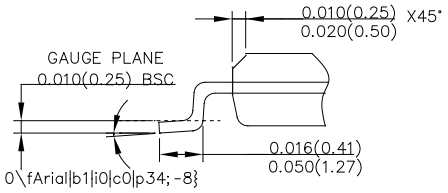
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

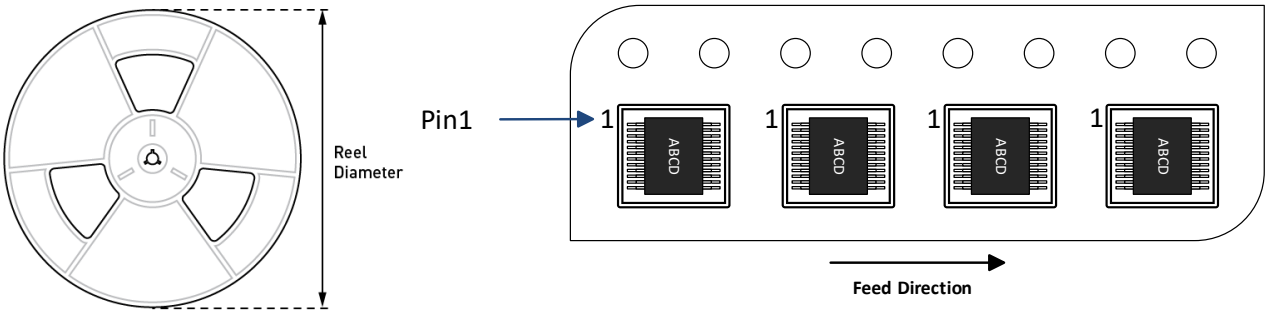


DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING REFERENCE TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP18811-4AGS	SOIC-8 NB	2500	100	13in	12mm	8mm
MP18811-4BGS						
MP18811-4CGS						
MP18811-4DGS						
MP18811-4EGS						
MP18811-A4AGS	SOIC-8 NB	2500	100	13in	12mm	8mm
MP18811-A4BGS						
MP18811-A4CGS						
MP18811-A4DGS						
MP18811-A4EGS						

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/21/2023	Initial Release	-