MP27931

5kV$_{RMS}$ Quad Channels Digital Isolator
Channel Direction: 3 Forward 1 Reverse

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MP27931 is a high performance four-channel digital isolator designed for robust applications. This device can survive a 5000V$_{RMS}$ isolation rating per UL 1577. This device is optimized for replacing opto-couplers and can support a high data rate of up to 150Mbps. This product can maintain its performance over a wide temperature range while minimizing power consumption.

The MP27931 uses capacitive isolation technology, to support up to 5kVrms insulation voltage rating. This device includes safety-related certifications according to UL 1577, VDE, CSA, as well as CQC. This isolator provides small size, low-power-consumption and higher reliability operation compared to traditional opto-coupler isolator.

This device provides schmitt trigger input and isolated encoding/decoding for high electromagnetic immunity in noisy environments. High/Low selectable fail-safe output supports fixed output even if the input signal power fails. This product is part of a family of quad channel digital isolators which can have 2-4 forward channels and 0-2 reverse channels for a total of four channels.

The MP27931 is available in a wide-body SOIC-16 WB package.

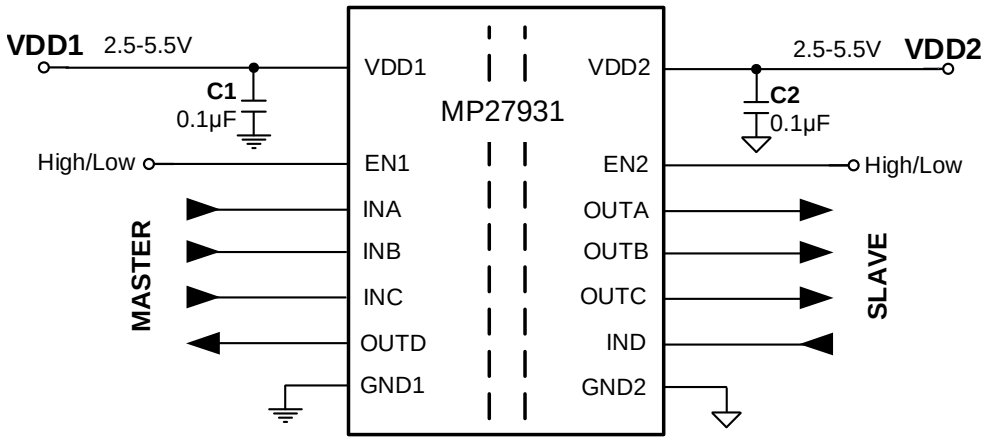
FEATURES

- Channel Direction: 3 Forward 1 Reverse
- 5kV$_{RMS}$ Isolation Voltage
- Support DC to 150Mbps Data Rate
- 2.5V to 5.5V Operation Range
- >±100kV/μs Common-mode Transient Immunity (CMTI)
- High System Level ESD, EFT, Surge Immunity Performance
- 13ns Propagation Delay for 5V Operation
- Ultra Low Power Supply Current
- Default Output Logic High (MP27931) and Low (MP27931-L) Options
- Tri-state Outputs with EN Control
- 1.2kV Peak V$_{IORM}$ Working Insulation
- Wide Temperature Range: -40°C to +125°C
- Available in SOIC-16 WB Package
- UL 1577 recognized
  - SOIC-16 WB Up to 5000 V$_{RMS}$ for 1 minute
- CSA Component Notice 5A Approval
- DIN EN IEC 60747-17 (VDE 0884-17): 2021-10 Certified (In Progress)
  - SOIC-16 WB: 7071 V$_{PK}$ Isolation
- CQC Certification per GB4943.1-2011 (In Progress)

APPLICATIONS

- Industrial Automation
- Isolated ADC/DAC
- Motor Controller and Driver
- Solar Inverters
- Isolated switch mode supplies
- Medical Equipment

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Output Default	Package	Top Marking	MSL Rating
MP27931GY	HIGH	SOIC-16 WB	*See Below*	TBD
MP27931-LGY	LOW			

* For Tape & Reel, add suffix -Z (e.g. MP27931GY-Z).

TOP MARKING

MP27931GY (SOIC-16 WB, Default HIGH)

MPSYYWW
MP27931
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP27931: Part number
LLLLLLLLL: Lot number

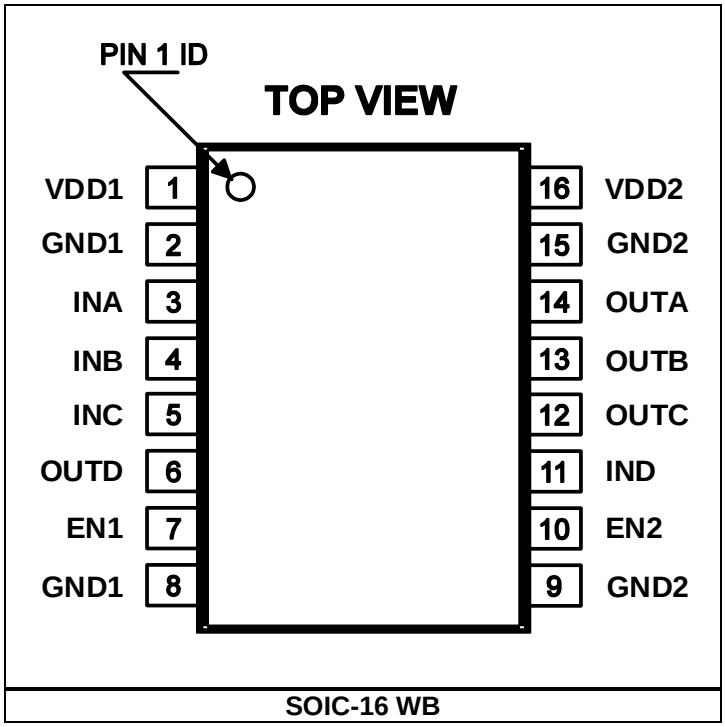
TOP MARKING

MP27931-LGY (SOIC-16 WB, Default LOW)

MPS YYWW
MP27931-L
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP27931-L: Part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE



SOIC-16 WB

PIN FUNCTIONS

Pin #	Name	Description
1	VDD1	**Side 1 power supply pin.** It is recommended to connect a 0.1μF decoupling capacitor between this pin and GND1 (pin2).
2, 8	GND1	**Side 1 ground pin.**
3	INA	**Channel A input pin.**
4	INB	**Channel B input pin.**
5	INC	**Channel C input pin.**
6	OUTD	**Channel D output pin.**
7	EN1	**Side 1 Output Port Enable Pin.** Active High, internal pulled up in default. It is recommended that the enable inputs be connected to an external logic high or low level when the IC is operating in noisy environments. To minimize noise coupling, do not connect circuit traces to EN1 or EN2 if they are left floating.
9, 15	GND2	**Side 2 ground pin.**
10	EN2	**Side 2 Output Port Enable Pin.** Active High, internal pulled up in default. It is recommended that the enable inputs be connected to an external logic high or low level when the IC is operating in noisy environments. To minimize noise coupling, do not connect circuit traces to EN1 or EN2 if they are left floating.
11	IND	**Channel D input pin.**
12	OUTC	**Channel C output pin.**
13	OUTB	**Channel B output pin.**
14	OUTA	**Channel A output pin.**
16	VDD2	**Side 2 power supply pin.** It is recommended to connect a 0.1μF decoupling capacitor between this pin and GND2 (pin15).

ABSOLUTE MAXIMUM RATINGS (1)

VDD1 to GND1, VDD2 to GND2 ..... -0.3V to +6.5V
Side 1 other pins to GND1 ..... -0.3V to VDD1+0.3V(2)
Side 2 other pins to GND2 ..... -0.3V to VDD2+0.3V(2)
Average output current per pin ..... -10mA to 10mA
Continuous power dissipation (T_A = +25°C) (3)
SOIC-16 WB ..... TBDW(5)
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±6000V
Charged device model (CDM) ..... ±2000V
Isolation barrier withstand with HBM ..... ±8000V

Recommended Operating Conditions (4)

Supply voltage V_{DD1}, V_{DD2} ..... 2.5V to 5.5V
Maximum signal data rate ..... DC to 150Mbps
Operating junction temp. (T_J) ... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

SOIC-16 WB		
EV27931-Y-00A(5)	TBD	TBD °C/W
JESD51-7(6)	TBD	TBD °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Maximum Voltage must not exceed 7.5V.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on EV27931-Y-00A, 2-layer, 63mm x 63mm PCB.
6) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{DD1} = V_{DD2} = 5V, T_J = -40°C to 125°C[7], typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Switching Timing Characteristics						
Minimum Pulse Width					5	ns
Propagation Delay[8]	t_{PLH}, t_{PHL}			13		ns
Pulse Width Distortion	PWD	$\|t_{PLH}- t_{PHL}\|$		1.5	4.5	ns
Propagation Delay Skew [9]	$t_{PSK(P-P)}$				4.5	ns
Channel-Channel Skew	t_{PS}	For both co-directional and opposing direction		0.8	2.5	ns
Output Rise/Fall Time[8]	t_r, t_f	C_L=15pF		2.5	5	ns
Peak Eye Diagram Jitter[10]	$t_{JIT(PK)}$			1.5		ns
Enable to Data Valid[11]	t_{EN-ON}			60	90	ns
Enable to Data Tri-State[11]	t_{EN-OFF}			50	75	ns
Input Power Fail to Valid Default Output	t_{SD}			500		ns
Start-up Time	t_{START}	From VDD1/VDD2 on to output valid		75		µs
Common-mode Transient Immunity[10]	CMTI	IN=0V or VDD, V_{CM} = 1.5kV	±100			kV/µs
Power Supply Range						
Supply Voltage Range	V_{DD1}		2.5		5.5	V
	V_{DD2}		2.5		5.5	V
Under Voltage Lockout Threshold	$V_{UVLO1-R}$	V_{DD1} Rising		2.25		V
	$V_{UVLO2-R}$	V_{DD2} Rising		2.25		V
Under Voltage Lockout Threshold Hysteresis	V_{UVHYS1}	V_{DD1}		200		mV
	V_{UVHYS2}	V_{DD2}		200		mV
Pin Input / Output Logic Threshold						
Input Voltage High Threshold	V_{ITH-H}	INx, ENx pins			2	V
Input Voltage Low Threshold	V_{ITH-L}		0.8			V
Input Threshold Hysteresis	$V_{ITH-HYS}$			350		mV
Pin Input Current Leakage		Connect INx to VDDx or GNDx			±10	µA
Pin Input Current Leakage		Test ENx pins, ENx =0V	-10	-5		µA
Output High Voltage	V_{OH}	OUTx pins. IOUT=-4mA	V_{DDx}-0.4	V_{DDx}-0.2		V
Output Low Voltage	V_{OL}	OUTx pins. IOUT=4mA		0.2	0.4	V
Tristate (high-impedance) Output Leakage Current		Connect OUTx to VDDx or GNDx, ENx = GNDx.			±10	µA
Output Impedance[12]	Z_O	OUTx pins		50		Ω
Thermal Protection						
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			20		°C

ELECTRICAL CHARACTERISTICS *(continued)*

V_{DD1} = V_{DD2} = 5V, T_J = -40°C to 125°C(7), typical values are tested at T_J = 25°C, unless otherwise noted.

Part Number	Parameter	Condition	Min	Typ	Max	Units
Power Supply Current						
DC Supply Current (*INx = 0V or VDD****)***						
MP27931	VDD1 Current	INx = VDD		2.5	3.8	mA
		INx = 0		7.9	11.9	mA
	VDD2 Current	INx = VDD		3.5	5.3	mA
		INx = 0		5.3	8.0	mA
MP27931-L	VDD1 Current	INx = VDD		7.9	11.9	mA
		INx = 0		2.5	3.8	mA
	VDD2 Current	INx = VDD		5.3	8.0	mA
		INx = 0		3.5	5.3	mA
1Mbps Supply Current (*INx = 500kHz Square Wave, C_{LOAD} = 15 pF on All Outputs****)***						
MP27931 MP27931-L	VDD1 Current			5.3	7.9	mA
	VDD2 Current			4.6	6.8	mA
10Mbps Supply Current (*INx = 5MHz Square Wave, C_{LOAD} = 15 pF on All Outputs****)***						
MP27931 MP27931-L	VDD1 Current			5.7	8.6	mA
	VDD2 Current			5.9	8.9	mA
100Mbps Supply Current (*INx = 50MHz Square Wave, C_{LOAD} = 15 pF on All Outputs****)***						
MP27931 MP27931-L	VDD1 Current			10.2	15.3	mA
	VDD2 Current			19.4	29.1	mA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{DD1} = V_{DD2} = 3.3V, T_J = -40°C to 125°C(7), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Switching Timing Characteristics						
Minimum Pulse Width					5	ns
Propagation Delay(8)	t_{PLH}, t_{PHL}			14		ns
Pulse Width Distortion	PWD	$\|t_{PLH}- t_{PHL}\|$		1.5	4.5	ns
Propagation Delay Skew (9)	$t_{PSK(P-P)}$				4.5	ns
Channel-Channel Skew	t_{PS}	For both co-directional and opposing direction		0.8	2.5	ns
Output Rise/Fall Time(8)	t_r, t_f	C_L=15pF		2.5	5	ns
Peak Eye Diagram Jitter(10)	$t_{JIT(PK)}$			1.5		ns
Enable to Data Valid(11)	t_{EN-ON}			60	90	ns
Enable to Data Tri-State(11)	t_{EN-OFF}			50	75	ns
Input Power Fail to Valid Default Output	t_{SD}			500		ns
Start-up Time	t_{START}	From VDD1/VDD2 on to output valid		75		µs
Common-mode Transient Immunity(10)	CMTI	IN=0V or VDD, V_{CM} = 1.5kV	±100			kV/µs
Power Supply Range						
Supply Voltage Range	V_{DD1}		2.5		5.5	V
	V_{DD2}		2.5		5.5	V
Under Voltage Lockout Threshold	$V_{UVLO1-R}$	V_{DD1} Rising		2.25		V
	$V_{UVLO2-R}$	V_{DD2} Rising		2.25		V
Under Voltage Lockout Threshold Hysteresis	V_{UVHYS1}	V_{DD1}		200		mV
	V_{UVHYS2}	V_{DD2}		200		mV
Pin Input / Output Logic Threshold						
Input Voltage High Threshold	V_{ITH-H}	INx, ENx pins			2	V
Input Voltage Low Threshold	V_{ITH-L}		0.8			V
Input Threshold Hysteresis	$V_{ITH-HYS}$			350		mV
Pin Input Current Leakage		Connect INx to VDDx or GNDx			±10	µA
Pin Input Current Leakage		Test ENx pins, ENx =0V	-10	-5		µA
Output High Voltage	V_{OH}	OUTx pins. IOUT=-4mA	V_{DDx}-0.4	V_{DDx}-0.2		V
Output Low Voltage	V_{OL}	OUTx pins. IOUT=4mA		0.2	0.4	V
Tristate (high-impedance) Output Leakage Current		Connect OUTx to VDDx or GNDx, ENx = GNDx.			±10	µA
Output Impedance(12)	Z_O	OUTx pins		50		Ω
Thermal Protection						
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			20		°C

ELECTRICAL CHARACTERISTICS *(continued)*

V_{DD1} = V_{DD2} = 3.3V, T_J = -40°C to 125°C(7), typical values are tested at T_J = 25°C, unless otherwise noted.

Part Number	Parameter	Condition	Min	Typ	Max	Units
Power Supply Current						
DC Supply Current (*INx = 0V or VDD****)***						
MP27931	VDD1 Current	INx = VDD		2.5	3.8	mA
		INx = 0		7.9	11.9	mA
	VDD2 Current	INx = VDD		3.5	5.3	mA
		INx = 0		5.3	8.0	mA
MP27931-L	VDD1 Current	INx = VDD		7.9	11.9	mA
		INx = 0		2.5	3.8	mA
	VDD2 Current	INx = VDD		5.3	8.0	mA
		INx = 0		3.5	5.3	mA
1Mbps Supply Current (*INx = 500kHz Square Wave, C_{LOAD} = 15 pF on All Outputs****)***						
MP27931 MP27931-L	VDD1 Current			5.2	7.9	mA
	VDD2 Current			4.5	6.8	mA
10Mbps Supply Current (*INx = 5MHz Square Wave, C_{LOAD} = 15 pF on All Outputs****)***						
MP27931 MP27931-L	VDD1 Current			5.6	8.4	mA
	VDD2 Current			5.6	8.4	mA
100Mbps Supply Current (*INx = 50MHz Square Wave, C_{LOAD} = 15 pF on All Outputs****)***						
MP27931 MP27931-L	VDD1 Current			9.3	14.0	mA
	VDD2 Current			16.7	25.1	mA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{DD1} = V_{DD2} = 2.5V, T_J = -40°C to 125°C(7), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Switching Timing Characteristics						
Minimum Pulse Width					5	ns
Propagation Delay(8)	t_{PLH}, t_{PHL}			15		ns
Pulse Width Distortion	PWD	$\|t_{PLH}- t_{PHL}\|$		1.5	4.5	ns
Propagation Delay Skew (9)	$t_{PSK(P-P)}$				4.5	ns
Channel-Channel Skew	t_{PS}	For both co-directional and opposing direction		0.8	2.5	ns
Output Rise/Fall Time(8)	t_r, t_f	C_L=15pF		2.5	5	ns
Peak Eye Diagram Jitter(10)	$t_{JIT(PK)}$			1.5		ns
Enable to Data Valid(11)	t_{EN-ON}			60	90	ns
Enable to Data Tri-State(11)	t_{EN-OFF}			50	75	ns
Input Power Fail to Valid Default Output	t_{SD}			500		ns
Start-up Time	t_{START}	From VDD1/VDD2 on to output valid		75		µs
Common-mode Transient Immunity(10)	CMTI	IN=0V or VDD, V_{CM} = 1.5kV	±100			kV/µs
Power Supply Range						
Supply Voltage Range	V_{DD1}		2.5		5.5	V
	V_{DD2}		2.5		5.5	V
Under Voltage Lockout Threshold	$V_{UVLO1-R}$	V_{DD1} Rising		2.25		V
	$V_{UVLO2-R}$	V_{DD2} Rising		2.25		V
Under Voltage Lockout Threshold Hysteresis	V_{UVHYS1}	V_{DD1}		200		mV
	V_{UVHYS2}	V_{DD2}		200		mV
Pin Input / Output Logic Threshold						
Input Voltage High Threshold	V_{ITH-H}	INx, ENx pins			2	V
Input Voltage Low Threshold	V_{ITH-L}		0.8			V
Input Threshold Hysteresis	$V_{ITH-HYS}$			350		mV
Pin Input Current Leakage		Connect INx to VDDx or GNDx			±10	µA
Pin Input Current Leakage		Test ENx pins, ENx =0V	-10	-5		µA
Output High Voltage	V_{OH}	OUTx pins. IOUT=-4mA	V_{DDx}-0.4	V_{DDx}-0.2		V
Output Low Voltage	V_{OL}	OUTx pins. IOUT=4mA		0.2	0.4	V
Tristate (high-impedance) Output Leakage Current		Connect OUTx to VDDx or GNDx, ENx = GNDx.			±10	µA
Output Impedance(12)	Z_O	OUTx pins		50		Ω
Thermal Protection						
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			20		°C

ELECTRICAL CHARACTERISTICS *(continued)*

V_{DD1} = V_{DD2} = 2.5V, T_J = -40°C to 125°C(7), typical values are tested at T_J = 25°C, unless otherwise noted.

Part Number	Parameter	Condition	Min	Typ	Max	Units
Power Supply Current						
DC Supply Current (*INx = 0V or VDD****)***						
MP27931	VDD1 Current	INx = VDD		2.5	3.8	mA
		INx = 0		7.9	11.9	mA
	VDD2 Current	INx = VDD		3.5	5.3	mA
		INx = 0		5.3	8.0	mA
MP27931-L	VDD1 Current	INx = VDD		7.9	11.9	mA
		INx = 0		2.5	3.8	mA
	VDD2 Current	INx = VDD		5.3	8.0	mA
		INx = 0		3.5	5.3	mA
1Mbps Supply Current (*INx = 500kHz Square Wave, C_{LOAD} = 15 pF on All Outputs****)***						
MP27931 MP27931-L	VDD1 Current			5.2	7.8	mA
	VDD2 Current			4.5	6.7	mA
10Mbps Supply Current (*INx = 5MHz Square Wave, C_{LOAD} = 15 pF on All Outputs****)***						
MP27931 MP27931-L	VDD1 Current			5.5	8.3	mA
	VDD2 Current			5.3	8.0	mA
100Mbps Supply Current (*INx = 50MHz Square Wave, C_{LOAD} = 15 pF on All Outputs****)***						
MP27931 MP27931-L	VDD1 Current			8.2	12.3	mA
	VDD2 Current			13.4	20.1	mA

Notes:

7) Not tested in production, derived by over-temperature correlation.
8) Refer to Figure 4.
9) $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
10) Derived by sample characterization, not tested in production.
11) Refer to Figure 6.
12) The nominal output impedance of an isolator driver channel is approximately 50Ω±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled-impedance PCB traces.

REGULATORY INFORMATION

UL	CSA	VDE(IEC)	CQC
Certified according to UL1577 Component Recognition Program	Certified according to CSA Component Acceptance Service Notice No.5A	Certified according to DIN EN IEC 60747-17 (VDE 0884-17): 2021-10; EN IEC 60747-17:2020 + AC:2021	Certified according to GB4943.1-2011
SOIC-16 WB Package: Single protection, 5000V_{RMS}	SOIC-16 WB Package: Single protection, 5000V_{RMS}	Basic isolation: Maximum transient isolation voltage, 7071 V_{PK} Maximum repetitive peak isolation voltage, 1200 V_{PK} Maximum surge isolation voltage, 3077 V_{PK}	Altitude ≤ 5000m, Tropical Climate, Reinforced insulation 600V_{RMS} Maximum working voltage Basic insulation 1000V_{RMS} Maximum working voltage
File (E322138)	File (E322138)	File (Pending)	File (Pending)

Notes:

13) Regulatory Certification apply to 5000V_{RMS} rated devices which are production tested to 6000V_{RMS} for 1 second. Regulatory Certification apply to 3750V_{RMS} rated devices which are production tested to 4500V_{RMS} for 1 second,

INSULATION SPECIFICATIONS

Parameter	Symbol	Condition	SOIC-16 WB	Units
External Clearance (14)	CLR	According to IEC 60664-1(VDE 0110-1) Shortest pin-to-pin distance through air between primary and secondary side	>8	mm
External Creepage (14)	CPG	According to IEC 60664-1(VDE 0110-1) Shortest pin-to-pin distance across the package surface between primary and secondary side	>8	mm
Minimum Internal Gap	DTI	Internal Clearance	>20	μm
Tracking Resistance (Comparative Tracking Index)	CTI	According to IEC 60112	>600	V_{RMS}
Material Group		According to IEC 60664-1	I	
Overvoltage Category per IEC 60664-1		Rated mains voltages ≤ 150V_{RMS}	I-IV	
		Rated mains voltages ≤ 300V_{RMS}	I-IV	
		Rated mains voltages ≤ 600V_{RMS}	I-III	

Notes:

14) Refer to package information for detailed dimensions. As isolated solution, the recommended land pattern is helpful to keep enough safety creepage and clearance distances on a printed-circuit board.

INSULATION CHARACTERISTICS

Parameter	Symbol	Condition	SOIC-16 WB	Units
UL 1577, 5th Ed				
Isolation Voltage Rating	V_{ISO}	$V_{TEST}=V_{ISO}$, t=60s, *(Qualification Test)* $V_{TEST}=V_{ISO}$ × 1.2, t=1s, *(100% Production Test)*	5000	V_{RMS}
DIN EN IEC 60747-17 (VDE 0884-17): 2021-10				
Maximum Working Isolation Voltage	V_{IORM}		1200	V_{PEAK}
Apparent Charge (15)	q_{pd}	Method B1. routine test $V_{pd(m)}$ = 1.875 x V_{IORM}, t_m = 1s, *(100% Production Test)*	<5	pC
		Method A, after sample test. And subgroup1 $V_{pd(m)}=V_{IORM}$ × 1.3, t_m=10s, After type test subgroup2/3 $V_{pd(m)}=V_{IORM}$ × 1.2, t_m=10s, *(Qualification Test)*	<5	pC
Transient Overvoltage	V_{IOTM}	$V_{TEST}=V_{IOTM}$ for t=60s *(Qualification Test)* $V_{TEST}=V_{IOTM}$ × 1.2 for t=1s *(100% Production Test)*	7071	V_{PEAK}
Maximum Surge Isolation Voltage	V_{IOSM}	Tested with surge waveform 1.2μs/50μs . $V_{TEST}=V_{ISOM}$ × 1.3 *(Qualification Test)*	3077	V_{PEAK}
Barrier Capacitance (16)	C_{IO}	f=1MHz	2	pF
Insulation Resistance (16)	R_{IO}	V_{IO}=500V, T_A=25°C	$>10^{12}$	Ω
		V_{IO}=500V, 100°C≤T_A≤125°C	$>10^{11}$	Ω
		V_{IO}=500V, $T_A=T_S$=150°C	$>10^{9}$	Ω
Pollution Degree			2	
Climatic Category			40/125/21	

Notes:

15) Electrical discharge caused by a partial discharge in the coupler.

16) The primary side terminals as well as the secondary side terminals of the barrier are connected together forming a two-terminal device. Then C_{IO} and R_{IO} are measured between the two terminals of the coupler.

SAFETY LIMITING VALUES (17)

Parameter	Symbol	Condition	SOIC-16 WB	Units
Maximum Safety Temperature (18)	T_S		150	°C
Safety input, output, or supply current	I_S	V_{DD} = 5.5 V, T_J = 150°C, T_A = 25°C	400	mA
Safety input, output, or total power (19)	P_S	T_J = 150°C, T_A = 25°C	2200	mW

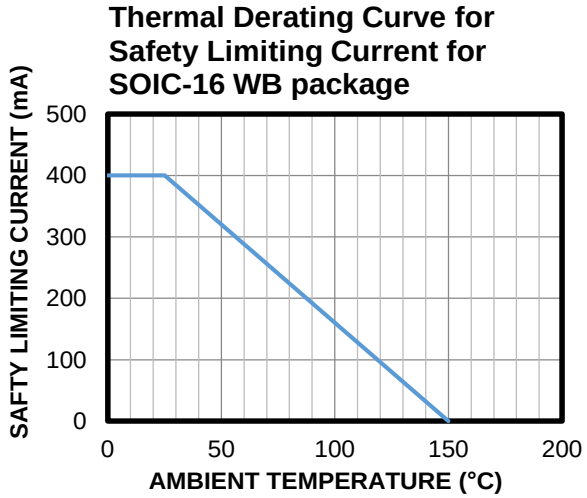
Notes:

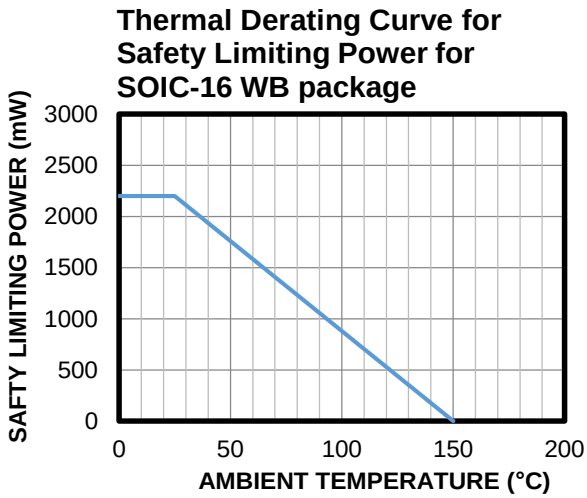
17) Maximum value allowed in the event of a failure.

18) The maximum safety temperature T_S has the same value as the maximum junction temperature T_J (MAX) specified in ABSOLUTE MAXIMUM RATINGS.

19) The safety power dissipation is a function of the maximum junction temperature TJ (MAX), the junction-to-ambient thermal resistance θ_{JA} and the ambient temperature T_A:
$T_S=T_J$ (MAX)=T_A+(θ_{JA} x P_S)

THERMAL DERATING CURVE FOR SAFETY LIMITING VALUES





TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board in the Design Example section on Page xx. V_{DD1} = V_{DD2} = 5V, INA / INB / INC / IND = 5MHz square waveform, T_A = 25°C, unless otherwise noted.

TBD

FUNCTIONAL BLOCK DIAGRAM

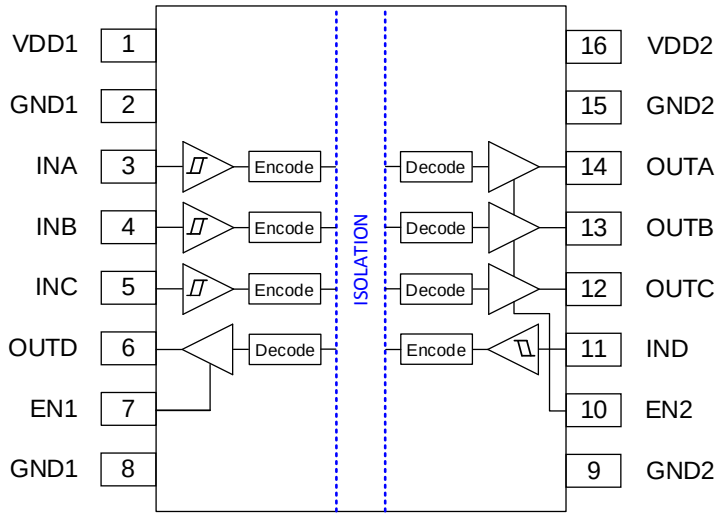


Figure 1: Functional Block Diagram

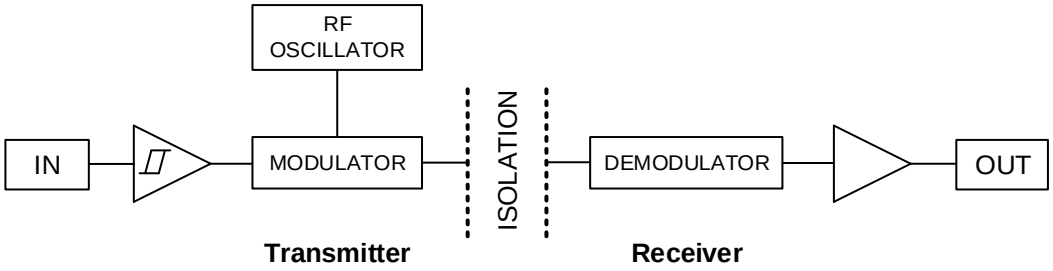


Figure 2: Isolated Signal Modulation Diagram

OUTPUT TRUTH TABLE

Table 1: Truth Table

IN SIDE VDD	OUT SIDE VDD	OUT SIDE EN	IN	OUT
Normal work state:				
Powered	Powered	H or FLOAT	H	H
Powered	Powered	H or FLOAT	L	L
Powered	Powered	H or FLOAT	FLOAT	H for MP27931 L for MP27931-L
EN off state				
X	Powered	L	X	Hi-Z
Input side powers off state:				
Un-powered(20)	Powered	H or FLOAT	X	H for MP27931 L for MP27931-L
Output side powers off state:				
X	Un-powered(20)	X	X	I

Hi-Z = high impendence, X = do not care, FLOAT = not connected, I = indeterminate, H = high level voltage, L = low level voltage

Notes:

20) An I/O can power the die for a given side through an internal diode if its source has adequate current.

OPERATION

The MP27931 is a 4 channels digital isolator optimized to replacing traditional opto-coupler isolation in application. It adopts capacitive isolation technology, supporting up to 5kVrms insulation voltage rating and up to 150Mbps data rate transmission.

Signal Isolation Function

MP27931 supports 5kVrms voltage isolation between two sides. Data signals applied on INx pins are transmitted to corresponding OUTx through internal isolation barrier. Figure 1 shows the IC diagram and Figure 2 shows isolated signal transmission structures.

Each signal channel consists of an RF transmitter and RF receiver separated by a semiconductor-based isolation barrier, on input port, the transmitter modulates the signal through an RF oscillator. When input signal is high, the RF oscillator keeps off. When input signal is low, the RF oscillator keeps on. On receiver side, a demodulator decodes the input state according to its RF energy content and applies the result to output pin. This signal modulation provides low power consumption and improved immunity to magnetic fields. Figure 3 shows the modulation scheme.

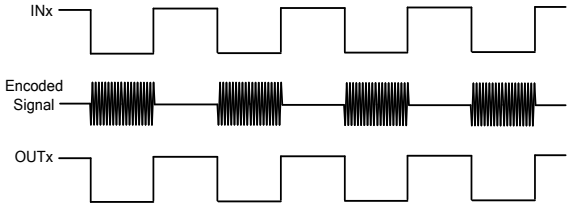


Figure 3: Signal Modulation Scheme

All channel signals have schmitt trigger input to enhance noise immunity. At the same time, all channels in one direction are optimized for propagation delay matching, which means they have similar delay time in one chip. It can be used for SPI interface isolation with good channel-channel skew.

Fail-safe Operation

MP27931 default output is high (MP27931-L default output is low) when the input power supply is not applied. With this fail-safe predetermined output, dc correctness is ensured in the absence of input logic transitions. So MP27931 can be used for SPI interface isolation while slave device is not selected at power failure status.

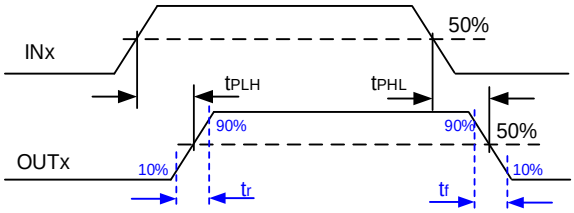


Figure 4: Propagation Delay Time

Power Supply

Both the VDD1 and VDD2 have an under-voltage lockout (UVLO) function to prevent erroneous operation during device startup & shutdown, or when the corresponding VDD is low.

Outputs are high impedance during power-up until the corresponding VDD is above the UVLO threshold for time period t_{START}. After this period, the outputs follow the state of inputs. Figure 5 shows the UVLO delay function.

Each side can enter or exit UVLO independently. While the output state is different. For example, when VDD1 enters UVLO, side 2 output will keep high if VDD2 is on. But when VDD2 enters in UVLO, side 2 output will be high impedance even VDD1 is on. This feature can prevent outputs wrong flip during VDD startup. Figure 5 shows the operation.

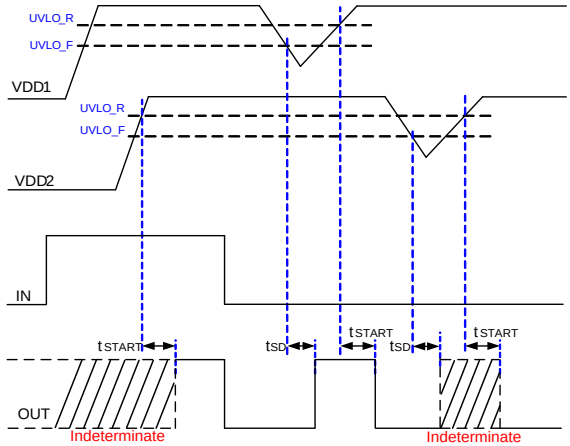


Figure 5: UVLO and Output Delay

EN Pin Control

MP27931 has one EN pin on each side of the isolation barrier, theses pins only control the output driver of each channel. When EN is high or floats, the OUT signal follows IN signal. When EN is low, the OUT runs into high-impedance state. Enable inputs EN1 and EN2 can be used for multiplexing, clock sync, or other output control. It is recommended that the enable inputs be connected to an external logic high or low level when the IC is operating in noisy environments. To minimize noise coupling, do not connect circuit traces to EN1 or EN2 if they are left floating.

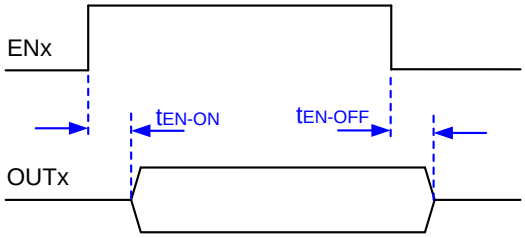


Figure 6: Enable Delay Time

Driver Output Protection

When the driver pin outputs over load or short to GND, one internal current limit circuit prevents the current from running too high. And if the die temperature is too high due to the high current, it will trigger thermal protection.

Thermal Protection

MP27931 has over temperature protection function in case the power dissipation during fault conditions. This thermal protection circuit disables the driver outputs when a die temperature rise to 150°C, There is about 20°C hysteresis. Once the junction temperature drops to about 130°C, the driver outputs are re-enabled work normally.

APPLICATION INFORMATION

Bypass Capacitor

A 0.1μF capacitor is recommended to ensure reliable propagation. Bypass capacitor should be placed as close to power supply and ground pins as possible.

Design Example

Table 2 is a design example following the application guidelines for the specifications below.

Table 2: Design Example

V_{DD1}	2.5-5.5V
V_{DD2}	2.5-5.5V

The detailed application schematic is shown in Figure 8. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheet.

PCB Layout Guidelines

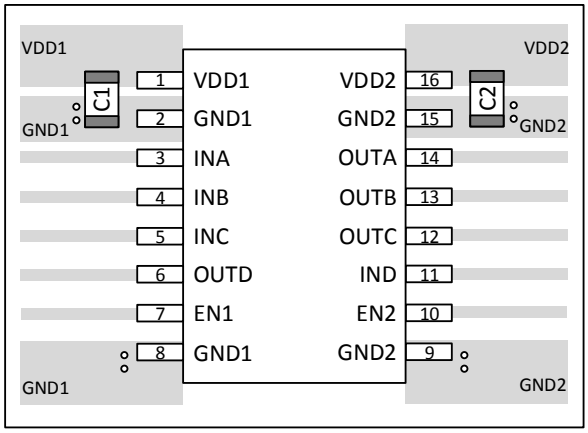
PCB layout is very important for normal operation. Refer to below layout guide lines.

1) For safety concern, primary side and secondary side must be physically separated. And the creepage/clearance must meet the standard for a certain application.

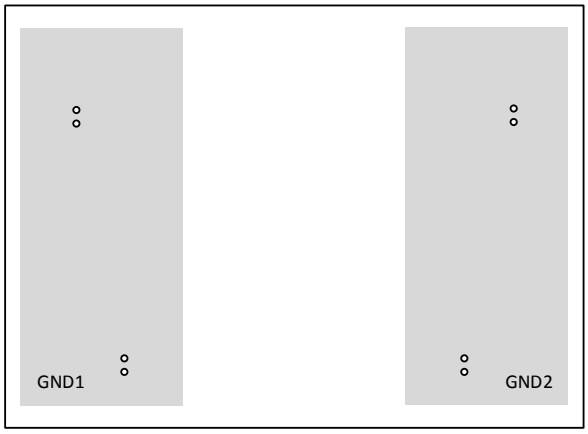
2) Minimize the loop area between signal traces and GND to avoid coupling noise into system. Keep signal traces away from other high speed traces or switching node, such as transformer, power inductor and MOS.

3) Two ceramic input decoupling capacitors need to be placed as close as possible to the VDD1 and GND1, VDD2 and GND2 pins.

4) For high speed signal, a four layers PCB is recommended to accomplish better EMI and signal propagation performance. Layer stacking: high speed signal, solid GND plane, VDD plane, low frequency signal.



Top Layer



Bottom Layer

Figure 7: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

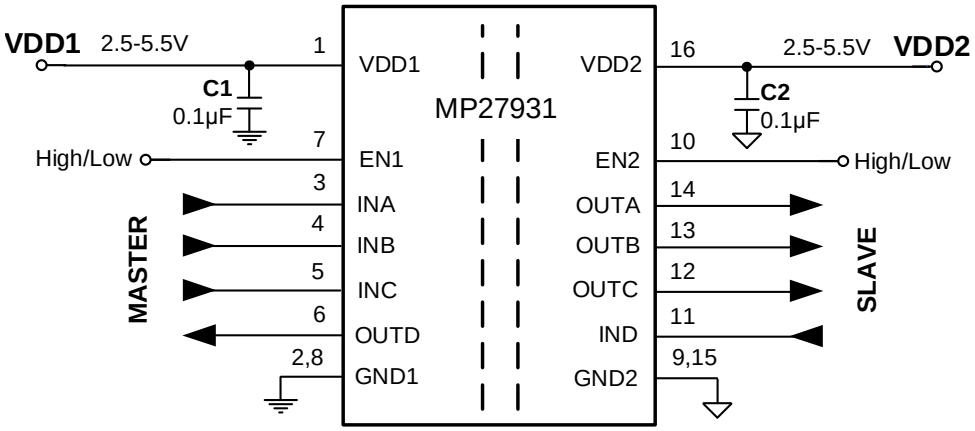
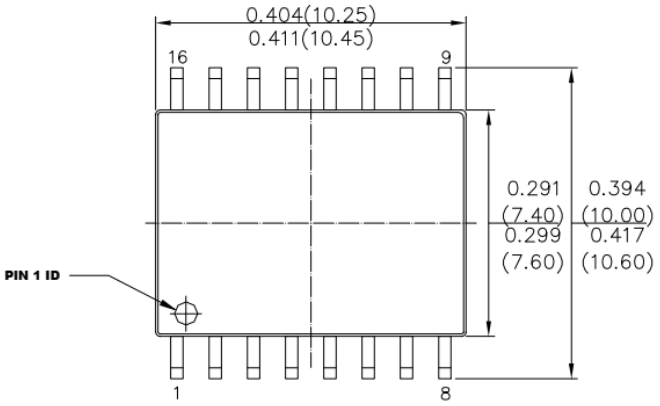


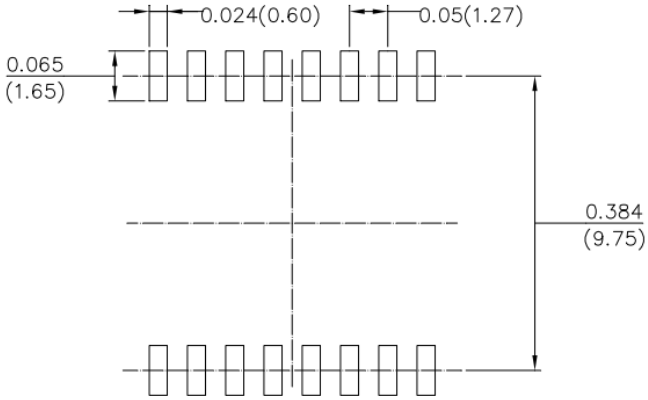
Figure 8: 4 Channels (Channel Direction: 3 Forward 1 Reverse) Isolated Interface

PACKAGE INFORMATION

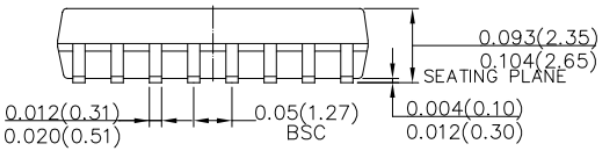
SOIC-16 WB (HV ISOLATION)



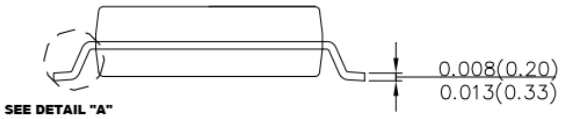
TOP VIEW



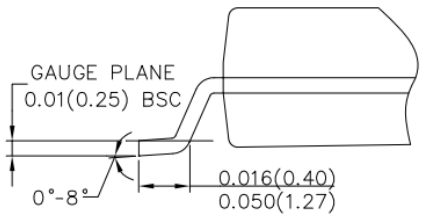
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-013, VARIATION AA.
6) DRAWING IS NOT TO SCALE.