MP4582

100V, 2A, 8μA IQ, SYNC Step-Down DC-DC Converter

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MP4582 is a 8μA IQ, synchronous step-down converter with integrated high-side and low-side MOSFETs. It supports up to 2A output current with internal compensation.

High power conversion efficiency over a wide load range is achieved by power save mode(PSM) and low IQ at light load condition to reduce the switching and gate driving losses.

To achieve small output ripple in light load, pulling MODE/SYNC pin high can set forced continuous conduction mode (FCCM). The frequency is always fixed 400KHz with all load condition.

Full protection features, include over-current protection (OCP), short-circuit protection (SCP) with hiccup, input and output over-voltage protection (OVP), and over-temperature protection (OTP).

The MP4582 is available in a QFN-19 (3mm×5mm) package.

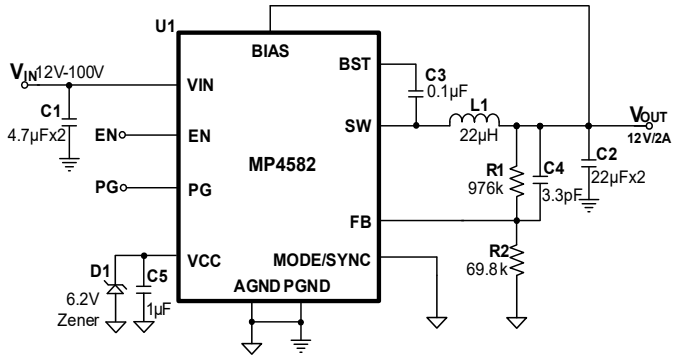
FEATURES

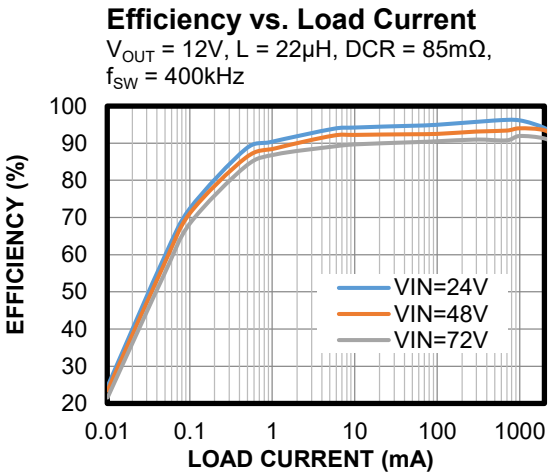
- 4.5V-to-100V Input Voltage Range
- 8μA Quiescent Current
- Fixed 400KHz Switching Frequency
- Selectable PSM/FCCM Mode
- 0.8V to 35V Output Voltage Range
- 180m/90m Internal MOSFETs
- Power Good(PG) Indication
- Additional BIAS Pin for High Efficiency Vcc
- Internal Loop Compensation and Soft-Start
- Available in QFN-19 (3mm×5mm) Package

APPLICATIONS

- Power Tool
- Solar Inverter/Optimizer
- Portable Power Station
- Battery Management System(BMS)
- Server Power/Telecom Power Unit

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP4582GQVE	QFN-19 (3mmx5mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP4582GQVE-Z).

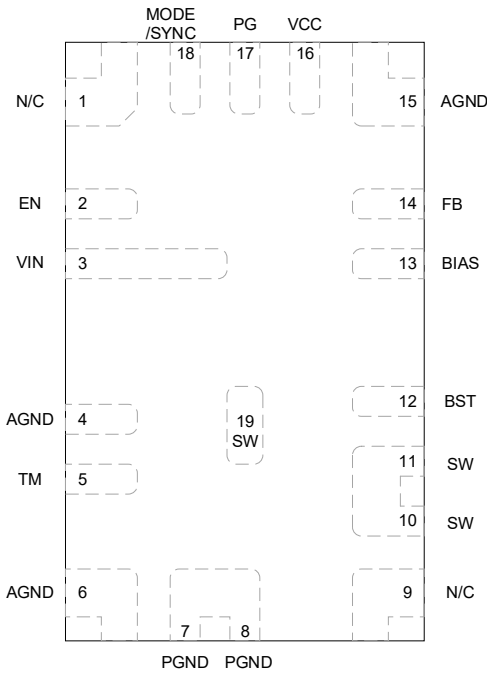
TOP MARKING

MPYW
4582
LLL
E

MP: MPS prefix
Y: Year code
W: Week code
4582: Part number
LLL: Lot number
E: Wettable flank

PACKAGE REFERENCE

TOP VIEW



QFN-19 (3mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 9	NC	**No Connection Pin.** Connect to Ground to improve thermal performance.
2	EN	**Power Enable Pin**. Pull high to enable MP4582, pull low to disable MP4582. Float internally, must pull high or pull low externally for this pin in application.
3	VIN	**Power Supply Input Pin**. A decoupling capacitor must be placed close to this pin and PGND to minimize switching spikes.
4, 6, 15	AGND	**Signal Ground**. Reference ground of the regulated output voltage. Single grounding to PGND (pin7 and pin8).
5	TM	**Test Mode Pin.** Must float in application.
7, 8	PGND	**Power Ground Pin.**
10, 11, 19	SW	**Switch Node of Converter.** Connect to the source of high-side FET and drain of low-side FET.
12	BST	**Bootstrap Power Pin.** Connect a 0.1µF capacitor between BST and SW.
13	BIAS	**External Power Bias Supply Pin.** It is suggested to connect BIAS to V_{OUT} or other voltage rail if the voltage>4.4V.
14	FB	**VOUT Voltage Feedback Pin.** Connect a resistor divider from V_{OUT} to FB.
16	VCC	**Internal 5V LDO output.** Supply power to internal control circuit. Decoupling with ≥1uF ceramic capacitor. Must connect one 6.2V Zener diode from VCC pin to GND.
17	PG	**Power Good Output Pin**. The output of PG is open drain, the PG output is pulled low when the EN UVLO, input UVLO or OTP is triggered.
18	MODE/ SYNC	**MODE/SYNC Pin**. Pull this pin low to set PSM mode, pull this pin high to set FCCM mode. Apply external clock to MODE/SYNC pin can change the switching frequency.

ABSOLUTE MAXIMUM RATINGS (1)

VIN, EN .....-0.3V to +105V
SW .....-0.3V to VIN+0.3V
SW (<10ns) .....-4V to VIN+4V
BIAS.....-0.3V to 14V
BST to SW .....-0.3V to 6.5V
All Other Pins.....-0.3V to +6.5V
Continuous Power Dissipation (T_A = +25°C) (2)
..... 3.9W(4)
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±1000V
Charged device model (CDM) ..... ±1000V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....4.5V to 100V
Output voltage (V_{OUT}).....0.8V to 35V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

EV4582-QVE-00A (4)	32	8	°C/W
QFN-19 (3mmx5mm) (5)	48	38	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EV4582-QVE-00A, a 64mmx64mm, 1OZ, 4-layer PCB.
5) The value of θ_{JA} given in this table is only valid for comparison with other packages, and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 48V, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
VIN Under Voltage Lockout Threshold Rising	VIN_{UVLO-R}			4.2		V
VIN Under Voltage Lockout Threshold Hysteresis	VIN_{HYS}			350		mV
VCC Under Voltage Lockout Threshold Rising	VCC_{UVLO-R}	VCC Rising		3.85		V
VCC Under Voltage Lockout Threshold Hysteresis	VCC_{HYS}			350		mV
VCC Regulation Voltage		V_{IN}=12V or V_{BIAS}=12V, 5mA	4.75	5	5.25	V
		V_{IN}=4.5V,5mA		4		V
		V_{BIAS}=4.5V,5mA		4.3		V
BIAS Power Supply Threshold		V_{BIAS} rising, override V_{IN} supply		4.25	4.4	V
		V_{BIAS} falling, recover to V_{IN} supply		4.05	4.2	V
Supply Current						
Shutdown Current	I_{SD}	V_{EN} = 0V, Measured on VIN pin		1		µA
Quiescent Current	I_Q	V_{FB} =0.82V, V_{BIAS}=0V, V_{BST}=5V, no switching, Measured on VIN pin		8		µA
		V_{FB} =0.82V, V_{BIAS}=5V, V_{BST}=5V, no switching, Measured on VIN pin		0.5		µA
		V_{FB} =0.82V, V_{BIAS}=5V, V_{BST}=5V, no switching, Measured on BIAS pin		8		µA
Enable Control						
EN Input High Threshold	V_{EN-ON}	V_{EN} Rising		1.2		V
EN Hysteresis	V_{EN-H}	V_{EN} Rising		225		mV
EN Input Current	I_{EN}	V_{EN} = 5V		0		µA
EN Turn-on Delay		EN on to Switching		400		µs
Switching Frequency						
Switching Frequency	F_{SW}		-10%	400	+10%	kHz
Minimum Off Time(6)	$t_{MIN-OFF}$			120		ns
Minimum On Time(6)	t_{MIN-ON}			40		ns
Reference Voltage						
FB Reference Voltage	V_{REF}	4.5V to 100V, T_J = 25°C	-1%	0.8	+1%	V
		4.5V to 100V, T_J = -40°C to 125°C	-1.5%	0.8	+1.5%	V
FB Input Current	I_{FB}	V_{FB}=1.05V	-100	-50	-10	nA
Internal Soft-Start Time	t_{SS}	10% to 90% of V_{REF}		4		ms

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 48V, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
FB Under Voltage Threshold	V_{UVP}			60%		V_{REF}
FB Over Voltage Threshold	V_{OVP}			107%		V_{REF}
FB Over Voltage Recover Hysteresis				1%		V_{REF}
Power Switch						
Low-Side Switch On-Resistance	R_{ON-L}			90		mΩ
High-Side Switch On-Resistance	R_{ON-H}			180		mΩ
Current Limit						
High Side Peak Current Limit	I_{H-LIMT}			3.1		A
Low Side Valley Current Limit	I_{L-LIMT}		1.8	2.1	2.5	A
Inductor Current ZCD Threshold	I_{ZCD}		0	50	100	mA
Power Good (PG)						
Power Good Upper Threshold		FB rising, PG falling	104%	107%	110%	V_{FB}
		FB falling, PG rising	103%	106%	109%	V_{FB}
		Hysteresis		1%		V_{FB}
Power Good Lower Threshold		FB falling, PG falling,	90%	93%	96%	V_{FB}
		FB rising, PG rising	91%	94%	97%	V_{FB}
		Hysteresis		1%		V_{FB}
Power Good Low to High Delay				380		us
Power Good High to Low Delay				150		us
Power Good Sink Current Capability		Sink 4mA			0.4	V
Power Good Leakage Current		V_{PG}=5V		1		µA
Thermal Protection(6)						
Thermal Shutdown Rising Threshold	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{SD-HYS}			20		°C

Note:

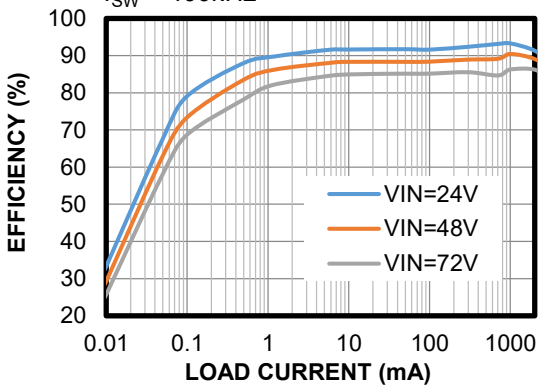
6) Guaranteed by engineering sample characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 48V, V_{OUT} = 12V, L = 22µH, T_A = 25°C, unless otherwise noted.

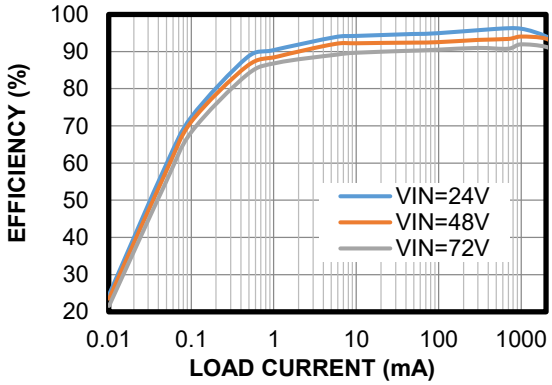
Efficiency vs. Load Current

V_{OUT} = 5V, L = 10µH, DCR = 34.5mΩ, f_{SW} = 400kHz



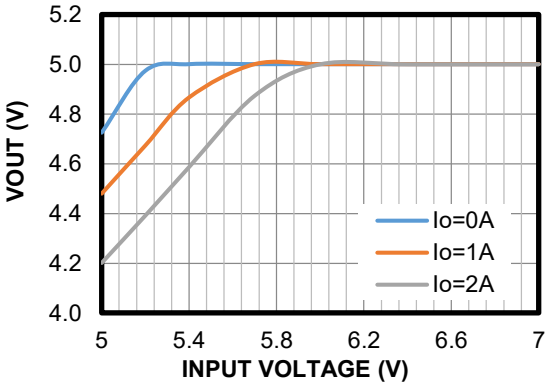
Efficiency vs. Load Current

V_{OUT} = 12V, L = 22µH, DCR = 85mΩ, f_{SW} = 400kHz



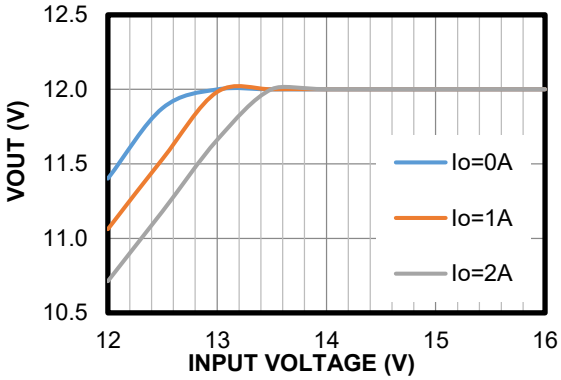
Dropout vs. Load Current

V_{OUT} = 5V, L = 10uH, DCR = 34.5mΩ f_{SW} = 400kHz



Dropout vs. Load Current

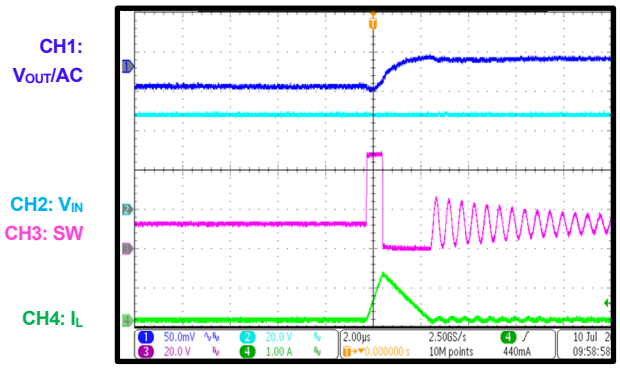
V_{OUT} = 12V, L = 22uH, DCR = 85mΩ f_{SW} = 400kHz



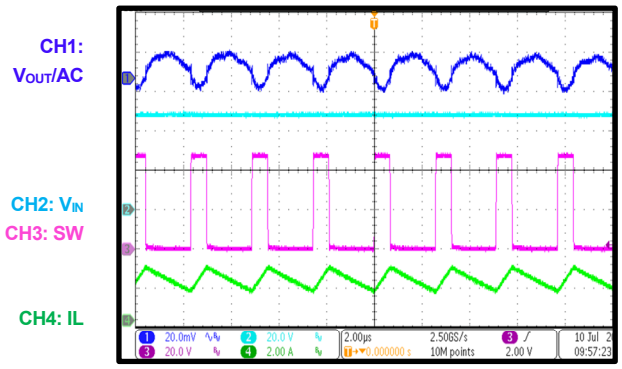
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{OUT} = 12V, L = 22µH, T_A = 25°C, unless otherwise noted.

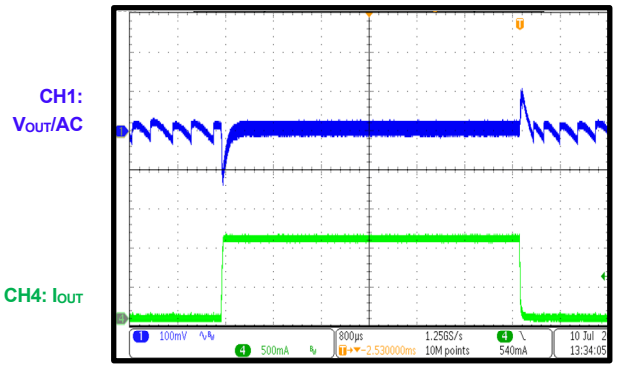
Steady State
I_{OUT}=0A



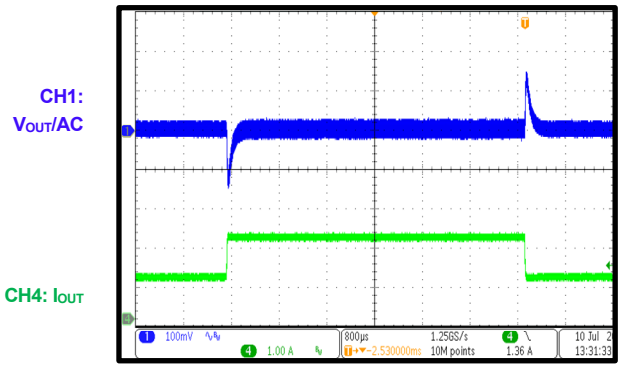
Steady State
I_{OUT}=2A



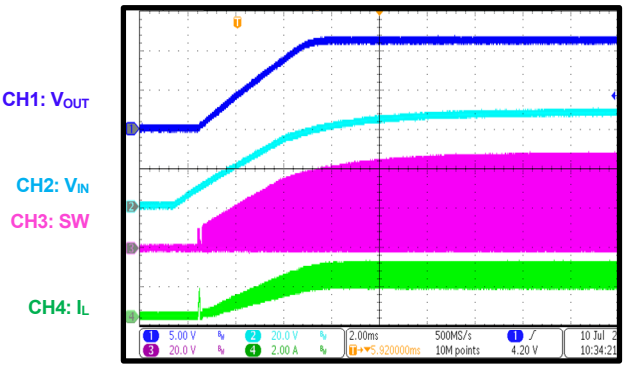
Load Transient
IOUT = 0A to 1A



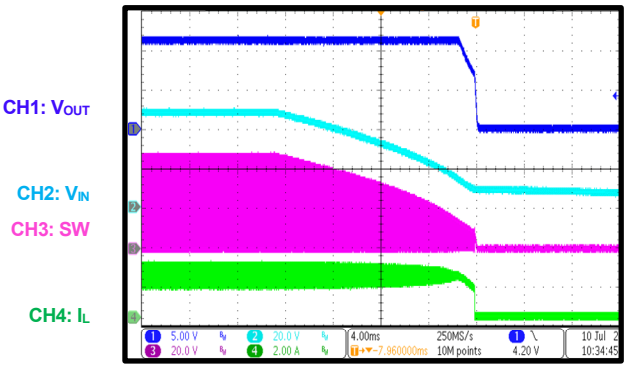
Load Transient
IOUT = 1A to 2A



Startup through VIN
IOUT = 2A



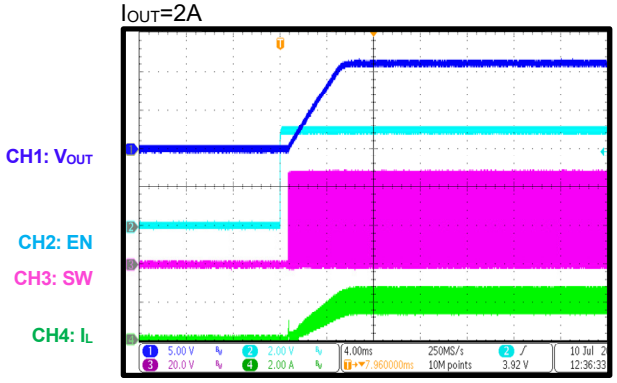
Shutdown through VIN
IOUT = 2A



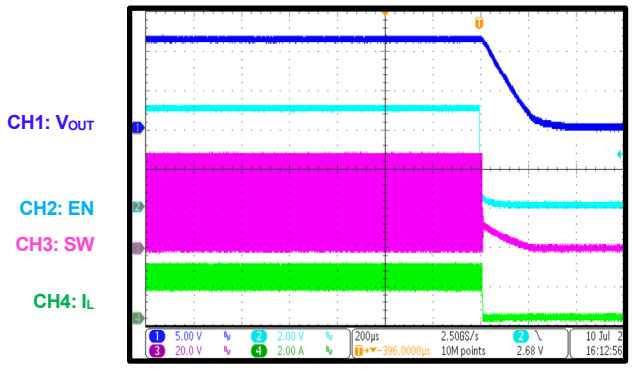
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{OUT} = 12V, L = 22µH, T_A = 25°C, unless otherwise noted.

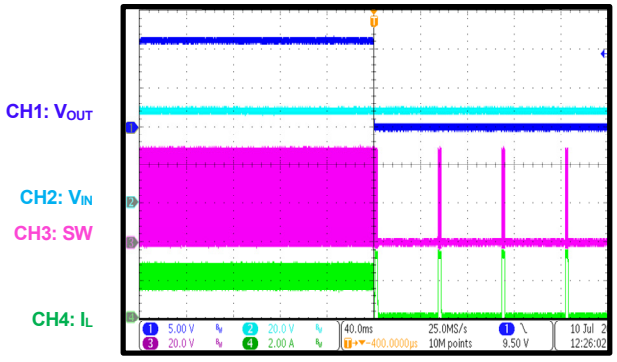
EN Startup
I_{OUT}=2A



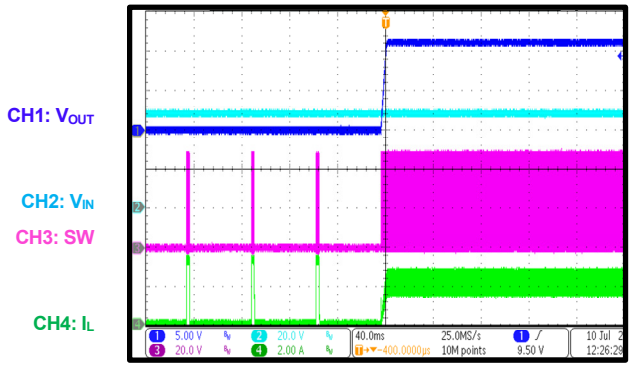
EN Shutdown
I_{OUT}=2A



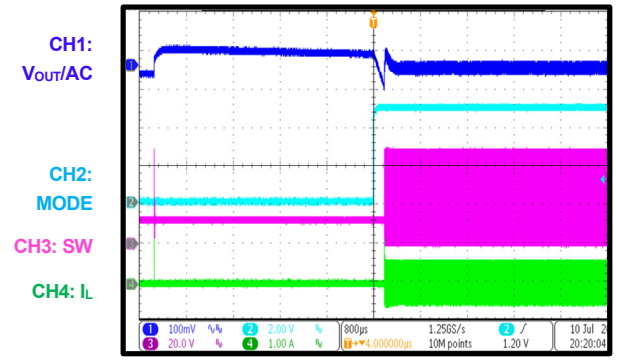
SCP Entry
IOUT=2A → SCP



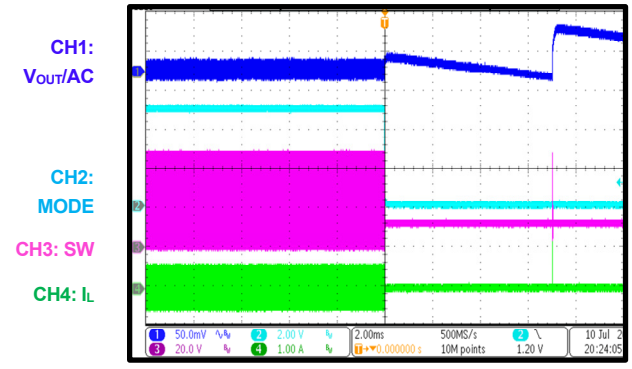
SCP Recovery
IOUT=SCP → 2A



Mode Transient
IOUT=0A, PSM → FCCM



Mode Transient
IOUT=0A, FCCM→ PSM



FUNCTIONAL BLOCK DIAGRAM

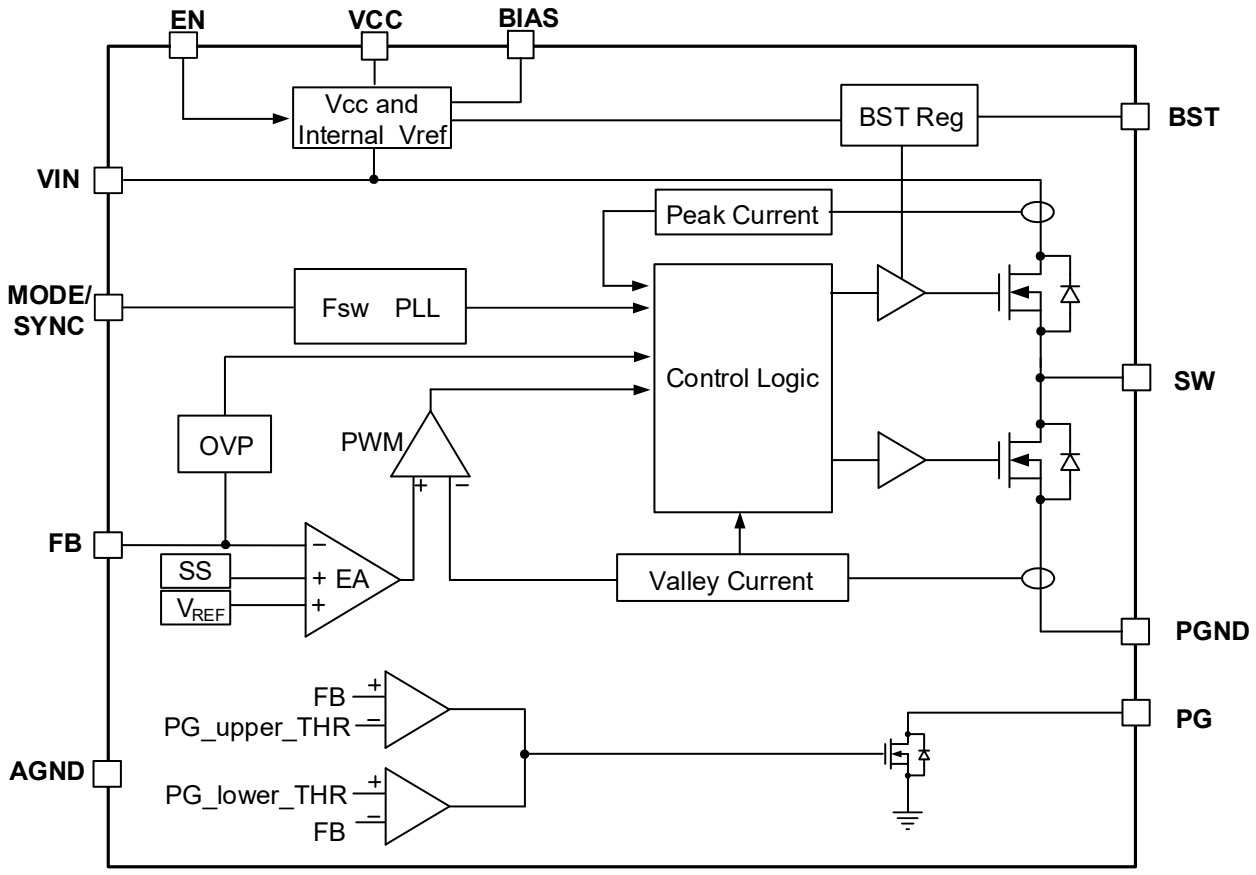


Figure 1: Functional Block Diagram

OPERATION

The MP4582 is a synchronous, step-down, switching regulator with integrated high-side and low-side power MOSFETs. It provides a highly-efficient solution with internal compensation. It features a wide input voltage range, internal soft-start control, and precise current limiting. Its low operational quiescent current makes it suitable for light load high efficiency application. Figure 1 shows the internal block diagram and below sections describe the detail function.

Buck Operation

MP4582 works with a fixed frequency, valley current control mode to regulate the output voltage. In each cycle, high-side MOSFET turns on first if FB voltage is lower than reference voltage. After high-side MOSFET turns off, Low-side MOSFET turns on to conduct the inductor current until it triggers COMP control signal. By repeating operation in this way, MP4582 regulates the output voltage. When the power MOSFET switches off, it remains off for at least 120ns before the next cycle starts.

If, in one PWM period, the current in the low-side MOSFET does not trigger the EA output value, the low-side MOSFET will remain on until trigger EA output value and then turn on high-side MOSFET again.

A dead short occurs between the VIN pin and GND pin if the high-side MOSFET and low-side MOSFET are turned on at the same time. This is called shoot-through. To avoid shoot-through, a dead time is generated internally between the high-side MOSFET and low-side MOSFET on and off periods. The dead time occurs between the high-side MOSFET off time and the low-side MOSFET on time, or vice versa.

Heavy-Load Operation

The MP4582 operates in continuous conduction mode (CCM) when the output current (IOUT) is high and the inductor current is above 0A. In CCM, the HS-FET turns on, then turns off once the on period is complete. Once the HS-FET turns off, the LS-FET turns on to conduct the inductor current. Pulse-width modulation (PWM) mode occurs when f_{SW} remains constant while the part is in CCM.

Light-Load Operation

The MP4582 can work in pulse-skip mode (PSM) under light-load conditions. In PSM, the LS-FET goes into tri-state (Hi-Z) when the inductor current drops close to 0A, and the output capacitors discharge slowly to GND through the FB pin's feedback resistor. If VOUT drops and the internal EA output voltage rises, the MP4582 starts the next switching cycle by turning on the HS-FET. The MP4582 automatically reduces f_{SW} and IQ when the device is not switching. This improves the device's efficiency when IOUT is low. When in PSM under light-load conditions, the HS-FET does not turn on as frequently as it does under heavy-load conditions. The frequency at which the HS-FET turns on is a function of I_{OUT}. As I_{OUT} increases, the HS-FET turns on more frequently. In turn, f_{SW} also increases. I_{OUT} exceeds the upper boundary level when the valley inductor current reaches 0A.

VCC Power Supply

MP4582 control circuit is powered by VCC, which is regulated from both V_{IN} and BIAS. VCC requires one $\geqslant$ 1uF, 16-V ceramic capacitor and one 6.2V Zener diode connected from VCC to GND for proper operation.

VCC_UVLO and VIN_UVLO circuit protect the chip from operating at an insufficient supply voltage. The MP4582 UVLO comparator monitors the voltage of VCC and VIN, MP4582 start work when both VIN and VCC is high enough.

When V_{IN} power is supplied and EN is high, MP4582 regulate V_{CC} from VIN first. If BIAS is higher than 4.25V (typ) and VIN is above UVLO thershold, MP4582 switches the power source from V_{IN} to BIAS, so that MP4582 can get higher efficiency for internal driver loss. If VOUT is higher than 14V, a zener is needed to decrease Vout voltage for BIAS pin power supply, by inserting the zener between Vout and BIAS Pin.

Start Up

When the EN pin is high VCC and VIN exceeds its UVLO, the MP4582 starts up via an internal soft start (SS) signal. Once the MP4582 starts switching, the SS signal ramps up from 0V and is compared to V_{REF}. The lower voltage feed the error amplifier (EA) to control V_{OUT}. After the SS signal exceeds V_{REF}, soft start completes and the internal reference block takes charge of the feedback loop regulation. The MP4582 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, neither the HS-FET nor LS-FET turns on until VSS exceeds VFB.

Enable (EN) and Programmable UVLO

EN pin enables and disables the MP4582. When EN pin voltage rise to the EN high threshold, the MP4582 enables all functions and starts switching operation. Switching operation is disabled when EN voltage falls below its lower threshold. EN is compatible with voltages up to 100V.

There is no internal resistor on EN. For automatic start-up, connect EN to V_{IN} through a resistor.

MODE/SYNC Control

Pull MODE/SYNC pin low to set PSM mode, Pull MODE/SYNC pin high to set FCCM mode. PSM and FCCM mode can transition each other online. Connect an external clock to sync internal switching frequency from default frequency to 2.2MHz.(sync SW rising to rising edge of external signal).

Switching Current Limit

MP4582 supports cycle-by-cycle switching current limit. During LS-FET ON state, the inductor current is monitored. When the sensed inductor current is higher than the valley current limit threshold, HS-FET will wait until inductor current falls below valley current limit to turn on again.

MP4582 also support switching peak current limit during HS-FET on-period. When peak current limit is triggered, the HS-FET shutdown immediately, and turn on LS-FET after a dead-time, the HS-FET will turn on again in next switching period.

Over Load and Short Circuit Protection

During over load or output short circuit condition, the output voltage drops due to cycle-by-cycle switching current limit. Once V_{FB} drops below the under-voltage (UV) threshold. MP4582 enters hiccup mode to periodically restart the part. During the SS time, hiccup mode is disabled.

During hiccup over-current protection (OCP), the MP4582 turns off the output power stage, and discharges the SS capacitor. Then the IC automatically initiates another soft start. If the over-current (OC) condition remains after the soft start ends, the device repeats this hiccup operation until the OC condition is removed. Once the OC condition has been removed, VOUT returns to the regulation level.

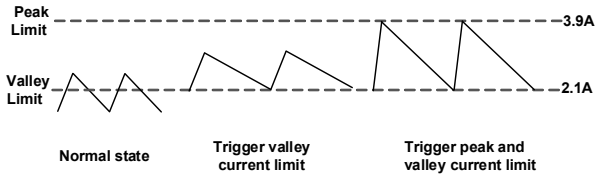


Figure 2: Current Limit Schematic

Input Over-Voltage Protection

MP4582 monitors the input voltage all the time, when the input voltage exceed input over voltage threshold, about 103V, due to negative inductor current, the controller will switch from FCCM mode to DCM mode. MP4582 will recover to normal control when Vin drop to a normal voltage, about 100V.

Output Over-Voltage Protection

MP4582 monitors the output voltage all the time, when the output voltage exceed 107% reference voltage threshold, MP4582 stop high side MOSFET immediately and turn on VOUT discharge function(1kΩ resistor between SW and GND). MP4582 will recover to normal control when VOUT drop to a normal voltage.

BST Power Supply

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. V_{CC} regulates the bootstrap capacitor voltage internally through D1, M1, C3, L1 and C2 (Figure 3). If (V_{IN}-V_{SW}) exceeds 5V, U1 will regulate M1 to maintain a 5V BST voltage across C3.

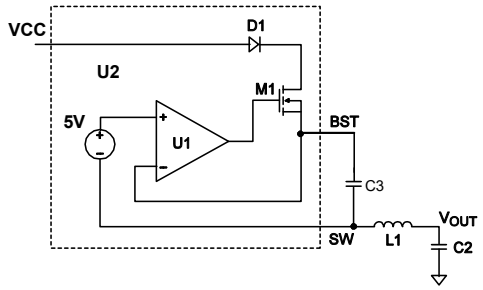


Figure 3: Internal Bootstrap Charger

Thermal Protection

MP4582 integrates one temperature monitor circuit. Once junction temperature is higher than 150°C, MP4582 shuts down. After the temperature drops to lower 130°C, the power supply resumes operation again.

Power Good

The power good signal indicates whether the output voltage is in the normal range compared internal reference voltage. It's an open drain output.

When the output voltage is higher than 94% and lower than 106% of internal reference voltage and the soft start is finished, the power good signal is pulled high; When the output voltage is lower than 93% or higher than 107% after soft start finished, PG signal will be pull low.

The PG output is pulled low when the EN UVLO, input UVLO or OTP is triggered.

APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider is used to set V_{OUT}. First, choose a value for the resistor (R1). Too small of a value for R1 can lead to considerable IQ loss, while too large of a value can make FB noise-sensitive. It is recommended to choose an R1 value between 100kΩ and 1MΩ. Then, R2 can be calculated with Equation (1):

$$R2=\frac{R1}{\frac{V_{OUT}}{V_{REF}}-1} \quad (1)$$

Where V_{REF} is the reference voltage (typically 0.8V). Figure 4 shows the typical feedback circuit.

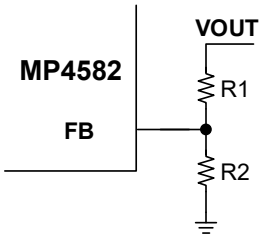


Figure 4: Feedback Network

Selecting the Inductor

A larger-value inductor provides less ripple current, which results in a lower output voltage ripple. However, a larger-value inductor has a larger physical footprint, higher series resistance, and lower saturation current. The inductance can be calculated with Equation (2):

$$L=\frac{V_{OUT}}{f_{SW}\times\Delta I_L}\times(1-\frac{V_{OUT}}{V_{IN}}) \quad (2)$$

Where ΔIL is the peak-to-peak inductor ripple current. It is recommend to choose an inductor ripple current range of 30%~60% of the maximum output current. The inductor should not saturate under the maximum peak inductor current. The peak inductor current can be calculated with Equation (3):

$$I_{LP}=I_{OUT}+\frac{V_{OUT}}{2f_{SW}\times L}\times(1-\frac{V_{OUT}}{V_{IN}}) \quad (3)$$

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the step-down converter while also maintaining the DC input voltage. For the best results, it is recommended to use ceramic capacitors placed as close to VIN as possible. X5R and X7R capacitors with ceramic dielectrics are recommended for their stability amid temperature fluctuations.

The capacitors must also have a ripple current rating above the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (4):

$$I_{CIN}=I_{OUT}\times\sqrt{\frac{V_{OUT}}{V_{IN}}\times(1-\frac{V_{OUT}}{V_{IN}})} \quad (4)$$

The worst-case scenario occurs at V_{IN} = 2V_{OUT}, calculated with Equation (5):

$$I_{CIN}=\frac{I_{OUT}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating greater than half the maximum load current.

The input capacitance determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the relevant specifications. The input voltage ripple can be estimated with Equation (6):

$$\Delta V_{IN}=\frac{I_{OUT}}{f_{SW}\times C_{IN}}\times\frac{V_{OUT}}{V_{IN}}\times(1-\frac{V_{OUT}}{V_{IN}}) \quad (6)$$

The worst-case scenario occurs at V_{IN} = 2V_{OUT}, calculated with Equation (7):

$$\Delta V_{IN}=\frac{1}{4}\times\frac{I_{OUT}}{f_{SW}\times C_{IN}} \quad (7)$$

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. It is recommended to use ceramic or POSCAP capacitors.

The output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (8)$$

With ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f^2_{SW} \times C_{OUT} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

With POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (10)$$

Selecting a larger output capacitor provides faster load transient response. However, the maximum output capacitor limit should be also considered when designing for application. If the output capacitor value is too high, the output voltage cannot reach the desired value during the SS time, and the capacitor fails to regulate. The maximum output capacitor value (C_{O_MAX}) can be estimated with Equation (11):

$$C_{O\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times t_{SS} / V_{OUT} \quad (11)$$

Where I_{LIM_AVG} is the average start-up current during the soft-start period, and t_{SS} is the SS time.

Design Example

Table 1 shows a design example following the application guidelines for the provided specifications.

Table 1: Design Example

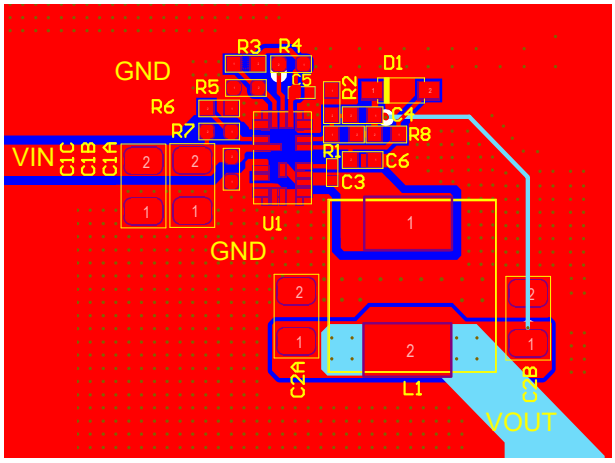
V_{IN}	12V to 100V
V_{OUT}	12V/2A
f_{SW}	400kHz

Figure 6 and Figure 7 shows the detailed application schematics. For the typical performance and circuit waveforms, see the Typical Performance Characteristics section. For more device applications, refer to the related evaluation board datasheet.

PCB Layout Guidelines

Efficient layout is critical for stable operation. For the best results, refer to Figure 5 and follow the guidelines below:

1. Place the high-current paths (GND, VIN, and SW) as close to the device as possible using short, direct, and wide traces.
2. Place the input capacitor as close to the VIN and GND pins as possible.
3. Place the external feedback resistors close to the FB pin.
4. Keep the switching node (SW) short, and as far away from the feedback network as possible.
5. Connect NC Pin to GND and place intensive vias next to the GND and NC Pin for better thermal performance.



●Top Layer ●Bottom Layer ●inner Layer

Figure 5: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

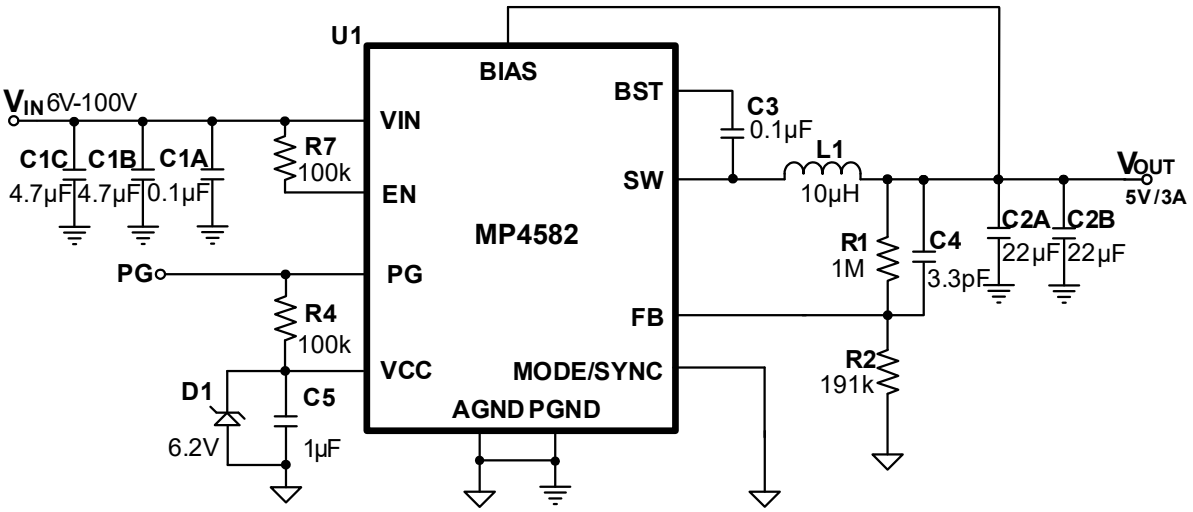


Figure 6: 5V Output Typical Application Circuit

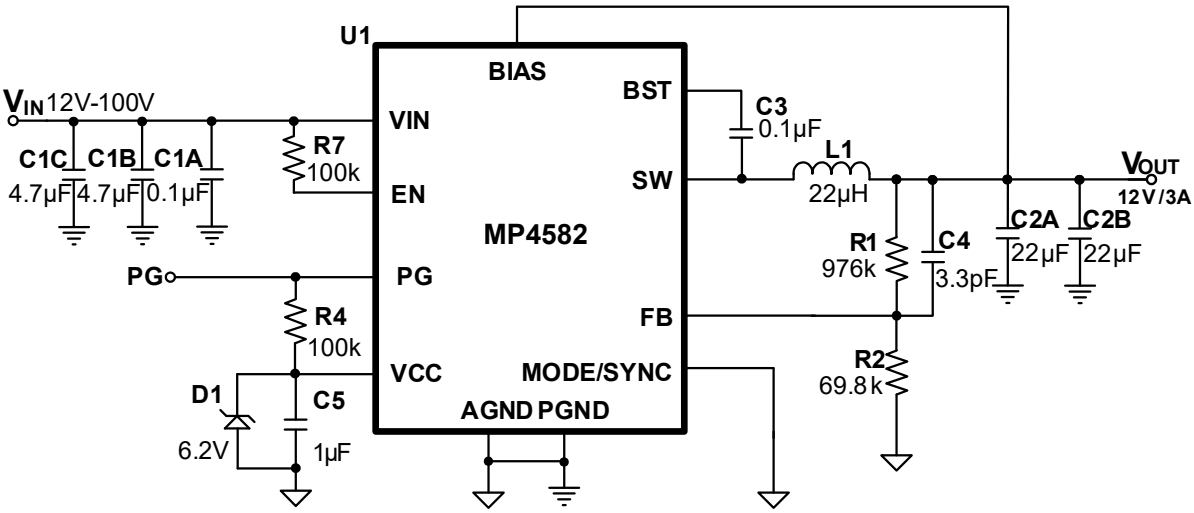
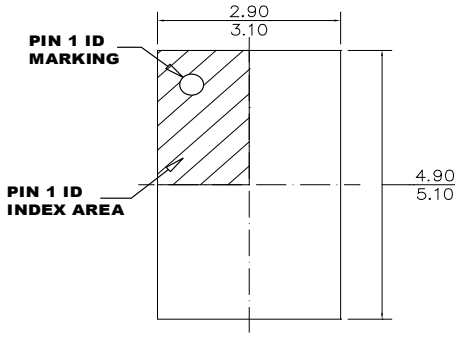


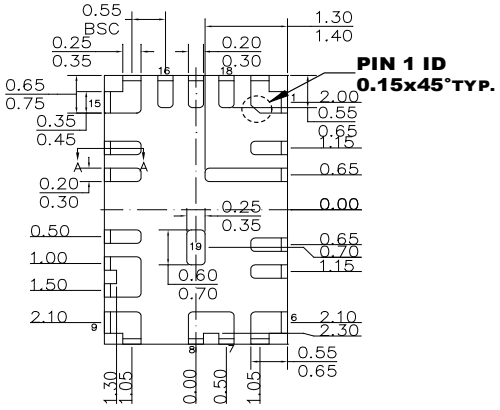
Figure 7:12V Output Typical Application Circuit

PACKAGE INFORMATION

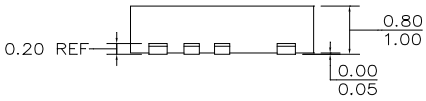
QFN-19 (3mmx5mm)



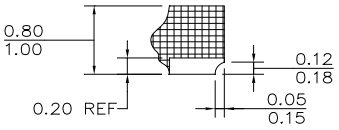
TOP VIEW



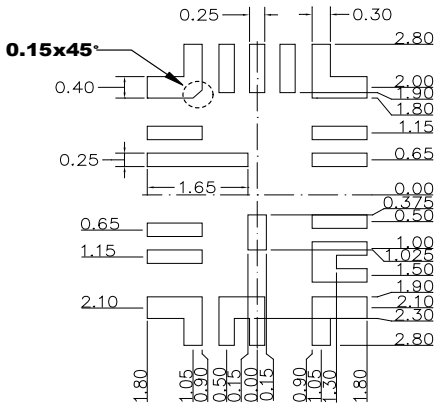
BOTTOM VIEW



SIDE VIEW



SECTION A-A

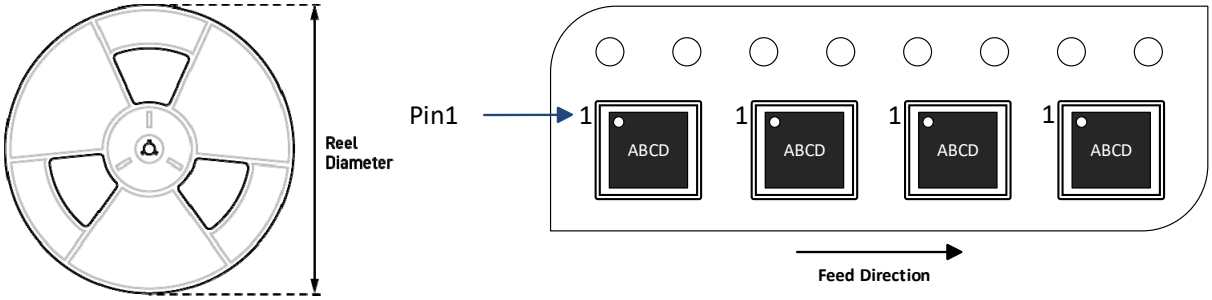


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP4582GQVE-Z	QFN-19 (3mmx5mm)	5000	N/A	N/A	13 in.	12 mm	8 mm