MP6600L

35V, 1.5A Stepper Motor Driver with Internal Current Sense

DESCRIPTION

The MP6600L is a stepper motor driver with current regulation and a built-in translator. Current sensing is internal and does not require external sense resistors. With high integration and a small package size, the MP6600L is a space-saving, cost-effective solution for bipolar stepper motor drives.

The device operates with a supply voltage up to 35V and can deliver motor currents up to 1.5A based on PCB design and thermal conditions. The MP6600L can operate a bipolar stepper motor in full-, half-, quarter-, or eighth-step mode. Internal safety features include over-current protection (OCP), input over-voltage protection (OVP), under-voltage lockout (UVLO), and thermal shutdown.

The MP6600L is available in a QFN-24 (4mmx4mm) package.

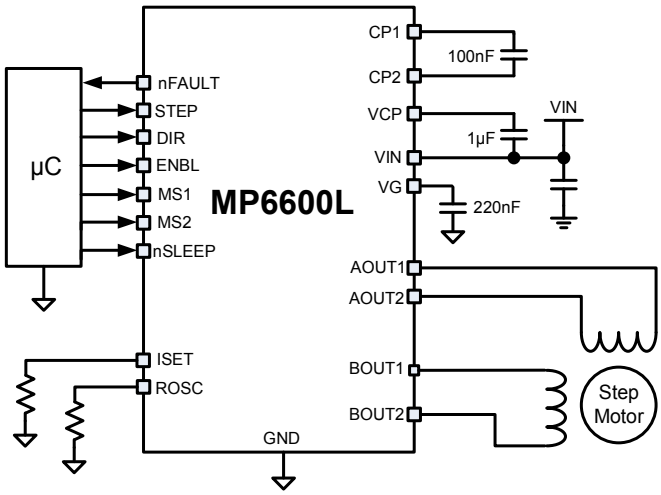
FEATURES

- Wide 4.5V to 35V Input Voltage Range
- Two Internal Full-Bridge Drivers
- Internal Current Sensing and Regulation
- Low On Resistance (195mΩ HS-FET, 170mΩ LS-FET)
- No Control Power Supply Required
- Simple Logic Interface
- 3.3V and 5V Compatible Logic Supply
- Step Modes from Full Step to Eighth-Step
- 1.5A Output Current
- Automatic Current Decay
- Over-Current Protection (OCP)
- Input Over-Voltage Protection (OVP)
- Thermal Shutdown and Under-Voltage Lockout (UVLO) Protection
- Fault Indication Output
- Available in a QFN-24 (4mmx4mm) Package

APPLICATIONS

- Bipolar Stepper Motors
- Printers

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6600LGR	QFN-24 (4mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix –Z (e.g. MP6600LGR–Z).

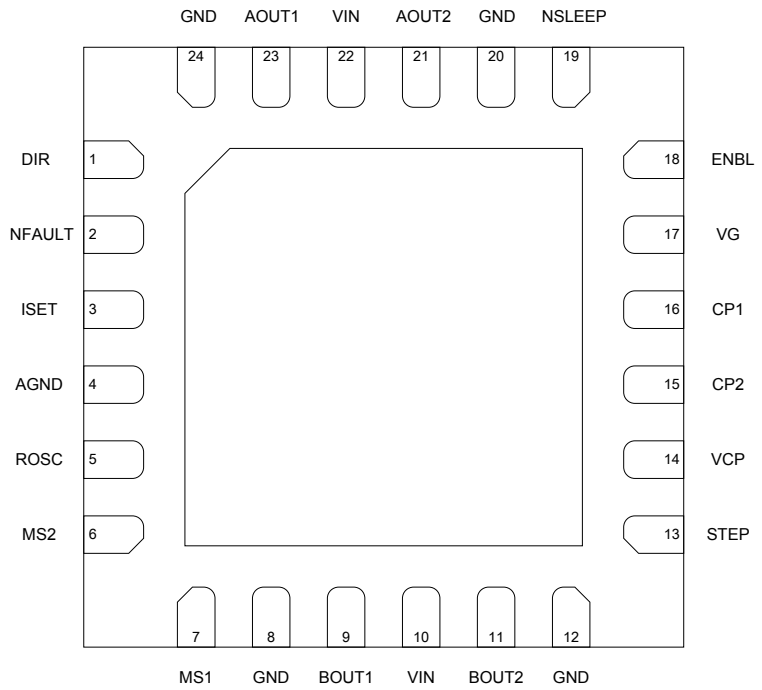
TOP MARKING

MPSYWW
M6600L
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
M6600L: Part number
LLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-24 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	DIR	**Direction input.** DIR has an internal pull-down resistor.
2	nFAULT	**Fault indication.** nFAULT is an open-drain output. Drive nFAULT to logic low when there is a fault condition (e.g. OCP, OTP, OVP).
3	ISET	**Current set programming.** Place a resistor from ISET to ground to set the current through the motor.
4	AGND	**Analog ground.**
5	ROSC	**Constant-off-time programming.** A resistor from ROSC to ground sets the PWM off time.
6	MS2	**Mode selection.** MS1 and MS2 set the step mode (full-, half-, quarter-, or eighth- step). MS1 and MS2 have an internal pull-down resistor.
7	MS1	
8, 12, 20, 24, EP	GND	**Power ground.**
9	BOUT1	**Bridge B output terminal 1.**
10, 22	VIN	**Input supply voltage.** Both VIN pins must be connected to the same supply. Decouple VIN to ground with a minimum 100nF ceramic capacitor.
11	BOUT2	**Bridge B output terminal 2.**
13	STEP	**Step input.** The rising edge sequences the translator and advances the motor by one increment. STEP has an internal pull-down resistor.
14	VCP	**Charge pump output.** Connect a 1μF, 16V, X7R ceramic capacitor from VCP to VIN.
15	CP2	**Charge pump capacitor.** Connect a 100nF, X7R ceramic capacitor rated for at least the VIN voltage between these terminals.
16	CP1	
17	VG	**Low-side MOSFETs gate drive voltage.** Connect a 220nF, 16V, X7R ceramic capacitor from VG to ground.
18	ENBL	**Enable input.** Drive ENBL to logic low to disable the bridge outputs and translator operation; drive it to logic high to enable these features. ENBL has an internal pull-down resistor.
19	nSLEEP	**Sleep mode input.** Drive nSLEEP to logic high to enable normal operation. nSLEEP has an internal pull-down resistor.
21	AOUT2	**Bridge A output terminal 2.**
23	AOUT1	**Bridge A output terminal 1.**

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) ..... -0.3V to +40V
xOUTx voltage ($V_{A/BOUT1/2}$) ..... -0.7V to +40V
VCP, CP2 ..... V_{IN} to V_{IN} + 6.5V
All other pins to AGND ..... -0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2) 2.9W
Storage temperature ..... -55°C to +150°C
Junction temperature ..... 150°C
Lead temperature (solder) ..... 260°C

ESD Rating

Human body model (HBM) ..... ±2kV
Charged device model (CDM) ..... ±2kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 4.5V to 35V
Output current ($I_{A/BOUT}$) ..... ±1.5A
Operating junction temp (T_J) ..... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-24 (4mmx4mm)	42	9 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}		4.5	24	35	V
Quiescent current	I_Q	V_{IN} = 24V, ENBL = 1, nSLEEP = 1, with no load		1.5	5	mA
	I_{SLEEP}	V_{IN} = 24V, nSLEEP = 0			1	µA
Internal MOSFETs						
Output on resistance	R_{HS}	V_{IN} = 24V, I_{OUT} = 1A, T_J = 25°C		0.195	0.3	Ω
		V_{IN} = 24V, I_{OUT} = 1A, T_J = 85°C		0.25		Ω
	R_{LS}	V_{IN} = 24V, I_{OUT} = 1A, T_J = 25°C		0.17	0.3	Ω
		V_{IN} = 24V, I_{OUT} = 1A, T_J = 85°C		0.25		Ω
Body diode forward voltage	V_F	I_{OUT} = 1.5A			1.1	V
Control Logic						
Input logic low threshold	V_{IL}				0.8	V
Input logic high threshold	V_{IH}		2.1			V
Logic input current	$I_{IN(H)}$	V_{IH} = 5V			20	µA
	$I_{IN(L)}$	V_{IL} = 0.8V			5	µA
Internal pull-down resistance	R_{PD}			500		kΩ
nFAULT Outputs (Open-Drain Outputs)						
Output low voltage	V_{OL}	I_O = 5mA			0.5	V
Output high leakage current	I_{OH}	V_O = 3.3V			1	µA
Protection Circuit						
UVLO rising threshold	V_{IN_RISE}		3.3	3.6	4	V
UVLO falling threshold	V_{IN_FALL}		3	3.3	3.7	V
Input OVP threshold	V_{OVP}		36	37.5	38.5	V
Input OVP hysteresis	ΔV_{OVP}			1900		mV
Over-current trip level	I_{OCP1}	Sinking	3.5	6	8.5	A
	I_{OCP2}	Sourcing	3.5	6	8.5	A
Over-current deglitch time (5)	t_{OCP}			1		µs
Thermal shutdown (5)	T_{TSD}			165		°C
Thermal shutdown hysteresis (5)	ΔT_{TSD}			15		°C
Current Regulation						
Constant-off-time	t_{OFF}	R_t = 200kΩ	19	23	26	µs
Peak current regulation level	I_{PEAK}	R_{ISET} = 71kΩ	0.95	1.0	1.05	A
ISET voltage	V_{ISET}		0.8	0.9	1	V
ISET current ratio	A_{ISET}	I_{ISET} / I_{OUT}	11	12.676	14	µA/A
Blanking time (5)	t_{BLANK}			2		µs
Current trip accuracy	ΔI_{TRIP}	R_{ISET} = 71kΩ, 71% to 100%	-5		+5	%
		R_{ISET} = 71kΩ, 38% to 67%	-9		+9	%
		R_{ISET} = 71kΩ, <34%	-12		+12	%

Note:

5) Guaranteed by design.

TIMING CHARACTERISTICS

V_{IN} = 24V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
STEP high time	t1		1			µs
STEP low time	t2		1			µs
Set-up time MSx, DIR to STEP rising	t3		200			ns
Hold time STEP rising to MSx, DIR change	t4		200			ns

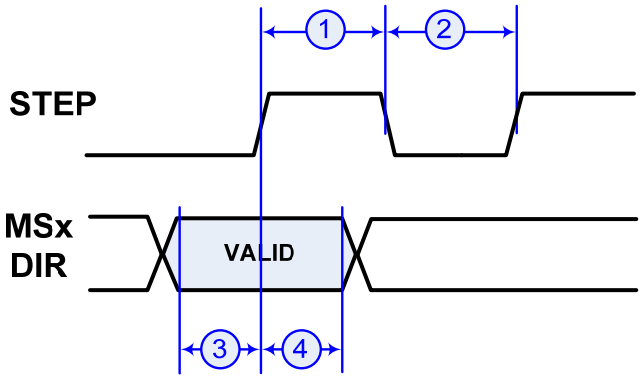
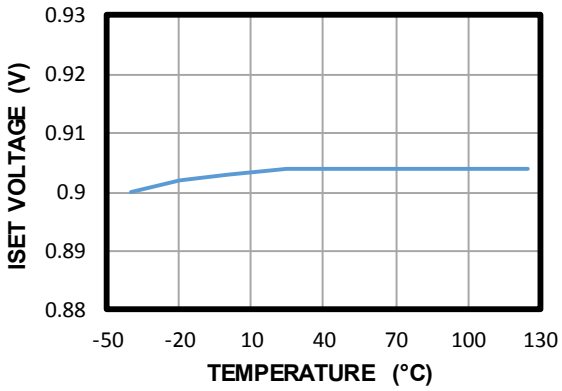


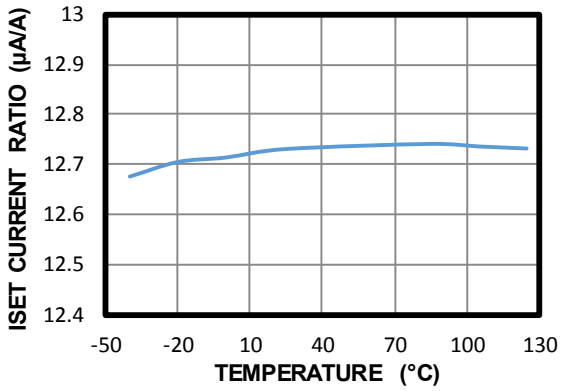
Figure 1: STEP Timing Diagram

TYPICAL CHARACTERISTICS

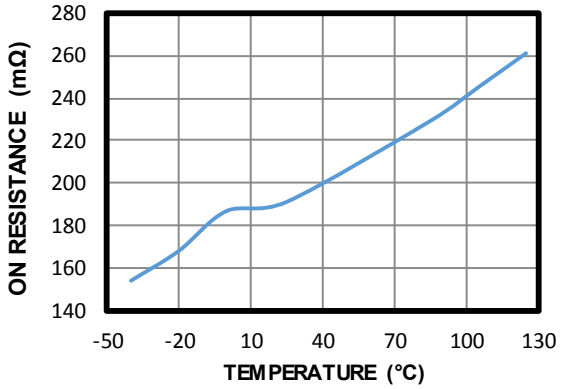
ISET Voltage vs. Temperature



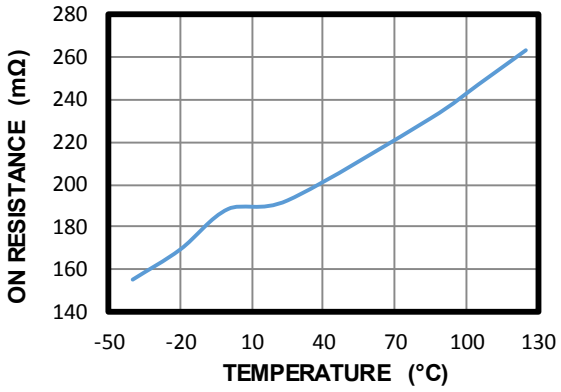
ISET Current Ratio vs. Temperature



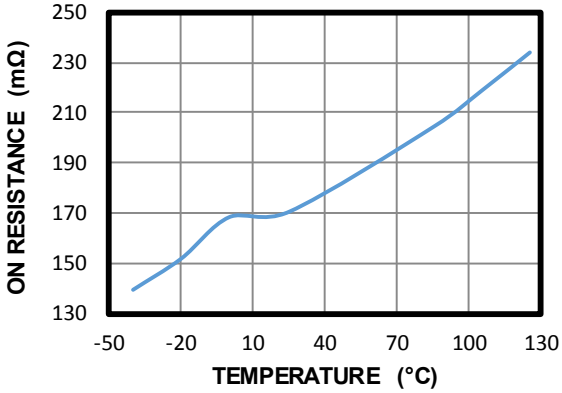
Bridge A HS-FET On Resistance vs. Temperature
V_{IN} = 24V, I_{OUT} = 1A



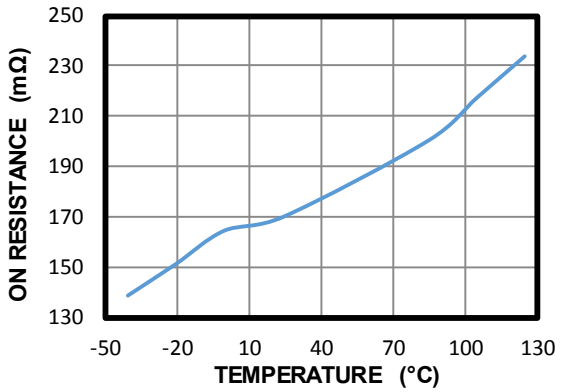
Bridge B HS-FET On Resistance vs. Temperature
V_{IN} = 24V, I_{OUT} = 1A



Bridge A LS-FET On Resistance vs. Temperature
V_{IN} = 24V, I_{OUT} = 1A

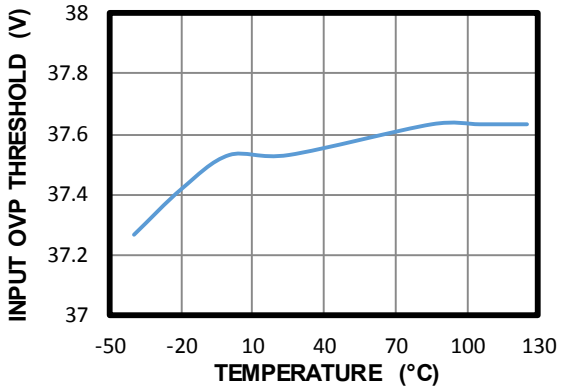


Bridge B LS-FET On Resistance vs. Temperature
V_{IN} = 24V, I_{OUT} = 1A



TYPICAL CHARACTERISTICS *(continued)*

Input OVP Threshold vs. Temperature

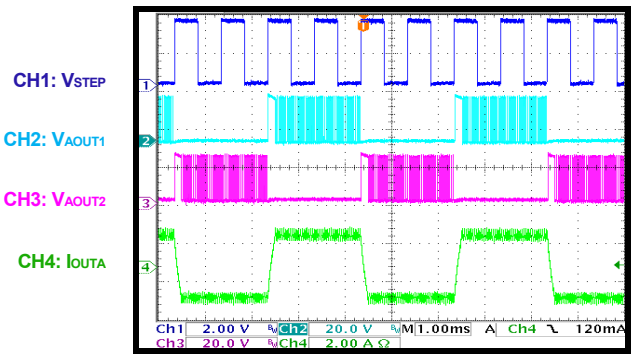


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, f_{STEP} = 1kHz, T_A = 25°C, resistor and inductor load: R = 3.3Ω, L = 1.5mH/channel, unless otherwise noted.

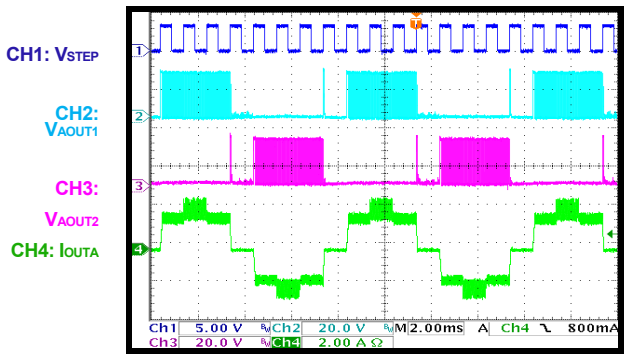
Steady State

I_{OUT} = 1A, full step



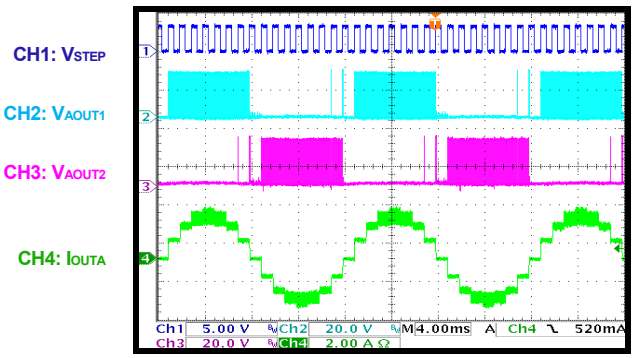
Steady State

I_{OUT} = 1.5A, Half-step



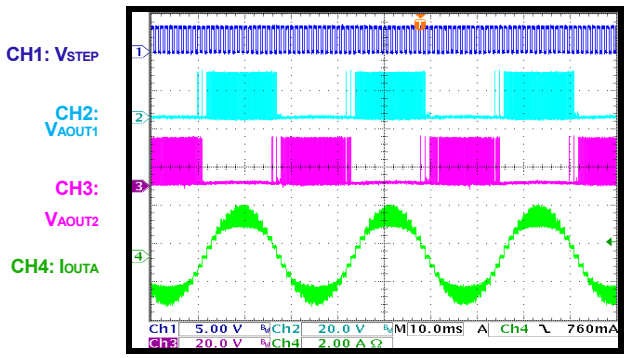
Steady State

I_{OUT} = 1.5A, Quarter-step



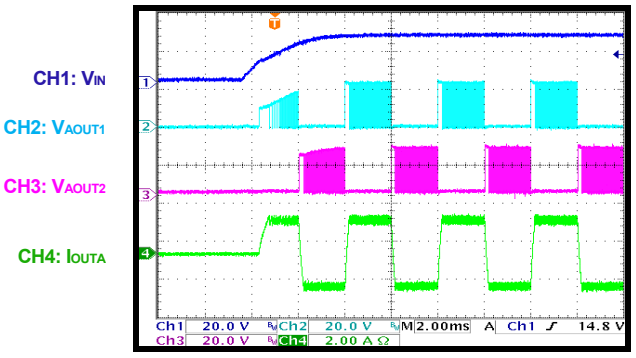
Steady State

I_{OUT} = 1.5A, Eighth-step



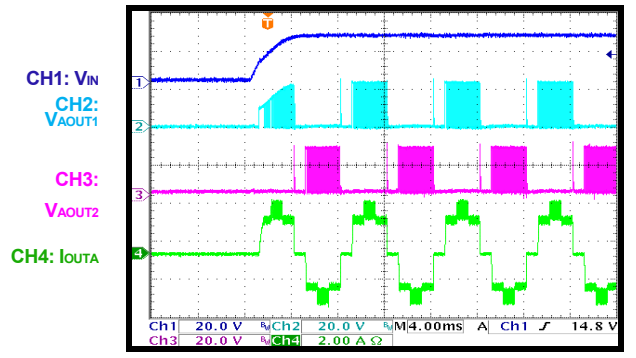
Power Ramp-Up

I_{OUT} = 1A, full step



Power Ramp-Up

I_{OUT} = 1.5A, Half-step

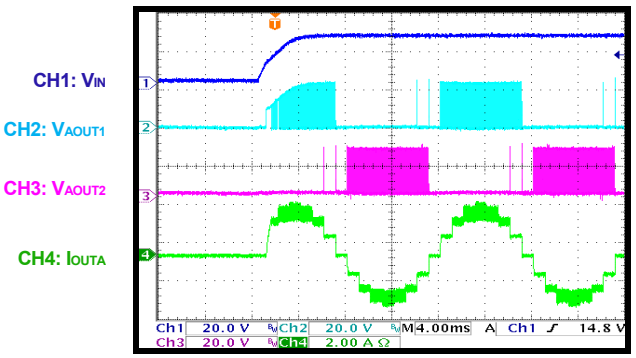


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, f_{STEP} = 1kHz, T_A = 25°C, resistor and inductor load: R = 3.3Ω, L = 1.5mH/channel, unless otherwise noted.

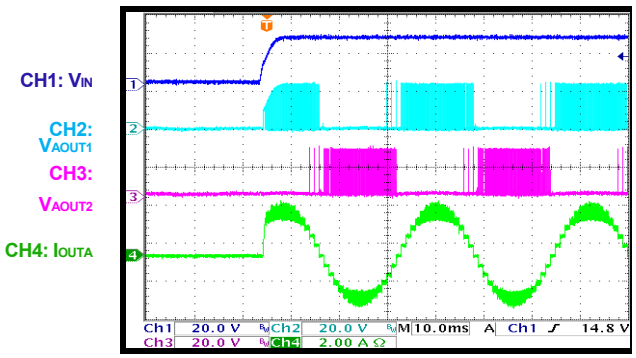
Power Ramp-Up

I_{OUT} = 1.5A, Quarter-step



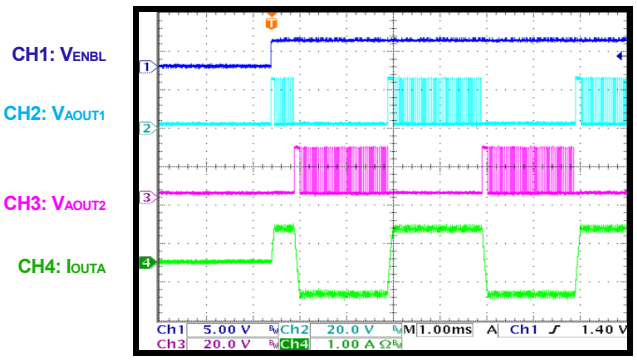
Power Ramp-Up

I_{OUT} = 1.5A, Eighth-step



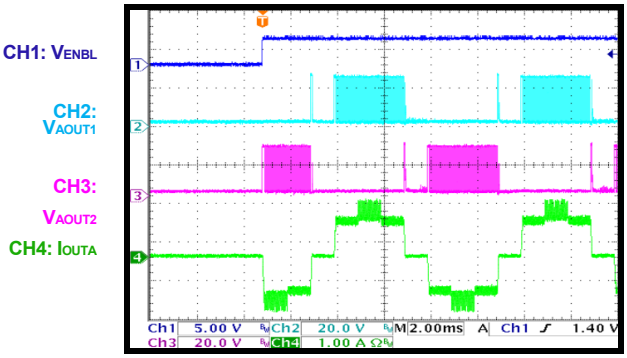
Enable

I_{OUT} = 1A, full step



Enable

I_{OUT} = 1.5A, Half-step



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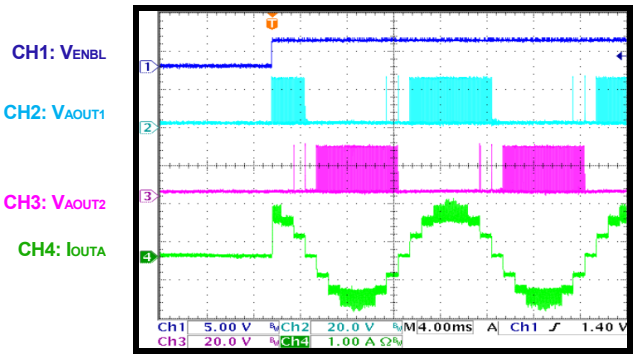
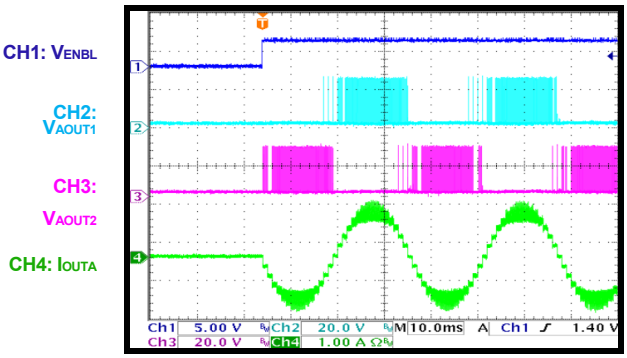


Enable

I_{OUT} = 1.5A, Eighth-step

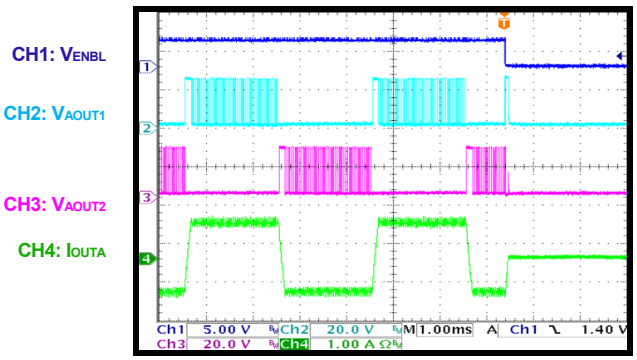


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, f_{STEP} = 1kHz, T_A = 25°C, resistor and inductor load: R = 3.3Ω, L = 1.5mH/channel, unless otherwise noted.

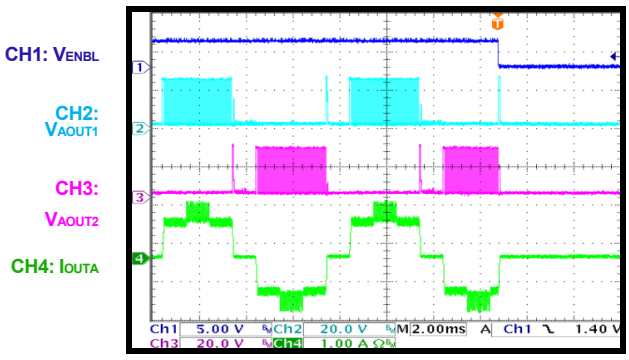
Disable

I_{OUT} = 1A, full step



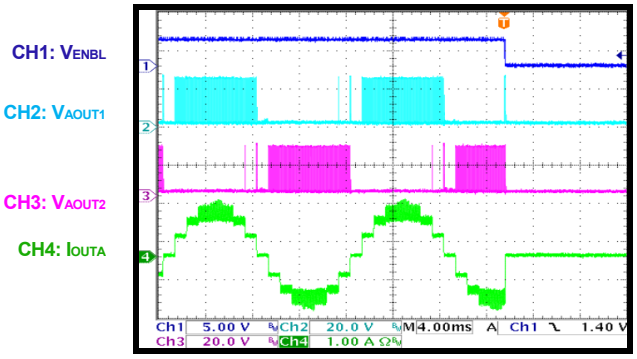
Disable

I_{OUT} = 1.5A, Half-step



Disable

I_{OUT} = 1.5A, Quarter-step



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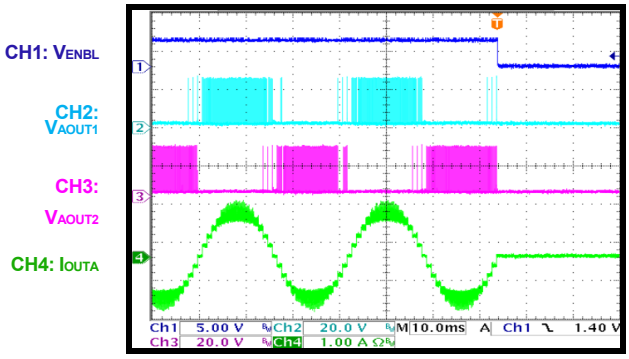

FUNCTIONAL BLOCK DIAGRAM

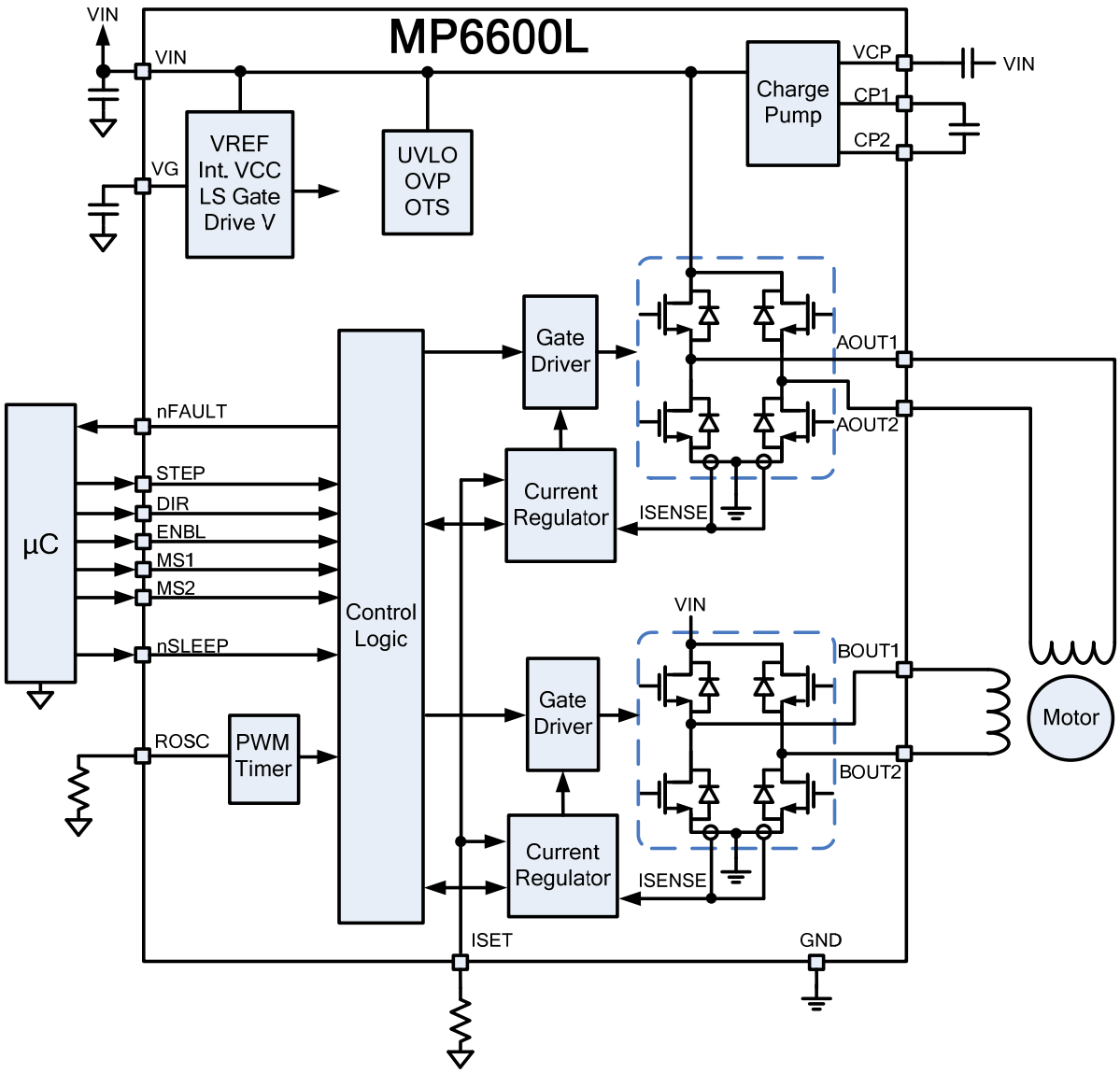

Figure 2: Functional Block Diagram

OPERATION

The MP6600L is a bipolar stepper motor driver that integrates eight N-channel power MOSFETs. These FETs are arranged as two full bridges that each have a current capability of 1.5A. The MP6600L operates over a wide 4.5V to 35V voltage supply range.

The device is designed to operate bipolar stepper motors in full-, half-, quarter-, and eighth-step modes. At each step, the current of each full bridge is set by the output voltage of a DAC, which is controlled by the output of the translator.

The currents in each of the two outputs are regulated with programmable constant-off-time (COT) pulse-width modulation (PWM) control. The MP6600L does not require external sense resistors because it integrates internal current sensing.

Stepping

The motor moves step by step by applying a series of pulses to the STEP input. A rising edge on STEP sequences the translator and advances the motor by one increment. The translator controls the input to the DACs and the direction of current flow in each winding. The amplitude of the increment (step size) is determined by the state of the MS1 and MS2 inputs (see Table 1).

The state of DIR determines the direction of the stepper motor's rotation.

The minimum STEP pulse width is 1µs. The logic control inputs (MSx and DIR) require at least 200ns of set-up time and hold time to the rising edge of the STEP input (see Figure 3).

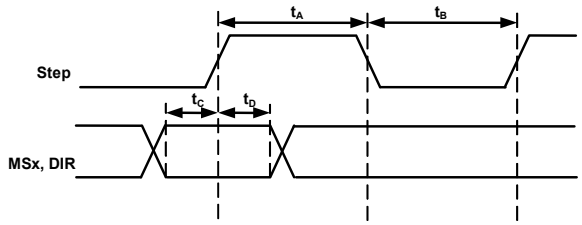

Figure 3: STEP Timing Diagram

Programmable Constant-Off-Time Current Control

The motor current is regulated by a programmable constant-off-time (COT) PWM current control circuit. Initially, a diagonal pair of MOSFETs turns on and drives the current through the motor winding. The current increases in the motor winding, which is sensed by an internal current-sense circuit. During the initial blanking time (t_{BLANK}), the high-side MOSFET (HS-FET) turns on regardless of current-limit detection.

When the current reaches the current trip threshold, the internal current comparator either shuts off the HS-FET so the winding inductance current freewheels through the two low-side MOSFETs (LS-FETs) in slow decay, or it turns on another diagonal pair of MOSFETs, so the current flows back to the input in fast decay mode. The current continues decreasing for the constant-off-time duration unless a zero current level is detected. Afterward, the HS-FET is enabled to increase the winding current again. Then the cycle repeats.

The off time (t_{OFF}) is determined by an external resistor (R_{OSC}). t_{OFF} can be estimated with Equation (1):

$$t_{OFF}(ns) = 115 \times R_{OSC}(k\Omega) \quad (1)$$

The full-scale (100%) regulation current can be calculated with Equation (2):

$$I_{MAX} = 71k\Omega / R_{ISET} \quad (2)$$

The DAC output reduces the trip current in precise steps. Calculate the trip current (I_{TRIP}) with Equation (3):

$$I_{TRIP} = \%I_{TRIP} \times I_{MAX} \quad (3)$$

See Table 2 on page 16 for the values of $\%I_{TRIP}$ at each step.

Blanking Time

There is usually a current spike during the switching transition due to the body diode's reverse recovery current and the distributed winding capacitance of the motor. This current spike requires filtering to prevent it from erroneously shutting down the HS-FET.

After the PWM cycle begins, the output of the current-sense comparator is ignored for the fixed blanking time. This blanking time results in a minimum on time for the PWM cycle.

Automatic Decay Mode

The MP6600L uses an automatic decay mode to provide accurate current regulation.

Initially, slow decay is used. If the current exceeds the I_{TRIP} threshold at the end of the fixed off time, fast decay mode is initiated by reversing the state of the H-bridge outputs.

Once the current level drops below the I_{TRIP} threshold during this fast decay period, slow decay is engaged again for another fixed off time. After the completion of this second fixed off time, a new PWM cycle begins.

Figure 4 shows the automatic decay mode operation during a current reduction as a result of a step input.

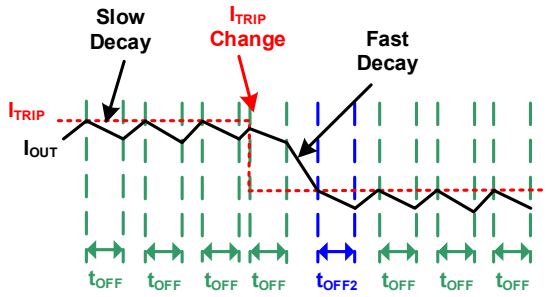

Figure 4: Slow Decay During t_{OFF}, unless $I_{OUT} > I_{TRIP}$ at the end of t_{OFF}

In the case of specifically high voltage and low inductance, or the regulation of very small currents, the minimum on time of the PWM cycle (set by the blanking time described above) can cause the current to rise quickly. In this case, both slow and fast decay are used (see Figure 5).

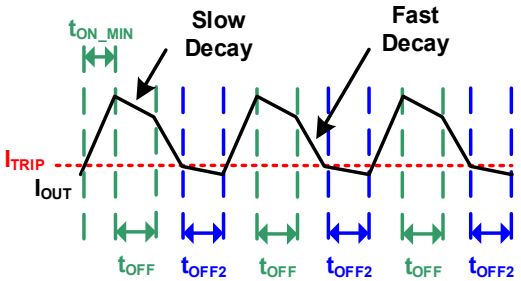

Figure 5: Current Regulation of Low Current/ Low Inductance

Microstep Selection (MS1, MS2)

The step mode is selected by applying logic high and low voltages to MS1 and MS2 (see Table 1). The MP6600L supports full, half-, quarter-, and eighth-step modes to progressively refine step resolution and control.

Table 1: Stepping Format

MS2	MS1	STEP Mode
L	L	Full step
L	H	Half-step
H	L	Quarter-step
H	H	Eighth-step

Full-step mode has four states with each motor winding driven by either 70.7% of the maximum positive current or 70.7% of the maximum negative current. This provides four steps per electrical rotation. Half-step mode creates eight steps per electrical rotation. Quarter- and eighth-step modes provide 16 and 32 steps per rotation, respectively.

Table 2 and Table 3 on pages 16 and 17, and Figure 6, Figure 7, Figure 8, and Figure 9 on pages 18 and 19 show the relative current level sequence for different settings of MSx.

The MSx pins have internal pull-down resistors.

nSLEEP, ENBL Operation

Driving nSLEEP low puts the device into a low-power sleep state. In this state, the gate drive charge pump is stopped, and all the internal circuits and H-bridge outputs are disabled. All inputs are ignored when nSLEEP is active low.

When the device wakes up from sleep mode, about 1ms must pass before a STEP command can be issued, which allows the internal circuitry to stabilize. nSLEEP has an internal pull-down resistor.

The ENBL pin controls the output drivers. When ENBL is high, the H-bridge outputs are enabled, and the rising edges on STEP are recognized. When ENBL is low, the H-bridge outputs are disabled, and the STEP input is ignored. ENBL has an internal pull-down resistor.

Fault Reporting

The MP6600L provides an nFAULT pin, which reports if a fault condition (e.g. OCP, OTP, or OVP) occurs. nFAULT is an open-drain output, and is driven low when a fault condition occurs. If the fault condition is removed, nFAULT is pulled high by an external pull-up resistor.

Over-Current Protection (OCP)

Over-current protection (OCP) circuitry limits the current through the MOSFETs by disabling the gate driver. If the over-current limit threshold is exceeded for longer than the over-current deglitch time, all MOSFETs in the H-bridge are disabled and nFAULT is driven low. The driver remains off until either nSLEEP is reset or VIN's power is cycled.

Over-current conditions on both high- and low-side devices (e.g. a short to ground, supply, or across the motor winding) result in an over-current shutdown. Note that OCP does not use the current-sense circuitry used for PWM current control.

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Over-Voltage Protection (OVP)

If V_{IN} exceeds the over-voltage protection (OVP) threshold, the H-bridge output is disabled and nFAULT is driven low. This protection is removed when V_{IN} drops below 36V.

Input Under-Voltage Lockout (UVLO) Protection

If at any time V_{IN} falls below the under-voltage lockout (UVLO) threshold voltage, all circuitry in the device is disabled and the internal logic is reset. Operation resumes when V_{IN} rises above the UVLO threshold.

Thermal Shutdown

If the die temperature exceeds safe limits, all MOSFETs in the H-bridge are disabled and nFAULT is driven low. Once the die temperature drops to a safe level, operation resumes automatically.

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MICROSTEPPING

Table 2: Relative Current Level Sequence (DIR=1)

Reset position is at step angle 45°

Eighth-Step #	Quarter-Step #	Half-Step #	Full Step #	Phase A Current %$I_{TRIP-LIMIT}$ (%)	Phase B Current %$I_{TRIP-LIMIT}$ (%)	Step Angle (°)
1	1	1		100.00	0.00	0.0
2				98.08	19.51	11.3
3	2			92.39	38.27	22.5
4				83.15	55.56	33.8
5	3	2	1	70.71	70.71	45.0
6				55.56	83.15	56.3
7	4			38.27	92.39	67.5
8				19.51	98.08	78.8
9	5	3		0.00	100.00	90.0
10				-19.51	98.08	101.3
11	6			-38.27	92.39	112.5
12				-55.56	83.15	123.8
13	7	4	2	-70.71	70.71	135.0
14				-83.15	55.56	146.3
15	8			-92.39	38.27	157.5
16				-98.08	19.51	168.8
17	9	5		-100.00	0.00	180.0
18				-98.08	-19.51	191.3
19	10			-92.39	-38.27	202.5
20				-83.15	-55.56	213.8
21	11	6	3	-70.71	-70.71	225.0
22				-55.56	-83.15	236.3
23	12			-38.27	-92.39	247.5
24				-19.51	-98.08	258.8
25	13	7		0.00	-100.00	270.0
26				19.51	-98.08	281.3
27	14			38.27	-92.39	292.5
28				55.56	-83.15	303.8
29	15	8	4	70.71	-70.71	315.0
30				83.15	-55.56	326.3
31	16			92.39	-38.27	337.5
32				98.08	-19.51	348.8

MICROSTEPPING *(continued)*

Table 3: Relative Current Level Sequence (DIR=0)

Reset position is at step angle 45°

Eighth-Step #	Quarter-Step #	Half-Step #	Full Step #	Phase A Current $\%I_{TRIP-LIMIT}$ (%)	Phase B Current $\%I_{TRIP-LIMIT}$ (%)	Step Angle (°)
1	1	1		100.00	0.00	0.0
2				98.08	-19.51	11.3
3	2			92.39	-38.27	22.5
4				83.15	-55.56	33.8
5	3	2	1	70.71	-70.71	45.0
6				55.56	-83.15	56.3
7	4			38.27	-92.39	67.5
8				19.51	-98.08	78.8
9	5	3		0.00	-100.00	90.0
10				-19.51	-98.08	101.3
11	6			-38.27	-92.39	112.5
12				-55.56	-83.15	123.8
13	7	4	2	-70.71	-70.71	135.0
14				-83.15	-55.56	146.3
15	8			-92.39	-38.27	157.5
16				-98.08	-19.51	168.8
17	9	5		-100.00	0.00	180.0
18				-98.08	19.51	191.3
19	10			-92.39	38.27	202.5
20				-83.15	55.56	213.8
21	11	6	3	-70.71	70.71	225.0
22				-55.56	83.15	236.3
23	12			-38.27	92.39	247.5
24				-19.51	98.08	258.8
25	13	7		0.00	100.00	270.0
26				19.51	98.08	281.3
27	14			38.27	92.39	292.5
28				55.56	83.15	303.8
29	15	8	4	70.71	70.71	315.0
30				83.15	55.56	326.3
31	16			92.39	38.27	337.5
32				98.08	19.51	348.8

MICROSTEPPING *(continued)*

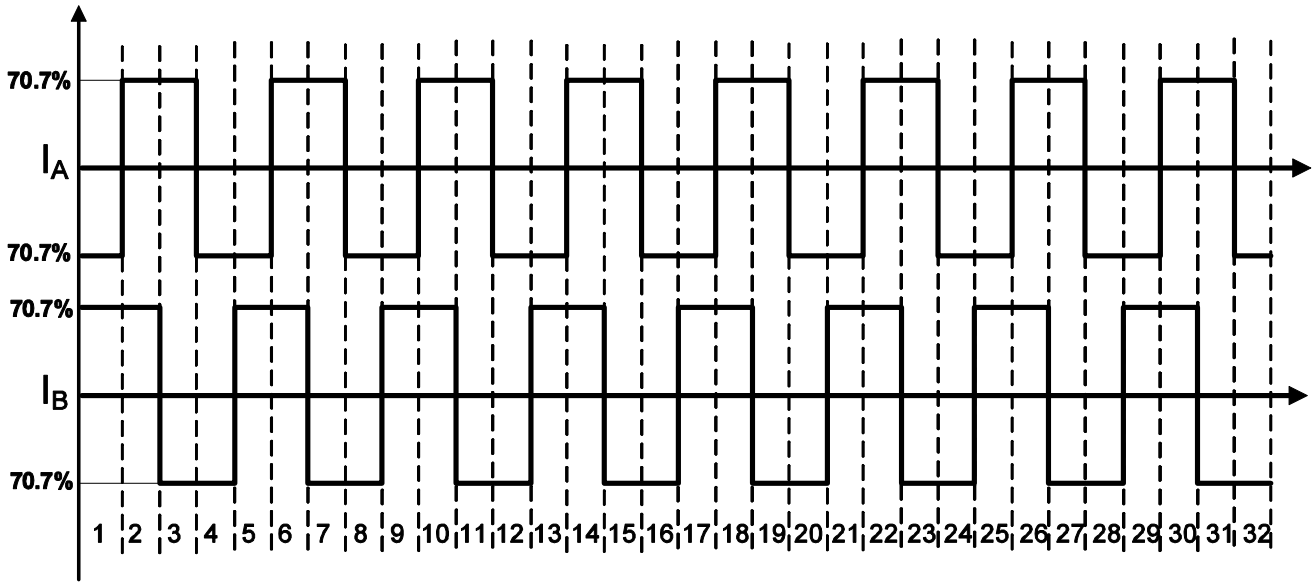


Figure 6: Full Step (4 Step Sequences, DIR = 0)

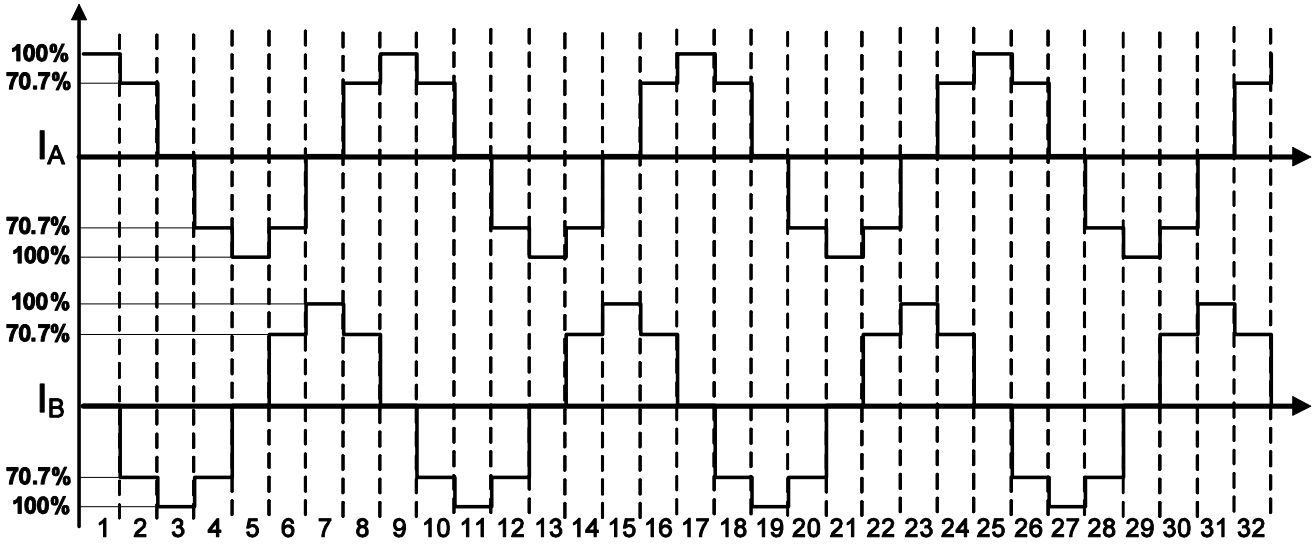


Figure 7: Half-Step (8 Step Sequences, DIR = 0)

MICROSTEPPING *(continued)*

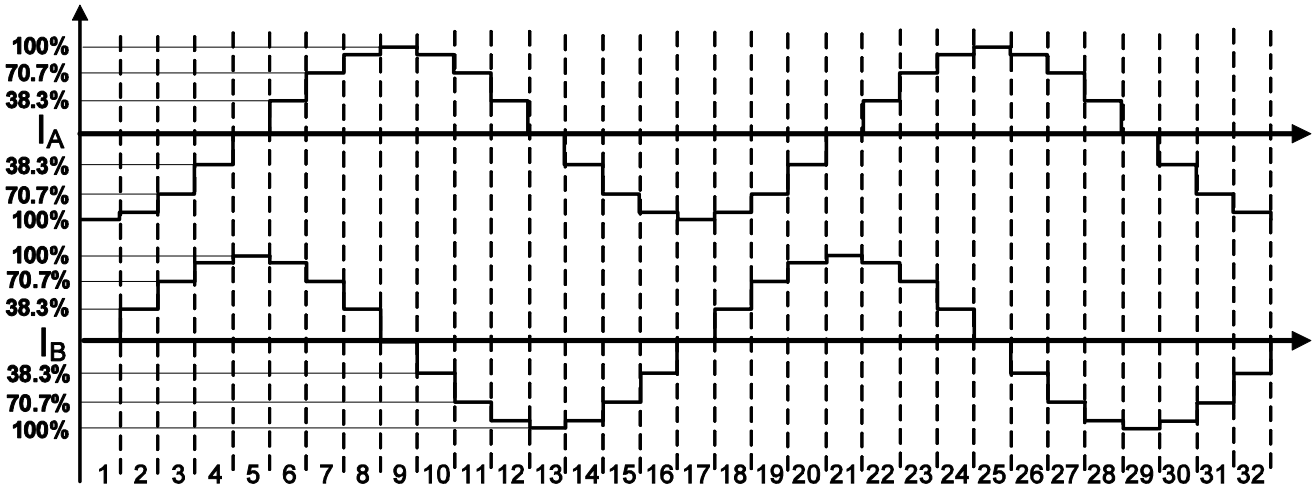


Figure 8: Quarter-Step (16 Step Sequences, DIR = 0)

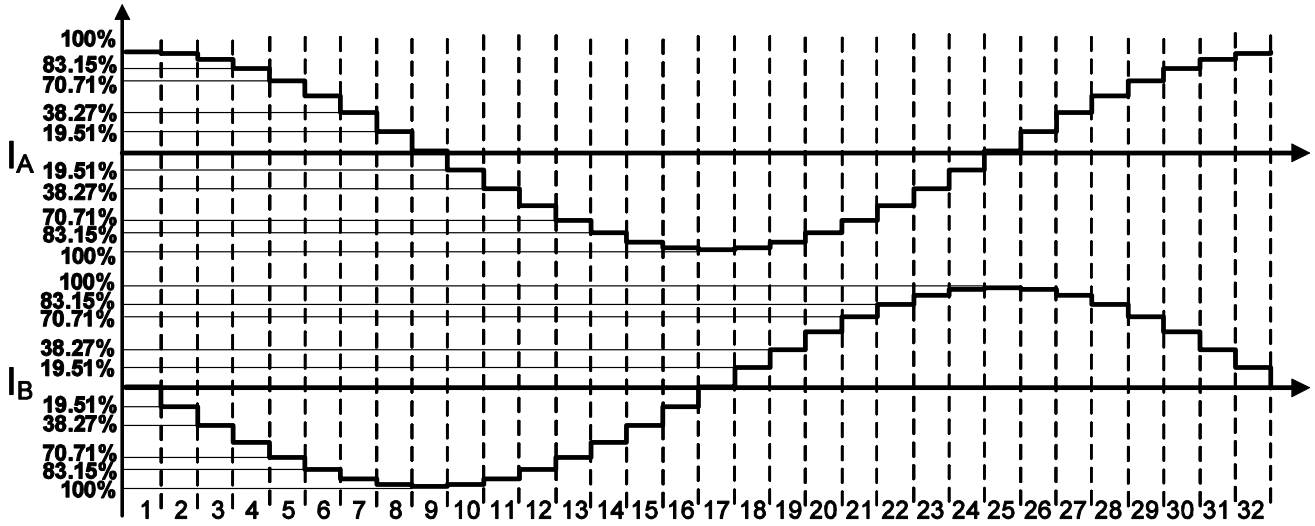
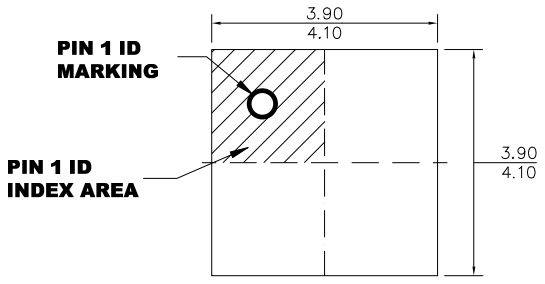


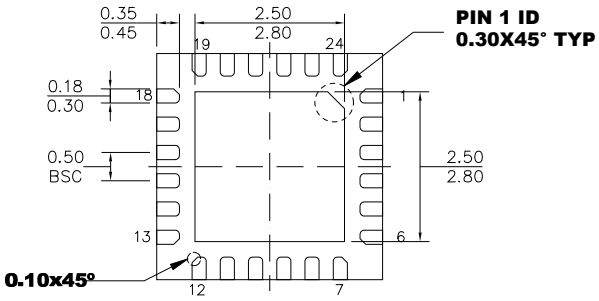
Figure 9: Eighth-Step (32 Step Sequences, DIR = 0)

PACKAGE INFORMATION

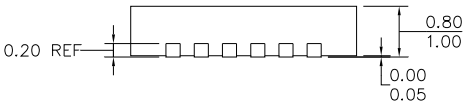
QFN-24 (4mmx4mm)



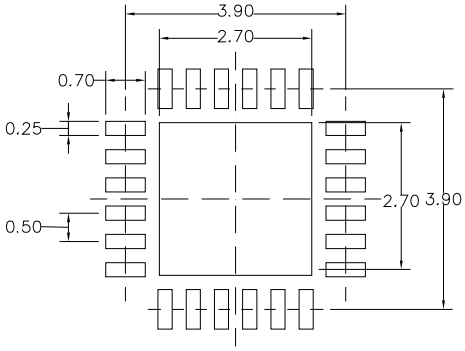
TOP VIEW



BOTTOM VIEW



SIDE VIEW

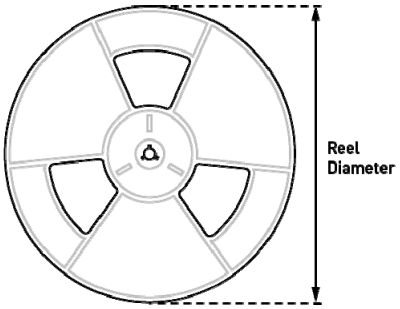


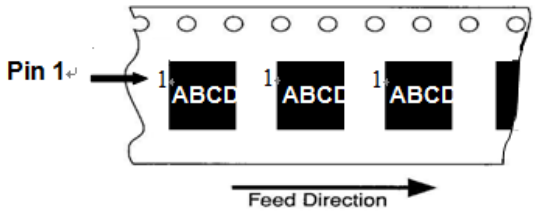
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6600LGR-Z	QFN-24 (4mmx4mm)	5000	N/A	13in	12mm	8mm