



The Future of Analog IC Technology®

# MP6601

## 35V, 2.5A, Stepper Motor Driver

### DESCRIPTION

The MP6601 is a stepper motor driver with parallel inputs and current regulation. Current sensing is internal and requires no external sense resistors. High integration and a small package size make the MP6601 a space-saving and cost-effective solution for bipolar stepper motor drives.

The MP6601 operates from a wide supply voltage of 4.5 - 35V and can deliver motor current up to 2.5A (depending on thermal conditions and the package). The MP6601 can operate a bipolar stepper motor in full-, half-, or quarter-step modes using internal 2-bit DACs.

Full protection features include over-current protection (OCP), input over-voltage protection (OVP), under-voltage lockout (UVLO), and thermal shutdown.

The MP6601 is available in QFN-24 (5mmx5mm) and TSSOP-28 EP packages.

### FEATURES

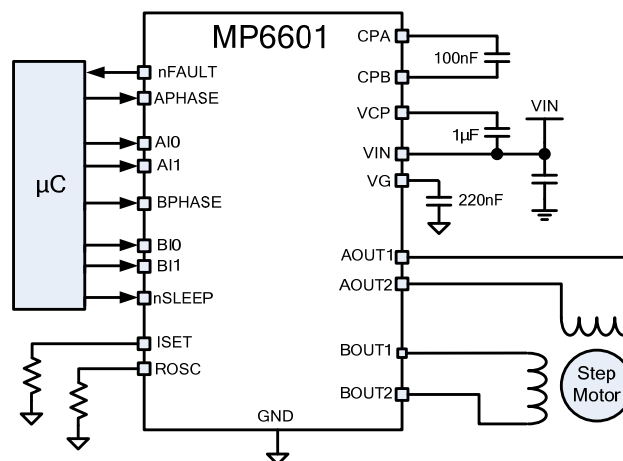
- Wide 4.5V to 35V Input Voltage Range
- Two Internal Full-Bridge Drivers
- Internal Current Sensing and Regulation
- Low On Resistance (HS: 170mΩ, LS: 150mΩ)
- No Control Power Supply Required
- Simple PHASE/I0/I1 Logic Interface
- 3.3V and 5V Compatible Logic Supply
- Step Modes from Full-Step to Quarter-Step
- 2.5A Output Current
- Automatic Current Decay
- Over-Current Protection (OCP)
- Input Over-Voltage Protection (OVP) Function
- Thermal Shutdown and Under-Voltage Lockout (UVLO) Protection
- Fault Indication Output
- Available in QFN-24 (5mmx5mm) and Thermally Enhanced TSSOP-28 EP Packages

### APPLICATIONS

- Bipolar Stepper Motors
- Printers

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### TYPICAL APPLICATION



## ORDERING INFORMATION

Part Number*	Package	Top Marking
MP6601GU	QFN-24 (5mmx5mm)	See Below
MP6601GF	TSSOP-28 EP	See Below

\* For Tape & Reel, add suffix -Z (e.g.: MP6601GU-Z)

### TOP MARKING (MP6601GU)

**MPSYYWW**  
**MP6601**  
**LLLLLLL**

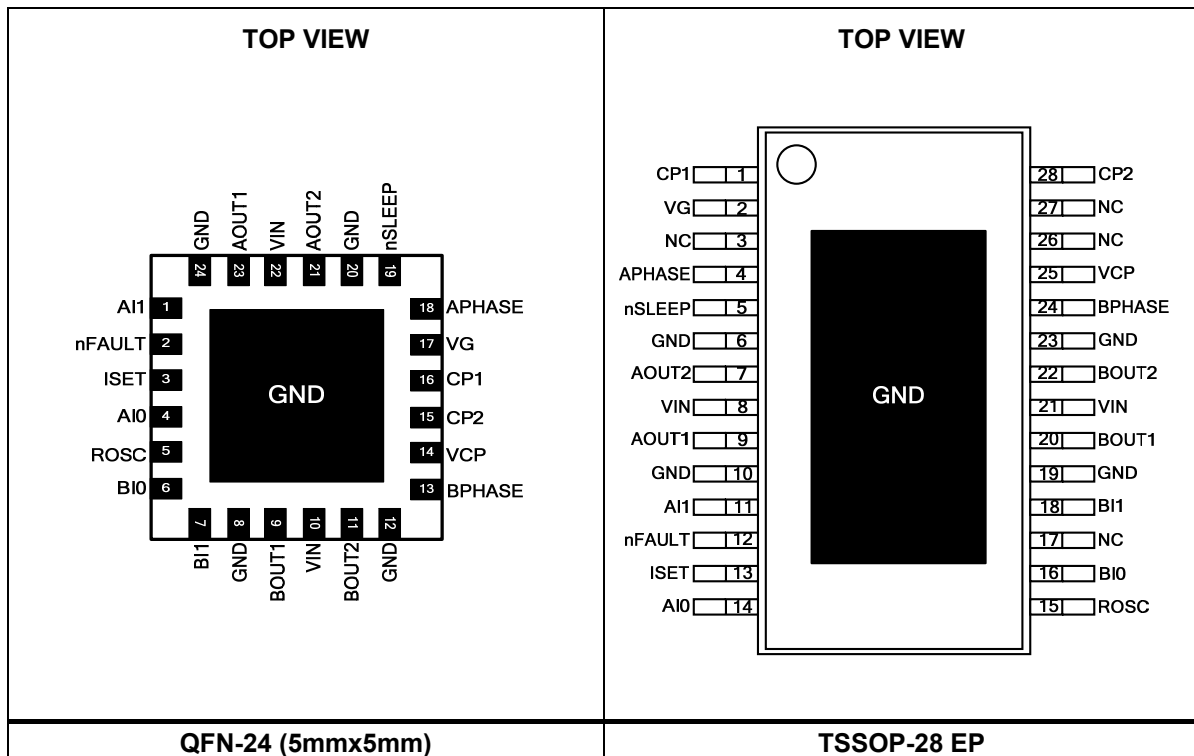
### TOP MARKING (MP6601GF)

**MPSYYWW**  
**MP6601**  
**LLLLLLLLL**

MPS: MPS prefix  
YY: Year code  
WW: Week code  
MP6601: Product code of MP6601GU  
LLLLLLL: Lot number

MPS: MPS prefix  
YY: Year code  
WW: Week code  
MP6601: Product code of MP6601GF  
LLLLLLLLL: Lot number

## PACKAGE REFERENCE



### ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

Supply voltage ( $V_{IN}$ )	-0.3V to 40V
xOUTx voltage ( $V_{A/OUT1/2}$ )	-0.7V to 40V
VCP, CPB	$V_{IN}$ to $V_{IN} + 6.5V$
ESD rating (HBD)	2kV
All other pins to AGND	-0.3V to 6.5V
Continuous power dissipation ( $T_A = +25^{\circ}C$ ) <sup>(2)</sup>	
QFN-24 (5mmx5mm)	3.5W
TSSOP-24 EP	3.9W
Storage temperature	-55°C to +150°C
Junction temperature	+150°C
Lead temperature (solder)	+260°C

### Recommended Operating Conditions <sup>(3)</sup>

Supply voltage ( $V_{IN}$ )	4.5V to 35V
Operating junction temp. ( $T_J$ )	-40°C to +125°C

### Thermal Resistance <sup>(4)</sup>

	$\theta_{JA}$	$\theta_{JC}$
QFN-24 (5mmx5mm)	36	8
TSSOP-28 EP	32	6

#### NOTES:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J$  (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 24V$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.

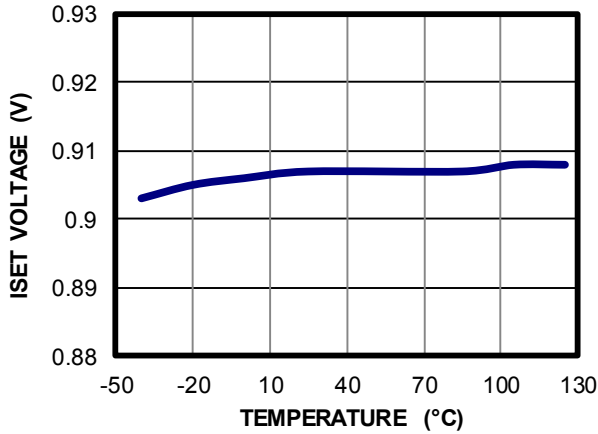
Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>Power Supply</b>						
Input supply voltage	$V_{IN}$		4.5	24	35	V
Quiescent current	$I_Q$	$V_{IN} = 24V$ , $nSLEEP = 1$ , with no load		1.5	5	mA
	$I_{SLEEP}$	$V_{IN} = 24V$ , $nSLEEP = 0$			1	$\mu A$
<b>Internal MOSFETs</b>						
Output on resistance	$R_{HS}$	$V_{IN} = 24V$ , $I_{OUT} = 1A$ , $T_J = 25^{\circ}C$		0.195	0.23	$\Omega$
		$V_{IN} = 24V$ , $I_{OUT} = 1A$ , $T_J = 85^{\circ}C$ <sup>(5)</sup>		0.25		$\Omega$
	$R_{LS}$	$V_{IN} = 24V$ , $I_{OUT} = 1A$ , $T_J = 25^{\circ}C$		0.17	0.22	$\Omega$
		$V_{IN} = 24V$ , $I_{OUT} = 1A$ , $T_J = 85^{\circ}C$ <sup>(5)</sup>		0.25		$\Omega$
Body diode forward voltage	$V_F$	$I_{OUT} = 1.5A$			1.1	V
<b>Control Logic</b>						
Input logic low threshold	$V_{IL}$				0.8	V
Input logic high threshold	$V_{IH}$		2.1			V
Logic input current	$I_{IN(H)}$	$V_{IH} = 5V$			20	$\mu A$
	$I_{IN(L)}$	$V_{IL} = 0.8V$			5	$\mu A$
Internal pull-down resistance	$R_{PD}$			500		k $\Omega$
<b>Home nFAULT Outputs (Open-Drain Outputs)</b>						
Output low voltage	$V_{OL}$	$I_O = 5mA$			0.5	V
Output high leakage current	$I_{OH}$	$V_O = 3.3V$			1	$\mu A$
<b>Protection Circuit</b>						
UVLO rising threshold	$V_{IN\_RISE}$			3.4	4.5	V
UVLO hysteresis	$V_{HYS}$			300		mV
Input OVP threshold	$V_{OVP}$		36	37.5	38.5	V
Input OVP hysteresis	$\Delta V_{OVP}$			1900		mV
Over-current trip level	$I_{OCP1}$	Sinking	3	6	8	A
	$I_{OCP2}$	Sourcing	3	6	8	A
Over-current deglitch time <sup>(5)</sup>	$t_{OCP}$			1		$\mu s$
Thermal shutdown <sup>(5)</sup>	$T_{TSD}$			165		$^{\circ}C$
Thermal shutdown hysteresis <sup>(5)</sup>	$\Delta T_{TSD}$			15		$^{\circ}C$
<b>Current Control</b>						
Constant off time	$t_{OFF}$	$R_t = 200k\Omega$	20	23	26	$\mu s$
Blanking time <sup>(5)</sup>	$t_{BLANK}$			2		$\mu s$
Peak current regulation level	$I_{PEAK}$	$R_{ISET} = 71k\Omega$	0.95	1.0	1.05	A
ISET voltage	$V_{ISET}$			0.9		V
ISET current ratio	$A_{ISET}$	$I_{ISET}/I_{OUT}$	11	12.676	14	$\mu A/A$
Current trip accuracy	$\Delta I_{TRIP}$	$R_{ISET} = 71k\Omega$ , 71 - 100%	-5		5	%
		$R_{ISET} = 71k\Omega$ , 38 - 67%	-10		10	%

**NOTE:**

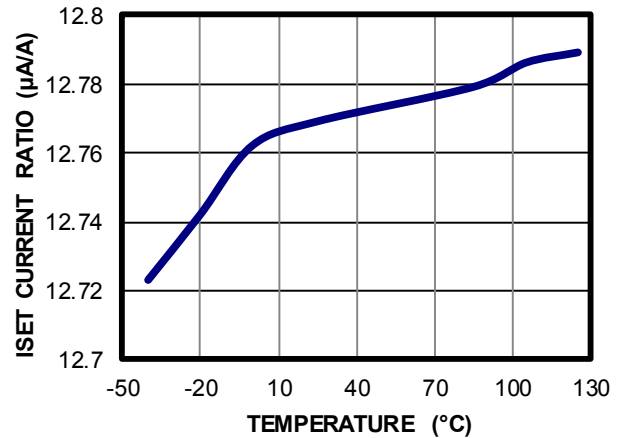
5) Guaranteed by design.

## TYPICAL CHARACTERISTICS

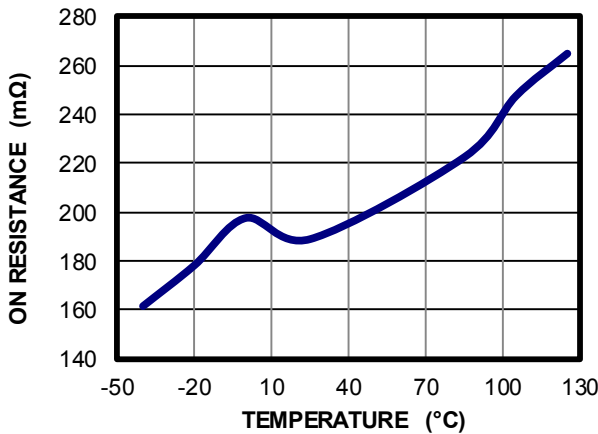
ISET Voltage vs. Temperature



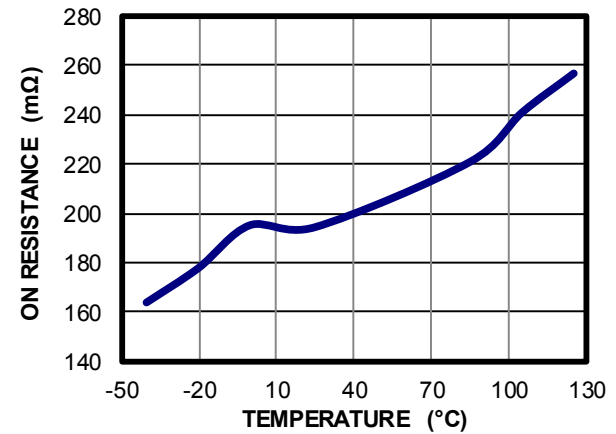
ISET Current Ratio vs. Temperature



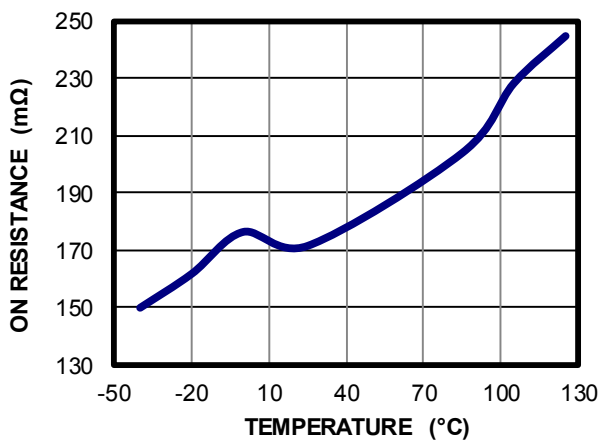
Bridge A HS On Resistance vs. Temperature



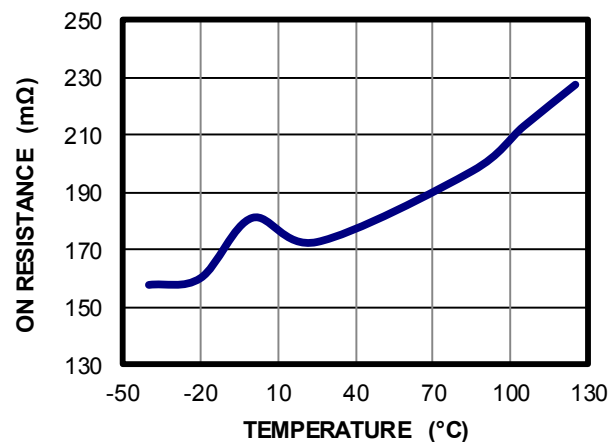
Bridge B HS On Resistance vs. Temperature



Bridge A LS On Resistance vs. Temperature

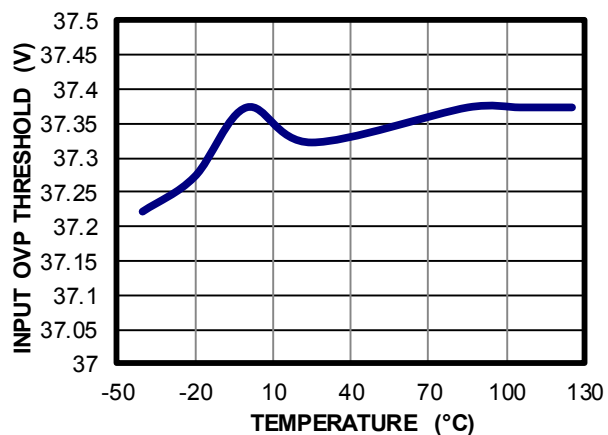


Bridge B LS On Resistance vs. Temperature



# TYPICAL CHARACTERISTICS *(continued)*

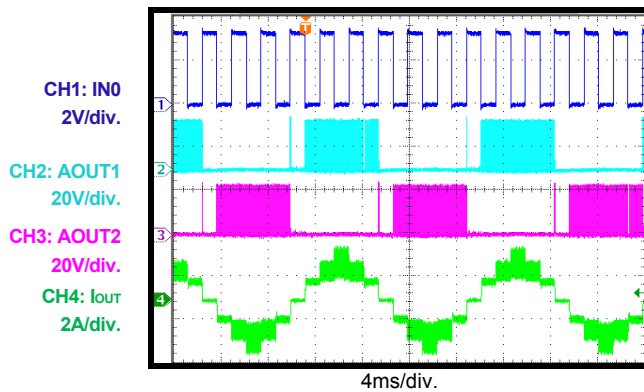
Input OVP Threshold vs.  
Temperature



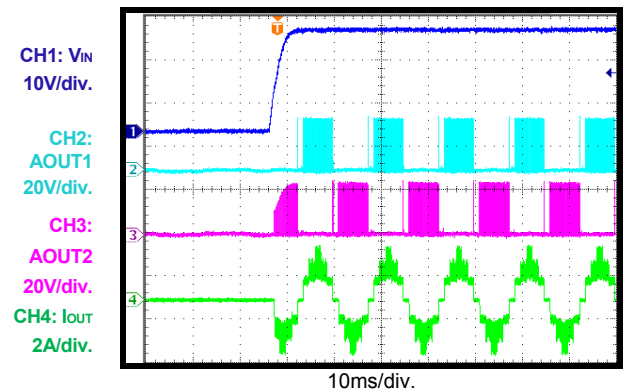
# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 24V$ ,  $I_{OUT} = 2.5A$ , 1/4-step,  $T_A = 25^{\circ}C$ , resistor + inductor load:  $R = 3.3\Omega$ ,  $L = 1.5mH/channel$ , unless otherwise noted.

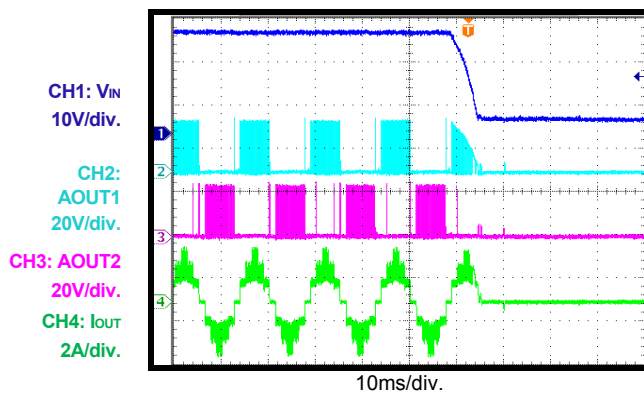
## Normal Operation



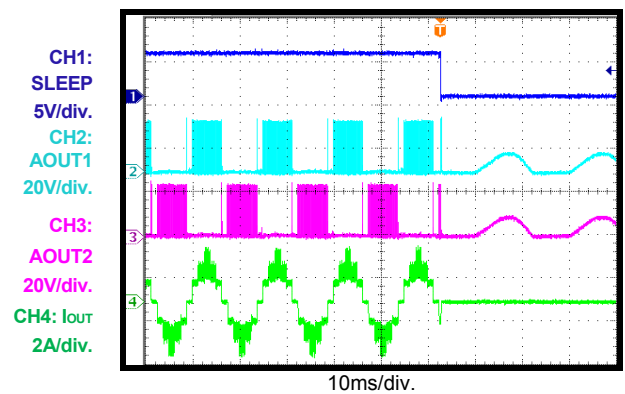
## VIN Power Start-Up



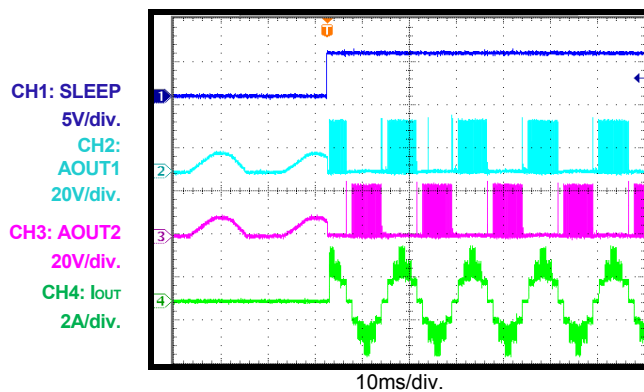
## VIN Power Shutdown



## Sleep Entry



## Sleep Recovery



## PIN FUNCTIONS

Pin # QFN	Pin # TSSOP	Name	Description
1	11	AI1	<b>Current-set inputs for phase A.</b>
2	12	nFAULT	<b>Fault indication.</b> nFAULT is an open-drain output. nFAULT is at logic low when a fault condition occurs (i.e.: OCP, OTP, OVP).
3	13	ISET	<b>Current set programming pin.</b> Connect a resistor from ISET to ground to set the current through the motor.
4	14	AI0	<b>Current-set inputs for phase A.</b>
5	15	ROSC	<b>Constant off time programming pin.</b> Connect a resistor from ROSC to ground to set the PWM off time.
6	16	BI0	<b>Current-set inputs for phase B.</b>
7	18	BI1	
8, 12, 20, 24, EP	6, 10, 19, 23, EP	GND	<b>Power ground.</b>
9	20	BOUT1	<b>Bridge B output terminal 1.</b>
10, 22	8, 21	VIN	<b>Input supply voltage.</b> Both VIN pins must be connected to the same supply. Decouple VIN to ground with a minimum 100nF ceramic capacitor.
11	22	BOUT2	<b>Bridge B output terminal 2.</b>
13	24	BPHASE	<b>Phase (direction) input for bridge B.</b>
14	25	VCP	<b>Charge pump output.</b> Connect a 1μF, 16V ceramic capacitor from VCP to VIN.
15	28	CP2	<b>Charge pump capacitor.</b> Connect a 100nF ceramic capacitor rated for the VIN voltage between these terminals.
16	1	CP1	
17	2	VG	<b>Low-side MOSFETs gate drive voltage.</b> Connect a 220nF, 16V ceramic capacitor from VG to ground.
-	3, 17, 26, 27	NC	<b>No connection.</b>
18	4	APHASE	<b>Phase (direction) input for bridge A.</b>
19	5	nSLEEP	<b>Sleep mode input.</b> Drive nSLEEP to logic low to place the MP6601 in low-power sleep mode. Drive nSLEEP to logic high to enable normal operation. nSLEEP has an internal pull-down resistor.
21	7	AOUT2	<b>Bridge A output terminal 2.</b>
23	9	AOUT1	<b>Bridge A output terminal 1.</b>



## BLOCK DIAGRAM

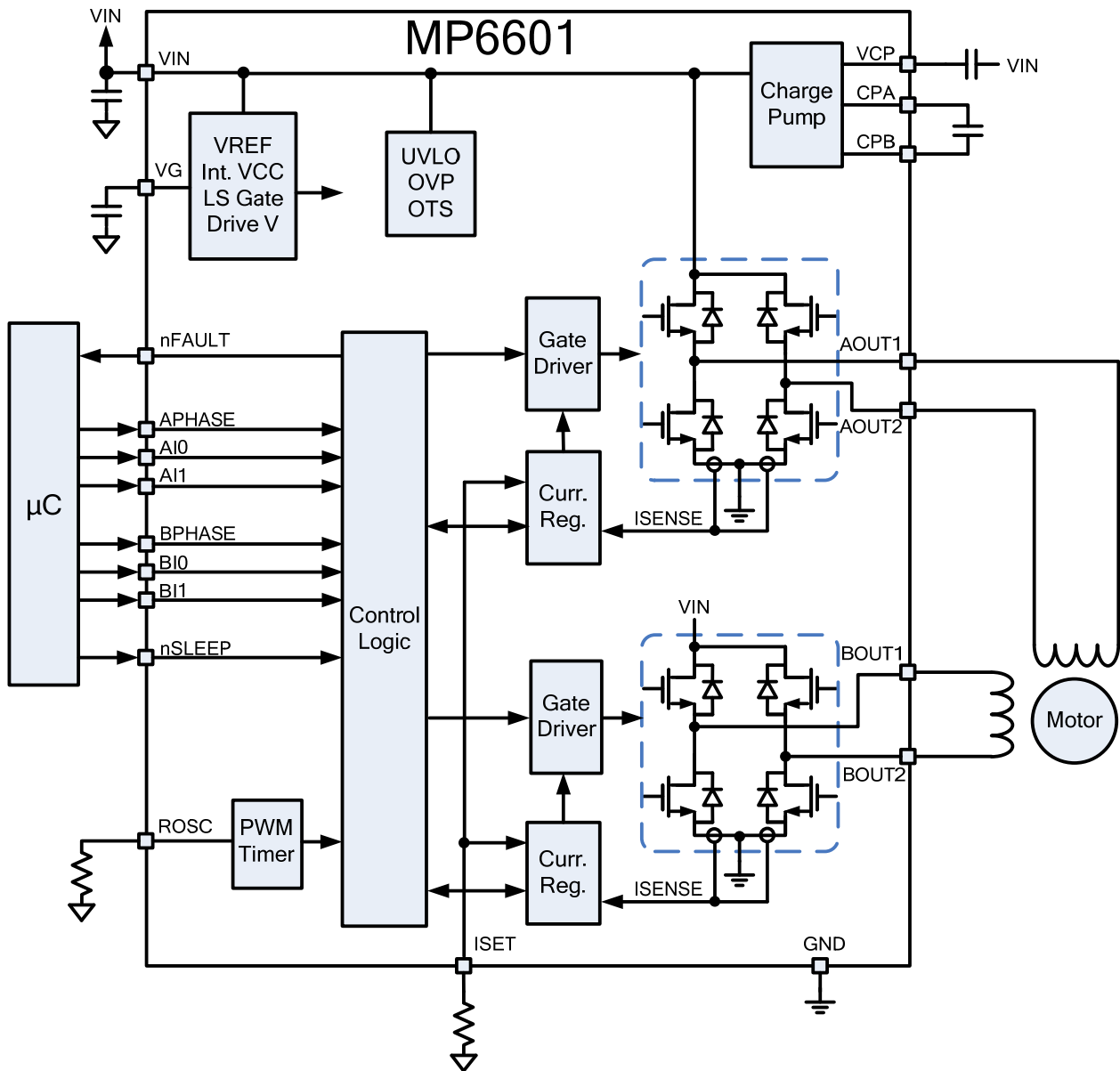


Figure 1: Functional Block Diagram

## OPERATION

The MP6601 is a bipolar stepper motor driver that integrates eight N-Channel power MOSFETs comprised of two internal full-bridges with 2.5A of current capability. The MP6601 operates over a wide supply voltage range of 4.5 - 35V.

The MP6601 is designed to operate bipolar stepper motors in full-, half-, and quarter-step modes. The current of each full-bridge is set by the output voltage of an internal DAC, which is controlled by the xI0 and xI1 input pins.

The currents in each of the two outputs are regulated with programmable, constant off-time, pulse-width modulation (PWM) control circuitry. The MP6601 integrates internal current sensing, eliminating the need for external sense resistors.

### Input Interface

The MP6601 contains two full H-bridges that operate independently. Each H-bridge has an input signal that controls the current flow direction in the H-bridge (see Table 1).

**Table 1: Input Control Truth Table**

xPHASE	xOUT1	xOUT2
0	L	H
1	H	L

Additionally, each H-bridge has two input pins that are used to scale the current regulation point in the bridge (see Table 2).

**Table 2: Current Regulator Sensing**

xI1	xI0	Current
0	0	100%
0	1	71%
1	0	38%
1	1	0% (high impedance)

### Programmable Constant Off-Time Current Control

The motor current is regulated by a programmable constant off-time PWM current control circuit. Its operation is described below:

- Initially, a diagonal pair of MOSFETs turns on and drives current through the motor winding.
- The current increases in the motor winding, which is sensed by an internal current-sense circuit. During the initial blanking time

( $t_{\text{BLANK}}$ ), the high-side MOSFET (HS-FET) always turns on in spite of current-limit detection.

- When the current reaches the current trip threshold, the internal current comparator either shuts off the HS-FET so the winding inductance current freewheels through the two low-side MOSFETs (LS-FET) (slow decay) or turns on another diagonal pair of MOSFETs so the current flows back to the input (fast decay).
- The current keeps decreasing for the constant off-time unless a zero current level is detected. Afterward, the HS-FET is enabled to increase the winding current again.
- The cycle then repeats.

Constant-off-time ( $t_{\text{off}}$ ) is determined by the selection of an external resistor ( $R_t$ ), which can be approximated with Equation (1):

$$t_{\text{OFF}}(\text{ns}) = 190 \times R_t(\text{k}\Omega) \quad (1)$$

The full-scale (100%) regulation current can be calculated with Equation (2):

$$I_{\text{Max}} = 71\text{k}\Omega / R_{\text{ISET}} \quad (2)$$

### Blanking Time

There is usually a current spike during the switching transition due to the body diode's reverse-recovery current or the distributed inductance or capacitance. This current spike requires filtering to prevent it from erroneously shutting down the HS-FET.

After the PWM cycle begins, the output of the current sense comparator is ignored for the fixed blanking time. This blanking time results in a minimum on time for the PWM cycle.

### Automatic Decay Mode

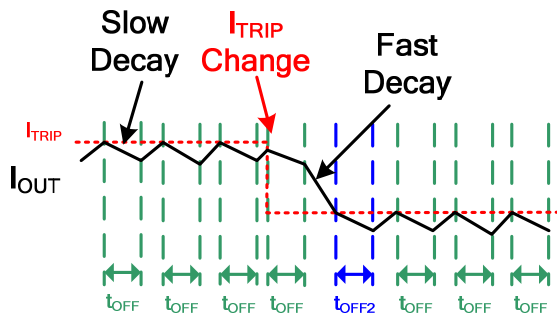
The MP6601 uses a fully automatic decay mode to provide accurate current regulation.

Initially, slow decay is used. At the end of the fixed off time, if the current is above the  $I_{\text{TRIP}}$  threshold, then fast decay mode is initiated by reversing the state of the H-bridge outputs.

Once the current level during this fast decay period drops below the  $I_{\text{TRIP}}$  threshold,

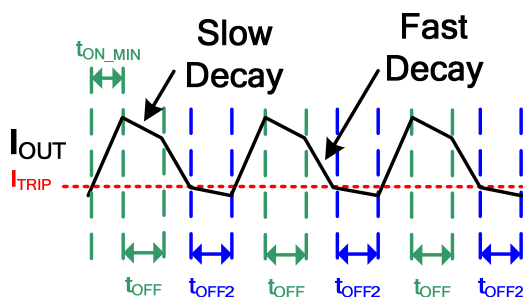
slow decay is engaged again for another fixed off time. After the completion of this second fixed off time, a new PWM cycle begins.

Figure 2 shows the automatic decay mode operation during a current reduction as a result of a change in  $xI0$  or  $xI1$ .



**Figure 2: Slow Decay during  $t_{OFF}$  Unless  $I_{OUT} > I_{TRIP}$  at End of  $t_{OFF}$**

In some cases (specifically high voltage and low inductance or regulation of very small currents), the minimum on time of the PWM cycle (set by the blanking time described above) can cause the current to rise very quickly. In this case, both slow and fast decay are used (see Figure 3).



**Figure 3: Current Regulation of Low Current/Low Inductance**

### Sleep Operation (nSLEEP)

Driving nSLEEP low puts the device into a low-power sleep state. In this state, the gate drive charge pump is stopped, and all internal circuits and H-bridge outputs are disabled. All inputs are ignored when nSLEEP is active low.

When waking up from sleep mode, approximately 1ms of time must pass before issuing a step command to allow the internal circuitry time to stabilize. nSLEEP has an internal pull-down resistor.

### Fault (nFAULT)

The MP6601 provides an nFAULT pin that reports to the system if a fault condition occurs, such as over-current protection (OCP), over-temperature protection (OTP), or over-voltage protection (OVP). nFAULT is an open-drain output type and is driven low when a fault condition occurs. If the fault condition is released, nFAULT is pulled high by an external pull-up resistor.

### Over-Current Protection (OCP)

OCP circuitry limits the current through the MOSFETs by disabling the gate driver. If the current reaches the over-current limit threshold and stays there for longer than the over-current deglitch time, all MOSFETs in the H-bridge are disabled, and nFAULT is driven low. The driver is disabled for 5ms, typically. Afterward, the driver is re-enabled automatically.

Over-current conditions on both the high- and low-side devices (i.e.: a short to ground, supply, or across the motor winding) result in an over-current shutdown. Note that OCP does not use the current-sense circuitry used for PWM current control.

### Over-Voltage Protection (OVP)

If the input voltage on VIN is higher than the OVP threshold, the H-bridge output is disabled, and nFAULT is driven low. This protection is released when VIN drops below 38V.

### Input UVLO Protection

If at any time the voltage on VIN falls below the under-voltage lockout (UVLO) threshold voltage, all circuitry in the device is disabled, and the internal logic is reset. Operation resumes when VIN rises above the UVLO threshold.

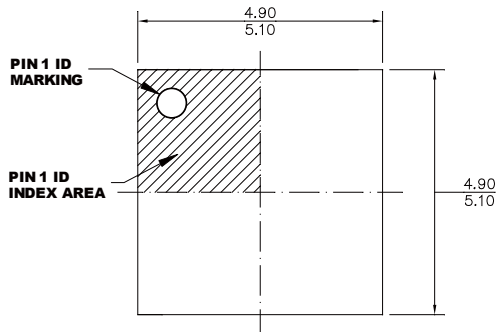
### Thermal Shutdown

If the die temperature exceeds safe limits, all MOSFETs in the H-bridge are disabled, and nFAULT is driven low. Once the die temperature has fallen to a safe level, operation resumes automatically.

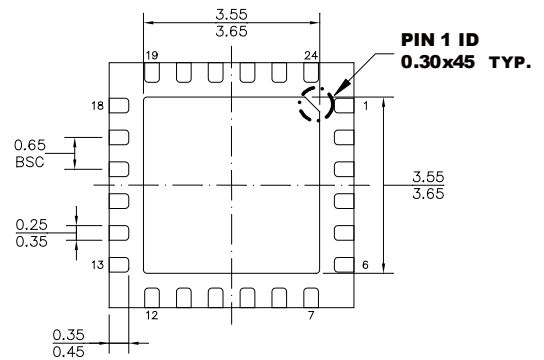


## PACKAGE INFORMATION

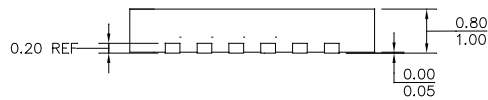
### QFN-24 (5mmx5mm)



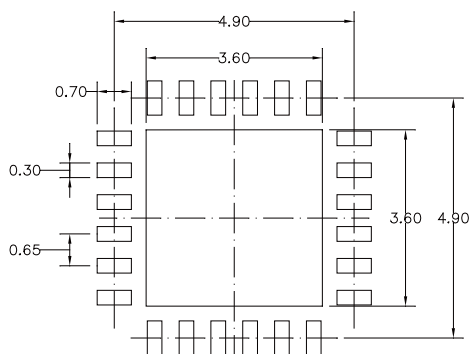
**TOP VIEW**



**BOTTOM VIEW**



**SIDE VIEW**



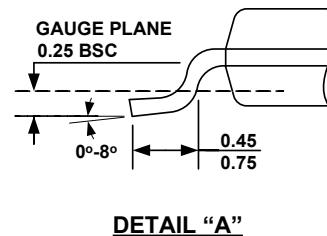
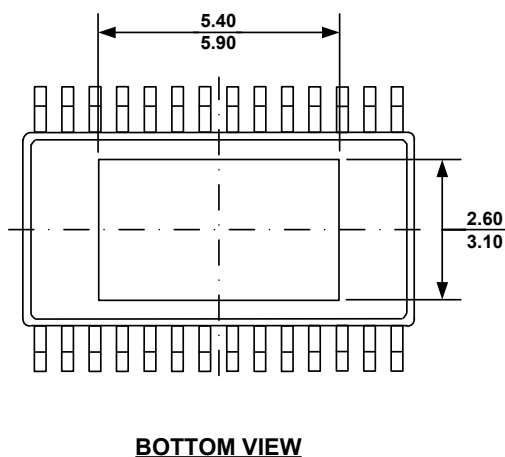
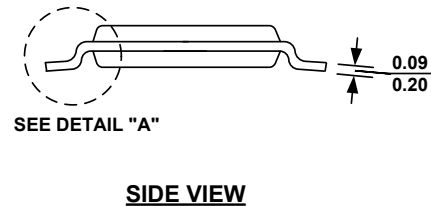
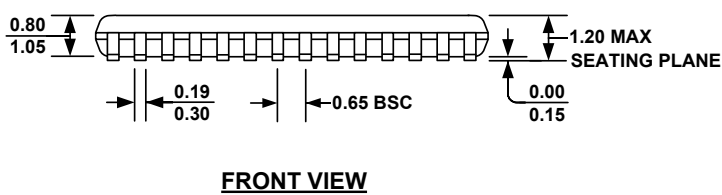
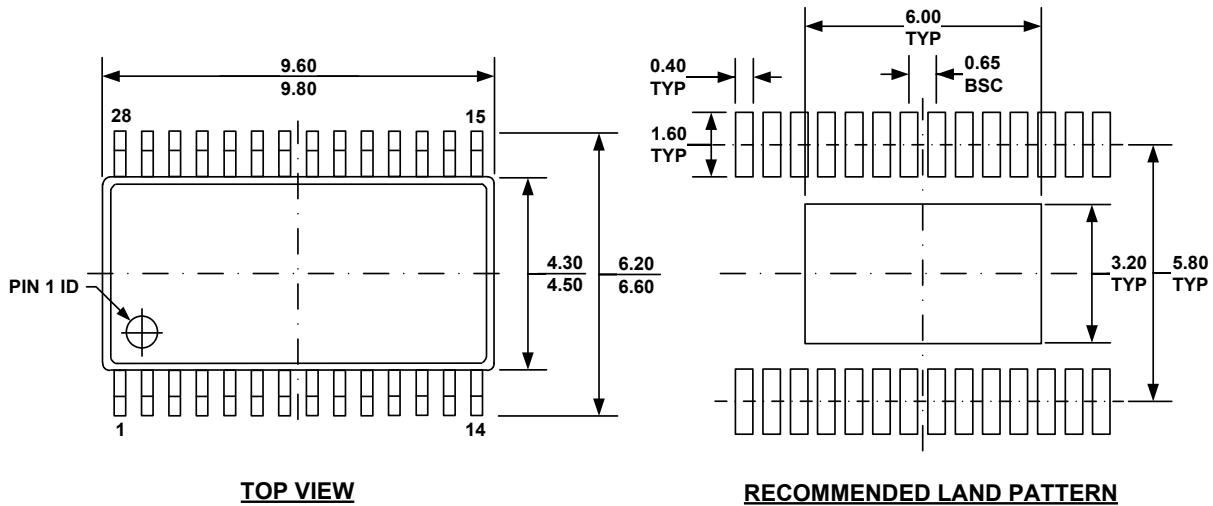
**RECOMMENDED LAND PATTERN**

### NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX
- 4) DRAWING CONFIRMS TO JEDEC MQ220.
- 5) DRAWING IS NOT TO SCALE

# PACKAGE INFORMATION (continued)

## TSSOP-28 EP



### NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION AET.
- 6) DRAWING IS NOT TO SCALE.

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