MPQ18811

Isolated, Single-Channel Gate Driver, AEC-Q100 Qualified

DESCRIPTION

The MPQ18811 is an isolated, single-channel gate driver solution with up to 6A of source and up to 10A of sink peak current capacity. The gate driver is designed to drive power switching devices with short propagation delay and pulse-width distortion. By utilizing capacitive-based isolation technology, the driver can provide 5kV$_{RMS}$ of withstand voltage (per UL 1577) with an SOIC wide-body (WB) package, and above 150kV/µs of common-mode transient immunity (CMTI) rating between the input side and the output driver. With the advanced features, the driver operates at high efficiency, high power density, and with robustness in a wide variety of automotive power applications.

A wide 2.8V to 5.5V, primary-side input power supply (V_{DDI}) range allows the driver to be interfaced with 3.3V or 5V digital controllers. The secondary-side driver accepts an up to 30V supply. All the supply pins feature various under voltage lockout (UVLO) protection levels.

The MPQ18811 is available in SOIC-8 narrow-body (NB) or wide-body (WB) packages.

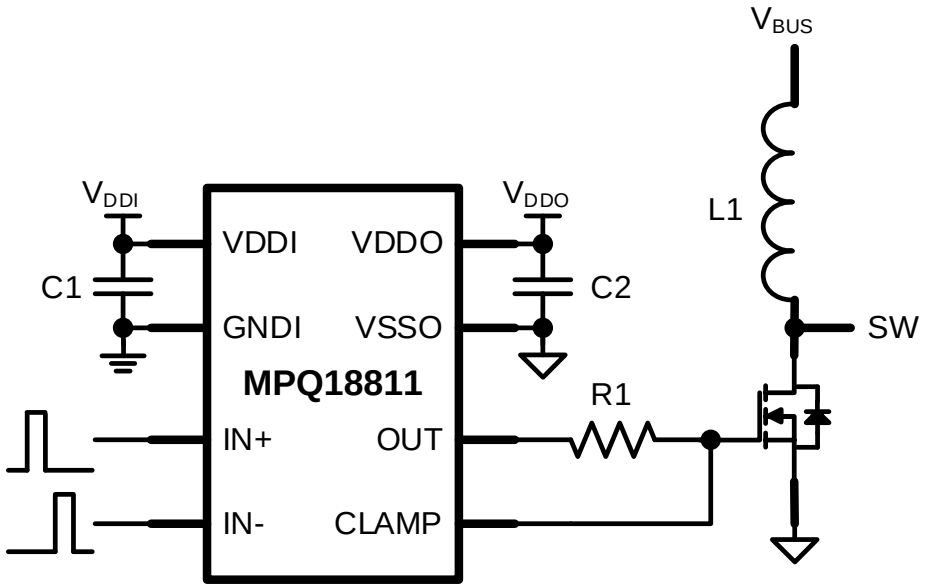
FEATURES

- Up to 5kV$_{RMS}$ Input to Output Reinforced Isolation Voltage (SOIC-8 WB)
- Common-Mode Transient Immunity (CMTI) >150kV/µs
- 2.8V to 5.5V Input VDDI Range to Interface with TTL/CMOS-Compatible Inputs
- Differential Input Control
- Up to 30V Output Drive Supply with Multiple Under-Voltage Lockout (UVLO) Options
- Output Configuration: Single-Output with Miller Clamp
- 6A Source/10A Sink Peak Current Output
- 55ns Typical Propagation Delay with Tiny ±5ns Distribution from Part to Part
- Internal Active Miller Clamp
- -40°C to +150°C Operating Junction Temperature (T_J) Range
- Available in SOIC-8 NB or SOIC-8 WB Packages
- UL 1577 Certified:
  - SOIC-8 NB: 3kV$_{RMS}$ Isolation for 60s
  - SOIC-8 WB: 5kV$_{RMS}$ Isolation for 60s
- Available in AEC-Q100 Grade 1
- DIN EN IEC 60747-17 (VDE 0884-17): 2021-10 Certified
- CQC Certification per GB 4943.1-2022

APPLICATIONS

- EV/HEV Motor Driver Inverters
- Onboard Chargers
- Industrial Drivers
- Half-/Full-Bridge Converters
- Isolated DC/DC and AC/DC Converters

TYPICAL APPLICATION



SELECTION GUIDE

Table 1: Selection Guide

Part Number	Peak Output Current (A)	Output UVLO Threshold (V)	Input Logic	Output Configuration	Miller Clamp	Package Type
MPQ18811-10BGS-AEC1	10	5	IN+/IN-	OUT	Yes	SOIC-8 NB
MPQ18811-10CGS-AEC1		8				
MPQ18811-10DGS-AEC1		10				
MPQ18811-10EGS-AEC1		12				
MPQ18811-10FGS-AEC1		15				
MPQ18811-10BGY-AEC1	10	5	IN+/IN-	OUT	Yes	SOIC-8 WB
MPQ18811-10CGY-AEC1		8				
MPQ18811-10DGY-AEC1		10				
MPQ18811-10EGY-AEC1		12				
MPQ18811-10FGY-AEC1		15				

ORDERING INFORMATION

Part Number*	Output UVLO (V)	Package	Top Marking	MSL Rating
MPQ18811-10CGS-AEC1	8	SOIC-8 NB	*See Below*	2
MPQ18811-10EGS-AEC1	12		*See Below*	
MPQ18811-10FGS-AEC1	15		*See Below*	
MPQ18811-10CGY-AEC1	8	SOIC-8 WB	*See Below*	3
MPQ18811-10EGY-AEC1	12		*See Below*	
MPQ18811-10FGY-AEC1	15		*See Below*	

* For Tape & Reel, add suffix -Z (e.g. MPQ18811-10FGY-AEC1-Z)

The 5V UVLO (B) and 10V UVLO (D) are additional options; contact the production line if needed.

Contact local sales or distributors to check the latest availability status for the ordering part numbers.

TOP MARKING

MPQ18811-10x (SOIC-8 NB)

1881110X
LLLLLLLL
MPSYWW

1881110X: Part number
10: Output peak sink current rating
X: UVLO level code, where x = B, C, D, E, or F
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

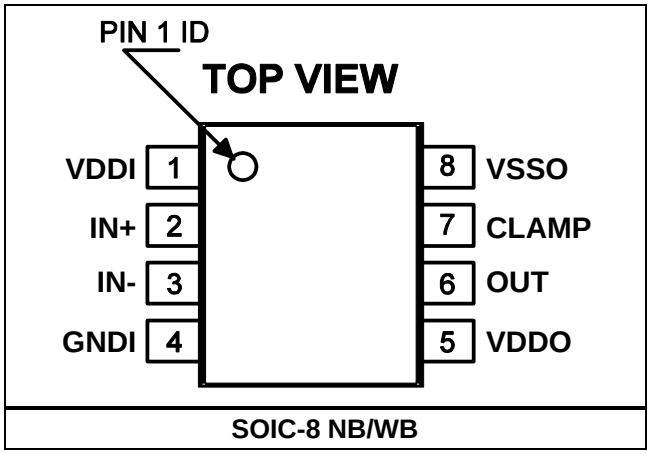
TOP MARKING

MPQ18811-10x (SOIC-8 WB)

18811-10X
LLLLLLLLL
MPSYWW

18811-10X: Part number
10: Output peak sink current rating
X: UVLO level code, where x = B, C, D, E, or F
LLLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE



SOIC-8 NB/WB

PIN FUNCTIONS

Pin #	Name	Description
1	VDDI	**Input-side power supply input.** The VDDI pin supplies power to the primary-side control circuitry. Decouple VDDI to GNDI locally using a low-ESR/ESL bypass capacitor. This capacitor should be placed as close to the chip as possible.
2	IN+	**Non-inverting logic control signal input.** The IN+ pin is pulled down internally.
3	IN-	**Inverting logic control signal input.** The IN- pin is pulled up internally.
4	GNDI	**Input-side ground.** The GNDI pin is the ground reference for all input-side signals and internal control blocks.
5	VDDO	**Output-side driver power supply input.** The VDDO pin supplies power to the secondary-side driver circuitry. Decouple VDDO to VSSO locally using a low-ESR/ESL bypass capacitor. This capacitor should be placed as close to the chip as possible.
6	OUT	**Gate drive output.** Connect the OUT pin to the gate of the power device using a gate driver resistor.
7	CLAMP	**Active Miller clamp output.** Connect the CLAMP pin directly to the gate of the power device.
8	VSSO	**Output-side ground.** The VSSO pin is the ground reference for the output driver.

ABSOLUTE MAXIMUM RATINGS (1)

V_{DDI} - V_{GNDI} .....-0.3V to +6.5V
V_{IN+}, V_{IN-} ..... V_{GNDI} - 0.3V to V_{DDI} + 0.3V
V_{IN+}, V_{IN-} (transient for 50ns)……..
..... V_{GNDI} - 5V to V_{DDI} + 0.3V
V_{DDO} - V_{SSO} .....-0.3V to +35V
V_{OUT}, V_{CLAMP} ..... V_{SSO} - 0.3V to V_{DDO} + 0.3V
V_{OUT}, V_{CLAMP} (transient for 200ns)……..
..... V_{SSO} - 2V to V_{DDO} + 0.3V
Continuous power dissipation (T_A = 25°C) (2)
SOIC-8 NB 1405mW
SOIC-8 WB 1785mW
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) (3)..... 4000V
Charged-device model (CDM) (4) 2000V

Recommended Operating Conditions (5)

V_{DDI} - V_{GNDI} .....2.8V to 5.5V
V_{IN+}, V_{IN-} ..... V_{GNDI} to V_{DDI}
V_{DDO} - V_{SSO} ..... 6.5V to 30V (5V UVLO option)
..... 9.2V to 30V (8V UVLO option)
..... 12V to 30V (10V UVLO option)
..... 14.5V to 30V (12V UVLO option)
..... 17.5V to 30V (15V UVLO option)
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance (6) θ_{JA} θ_{JC}

SOIC-8 NB..... 89 ..... 37... °C/W
SOIC-8 WB..... 70 ..... 19... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AECQ100-002.
4) Per AECQ100-011.
5) The device is not guaranteed to function outside of its operating conditions.
6) Measured on the MPQ18811 evaluation board, 2-layer PCB.

ELECTRICAL CHARACTERISTICS

2.8V ≤ (V_{DDI} - V_{GNDI}) ≤ 5.5V, V_{DDO} - V_{SSO} = 12V/15V/20V (7), T_J = -40°C to +150°C, typical values are tested at T_J = 25°C, all voltages with respect to the corresponding ground(s), unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input-Side Supply Voltage						
V_{DDI} under-voltage lockout (UVLO) threshold	V_{DDI_UVLO}	(V_{DDI} - V_{GNDI}) falling	2.42	2.6	2.78	V
V_{DDI} UVLO hysteresis	$V_{DDI\_UVLO\_HYS}$		80	100	120	mV
Input-Side Supply Current						
VDDI quiescent current	I_{VDDI_Q}	V_{IN+} = V_{GNDI}		0.6	1	mA
VDDI operating current	I_{VDDI}	f_{SW} = 500kHz, 50% duty, C_{LOAD} = 100pF		1.3	2	mA
Logic Input Level (IN+/IN-)						
Logic input high threshold	V_{LI_HIGH}	(V_{LI} - V_{GNDI}) rising		1.8	2	V
Logic input low threshold	V_{LI_LOW}	(V_{LI} - V_{GNDI}) falling	0.8	1.2		V
Logic input hysteresis	V_{LI_HYS}		0.5	0.6	0.7	V
Logic input internal pull-up resistance	R_{LI_PU}	IN- to VDDI		50		kΩ
Logic input internal pull-down resistance	R_{LI_PD}	IN+ to GNDI		50		kΩ
Output-Side Supply Voltage						
V_{DDO} UVLO threshold	V_{DDO_UVLO}	-B, 5V UVLO, (V_{DDO} - V_{SSO}) falling	5	5.5	6	V
		-C, 8V UVLO, (V_{DDO} - V_{SSO}) falling	7.5	8	8.5	V
		-D, 10V UVLO, (V_{DDO} - V_{SSO}) falling	9.3	10	10.7	V
		-E, 12V UVLO, (V_{DDO} - V_{SSO}) falling	10	11	12	V
		-F, 15V UVLO, (V_{DDO} - V_{SSO}) falling	13.8	15	16.5	V
V_{DDO} UVLO hysteresis	$V_{DDO\_UVLO\_HYS}$	-B, 5V UVLO	200	300	400	mV
		-C, 8V UVLO	400	500	600	mV
		-D/-E/-F, 10V/12V/15V UVLO	0.8	1	1.2	V
Output-Side Supply Current						
VDDO quiescent current	I_{VDDO_Q}	V_{IN+} = V_{GNDI}		1	1.5	mA
VDDO operation current	I_{VDDO}	f_{SW} = 500kHz, C_{LOAD} = 100pF, V_{DDO} - V_{SSO} = 12V		3.3	4.5	mA
		f_{SW} = 500kHz, C_{LOAD} = 100pF, V_{DDO} - V_{SSO} = 15V		3.6	5	mA
		f_{SW} = 500kHz, C_{LOAD} = 100pF, V_{DDO} - V_{SSO} = 20V		4	5.5	mA
Gate Driver						
High-level output voltage	V_{OUT_HIGH}	I_{OUT} = -200mA	V_{DDO} - 0.33	V_{DDO} - 0.18		V
Low-level output voltage	V_{OUT_LOW}	I_{OUT} = 200mA		V_{SSO} + 74	V_{SSO} + 134	mV
		VDDO open/not powered, I_{OUT} = 1A (active pull-down)		V_{SSO} + 2	V_{SSO} + 2.5	V

ELECTRICAL CHARACTERISTICS *(continued)*

2.8V ≤ (V_{DDI} - V_{GNDI}) ≤ 5.5V, V_{DDO} - V_{SSO} = 12V/15V/20V (7), T_J = -40°C to +150°C, typical values are tested at T_J = 25°C, all voltages with respect to the corresponding ground(s), unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Output peak source current (8)	I_{OUT_SRC}	V_{DDO} - V_{SSO} = 20V, V_{OUT} - V_{SSO} = 10V, f_{SW} = 1kHz	-3	-6		A
Output peak sink current (8)	I_{OUT_SNK}	V_{DDO} - V_{SSO} = 20V, V_{OUT} - V_{SSO} = 10V, f_{SW} = 1kHz	5	10		A
Output source resistance	R_{OUT_SOURCE}	I_{OUT} = -200mA		900	1650	mΩ
Output sink resistance	R_{OUT_SINK}	I_{OUT} = 200mA		370	670	mΩ
Dead Time (DT) and Overlap Protection						
Dead time (DT)	t_{DT}	For IN+/IN- control	6	10	15	ns
Active Miller Clamp						
Active clamp threshold voltage	V_{CLAMP_TH}	(V_{CLAMP} - V_{SSO}) falling	1.5	2	2.5	V
Low-level clamp voltage	V_{CLAMP_LOW}	I_{CLAMP} = 1A		V_{SSO} + 1	V_{SSO} + 2.5	V
Low-level clamp current	I_{CLAMP_LOW}	V_{CLAMP} - V_{SSO} = 2.5V	1.2	2		A
Clamp FET on resistance	R_{CLAMP}	I_{CLAMP} = 200mA		1	2	Ω
Active clamp turn-on delay	t_{CLAMP}	Once (V_{CLAMP} - V_{SSO}) falls below V_{CLAMP_TH}		20	40	ns
Thermal Shutdown						
Primary thermal shutdown threshold	T_{SD_PRI}	Junction temperature (T_J) rising		170		°C
Primary thermal shutdown hysteresis	T_{HYS_PRI}			20		°C
Secondary thermal shutdown threshold	T_{SD_SEC}	T_J rising		170		°C
Secondary thermal shutdown hysteresis	T_{HYS_SEC}			20		°C
Switching Characteristics (See Dynamic Parameter Definitions Section on Page 18 and Page 19 for More Details)						
Output rising time	t_R	(V_{OUT} - V_{SSO}) rising, C_{LOAD} = 10nF V_{DDO} - V_{SSO} = 20V		42	55	ns
Output falling time	t_F	(V_{OUT} - V_{SSO}) falling, C_{LOAD} = 10nF V_{DDO} - V_{SSO} = 20V		32	43	ns
Minimum pulse-width	t_{PW_MIN}	Output pulse off if shorter than t_{PW_MIN}, C_{LOAD} = 0pF			28	ns
Propagation delay from input high to output rising edge	t_{PDLH}	C_{LOAD} = 0pF	40	55	65	ns
Propagation delay from input low to output falling edge	t_{PDHL}	C_{LOAD} = 0pF	40	55	65	ns
Pulse-width distortion ($\lvert t_{PDLH} - t_{PDHL} \rvert$)	t_{PWD}	C_{LOAD} = 0pF		2.7	7	ns

ELECTRICAL CHARACTERISTICS *(continued)*

2.8V ≤ (V_{DDI} - V_{GNDI}) ≤ 5.5V, V_{DDO} - V_{SSO} = 12V/15V/20V (7), T_J = -40°C to +150°C, typical values are tested at T_J = 25°C, all voltages with respect to the corresponding ground(s), unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Propagation delay part-to-part skew (9)	t_{PDS}	C_{LOAD} = 0pF			10	ns
Start-up delay from input supply UVLO exit to output rising edge	t_{STU_VDDI}	V_{IN+} = V_{DDI}, V_{IN-} = V_{GNDI}, C_{LOAD} = 0pF	12	16	22	µs
Shutdown delay from input supply UVLO entry to output falling edge (8)	t_{SHD_VDDI}	V_{IN+} = V_{DDI}, V_{IN-} = V_{GNDI}, C_{LOAD} = 0pF		250		ns
Start-up delay from output supply UVLO exit to output rising edge	t_{STU_VDDO}	V_{IN+} = V_{DDI}, V_{IN-} = V_{GNDI}, C_{LOAD} = 0pF	14	20	27	µs
Shutdown delay from output supply UVLO entry to output falling edge (8)	t_{SHD_VDDO}	V_{IN+} = V_{DDI}, V_{IN-} = V_{GNDI}, C_{LOAD} = 0pF		600		ns
Static common-mode transient immunity (8)	$CMTI_{STC}$	V_{IN-} = V_{GNDI}, V_{IN+} = V_{GNDI} or V_{DDI}, slew rate of V_{GNDI} versus V_{SSO}, V_{CM} = 1500V	150			kV/µs
Dynamic common-mode transient immunity (8)	$CMTI_{DYN}$	V_{IN-} = V_{GNDI}, f = 100kHz pulse at IN+, slew rate of V_{GNDI} versus V_{SSO}, V_{CM} = 1500V	150			kV/µs

Notes:

7) For the test condition, V_{DDO} - V_{SSO} = 12V is used for the 5V and 8V UVLO devices, V_{DDO} - V_{SSO} = 15V is used for the 10V and 12V UVLO devices, and V_{DDO} - V_{SSO} = 20V is used for the 15V UVLO devices.
8) Guaranteed by characterization. Not production tested.
9) Guaranteed by characterization. The propagation delay part-to-part skew is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.

INSULATION & SAFETY-RELATED SPECIFICATIONS

Parameters	Symbol	Condition	SOIC-8 WB	SOIC-8 NB	Units
External air gap (clearance) (10)	CLR	Shortest pin-to-pin distance through air between primary and secondary side	>8	>4	mm
External tracking (creepage) (10)	CPG	Shortest pin-to-pin distance across the package surface between primary and secondary side	>8	>4	mm
Distance through insulation	DTI	Internal clearance	>25	>12	μm
Comparative tracking index	CTI	According to IEC 60112	>600	>600	V
Material group		According to IEC 60664-1	I	I	
Over-voltage category (per IEC 60664-1)		Rated mains voltages ≤ 150V_{RMS}	I-IV	I-IV	
		Rated mains voltages ≤ 300V_{RMS}	I-IV	I-III	
		Rated mains voltages ≤ 600V_{RMS}	I-III	I-II	
		Rated mains voltages ≤ 1000V_{RMS}	I-II	-	
UL 1577, 5th Edition					
Recognized under the UL 1577 Component Recognition Program, Single Protection, File Number: E322138					
Dielectric withstand insulation voltage	V_{ISO}	V_{TEST} = V_{ISO} for t = 60s (qualification), V_{TEST} = 1.2 x V_{ISO} for t = 1s (100% production)	5000	3000	V_{RMS}
DIN EN IEC 60747-17 (VDE 0884-17): 2021-10 (11)					
Certified according to DIN EN IEC 60747-17 (VDE 0884-17): 2021-10, EN IEC 60747-17: 2020, and AC: 2021; certification number: 40057755, 40055265					
Maximum repetitive peak isolation voltage	V_{IORM}	AC voltage (bipolar)	2121	990	V_{PK}
Maximum working isolation voltage	V_{IOWM}	AC voltage (sine wave), according to the time-dependent dielectric breakdown (TDDB) test	1500	700	V_{RMS}
		DC voltage	2121	990	V_{DC}
Maximum transient isolation voltage	V_{IOTM}	V_{TEST} = V_{IOTM} for t = 60s (qualification), V_{TEST} = 1.2 x V_{IOTM} for t = 1s (100% production)	7000	4242	V_{PK}
Apparent charge (12) measuring voltage	$V_{PD(M)}$	Method B1, at routine test (100% production) and preconditioning (type test), $V_{PD(INI)}$ = 1.2 x V_{IOTM}, t_{INI} = 1s, $V_{PD(M)}$ = 1.5 x V_{IORM} (basic insulation), t_m = 1s, partial discharge < 5pC	-	1485	V_{PK}
		Method B1, at routine test (100% production) and preconditioning (type test), $V_{PD(INI)}$ = 1.2 x V_{IOTM}, t_{INI} = 1s, $V_{PD(M)}$ = 1.875 x V_{IORM} (reinforced insulation), t_M = 1s, partial discharge < 5pC	3977	-	V_{PK}
Maximum surge isolation voltage (13)	V_{IOSM}	Tested per IEC 62368-1 with 1.2/50μs pulse, V_{TEST} = 1.3 x V_{IMP} (basic insulation, qualification)	-	4242	V_{PK}
		Tested per IEC 62368-1 with 1.2/50μs pulse, V_{TEST} = 1.3 x V_{IMP} tested with 10kV (reinforced insulation, qualification)	8000	-	V_{PK}

INSULATION & SAFETY-RELATED SPECIFICATIONS *(continued)*

Parameters	Symbol	Condition	SOIC-8 WB	SOIC-8 NB	Units
Barrier capacitance (14)	C_{IO}	f = 1MHz	~1	~1	pF
Insulation resistance (14)	R_{IO}	V_{IO} = 500V, T_A = 25°C	>10^{12}		Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	>10^{11}		Ω
		V_{IO} = 500V, T_A = T_S = 150°C	>10^{9}		Ω
Pollution degree		Per DIN VDE 0110, table 1	2		
Climatic category			40/125/21		
IEC/EN/UL/CSA 62368-1/61010-1, IEC 60950-1					
TUV SUD certification conformity; certificate number: SG PSB-IV-07177M1, SG PSB-IV-07941, SG PSB-OF-06920M1, SG PSB-OF-007050, SG PSB-MS-00361, U10 113824 0003 Rev. 01, B 113824 0002 Rev. 02, U10 113824 0011 Rev. 00, B 113824 0010 Rev. 00. SOIC-8 WB: Reinforced insulation, altitude ≤ 5000m, 125°C thermal cycling test passed, 700V_P maximum working voltage SOIC-8 NB: Basic insulation, altitude ≤ 5000m, 125°C thermal cycling test passed, 660V_P maximum working voltage					
GB 4943.1-2022					
Certified according to CQC GB 4943.1-2022, file number: CQC22001348725, CQC23001376765 SOIC-8 WB: Reinforced insulation, altitude ≤ 5000m, 125°C thermal cycling test passed, 700V_P maximum working voltage SOIC-8 NB: Basic insulation, altitude ≤ 5000m, 125°C thermal cycling test passed, 660V_P maximum working voltage					

Notes:

10) See the Package Information section on page 31 and page 32 for the detailed dimensions. As an isolated solution, the recommended land pattern has enough safety creepage and clearance distance on a PCB.
11) This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
12) Electrical discharge caused by a partial discharge in the coupler.
13) The surge test is carried out in oil.
14) The barrier's primary-side and secondary-side terminals are connected together to form a two-terminal device. Then C_{IO} and R_{IO} are measured between the two terminals of the coupler.

SAFETY LIMITING VALUES (15)

Parameters	Symbol	Condition	SOIC-8 WB	SOIC-8 NB	Units
Maximum safety temperature (16)	T_S		150	150	°C
Maximum output safety current	I_{S_O}	V_{DDO} - V_{SSO} = 12V (17), T_J = 150°C, T_A = 25°C	147	115	mA
		V_{DDO} - V_{SSO} = 30V, T_J = 150°C, T_A = 25°C	59	46	mA
Safety power dissipation (18)	P_S	Input side	15	15	mW
		Output side	1770	1390	mW
		Total	1785	1405	mW

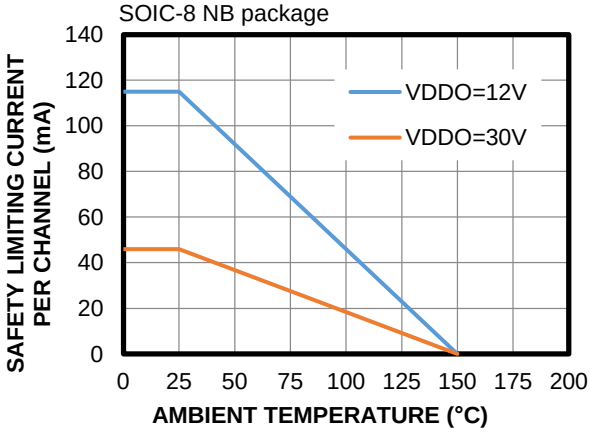
Notes:

15) The maximum value allowed in the event of a failure.
16) The maximum safety temperature, T_S, is the same value as the maximum junction temperature, T_J (MAX), specified in the Absolute Maximum Ratings section on page 6.
17) Tested for both the 5V and 8V UVLO devices.
18) Test conditions: V_{DDI} - V_{GNDI} = 5.5V, V_{DDO} - V_{SSO} = 30V, T_J = 150°C, T_A = 25°C. The safety power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature T_A: $T_S = T_J (MAX) = T_A + (\theta_{JA} \times P_S)$, $P_S = I_S \times V_{IN}$, where V_{IN} is the input voltage).

THERMAL DERATING CURVES FOR SAFETY LIMITING VALUES

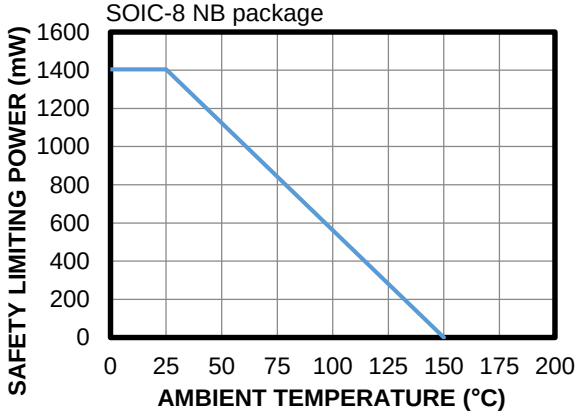
Safety Limiting Current per Channel vs. Ambient Temperature

SOIC-8 NB package



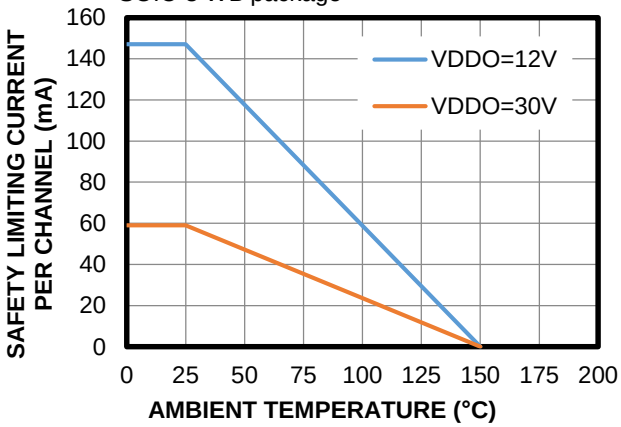
Safety Limiting Power vs. Ambient Temperature

SOIC-8 NB package



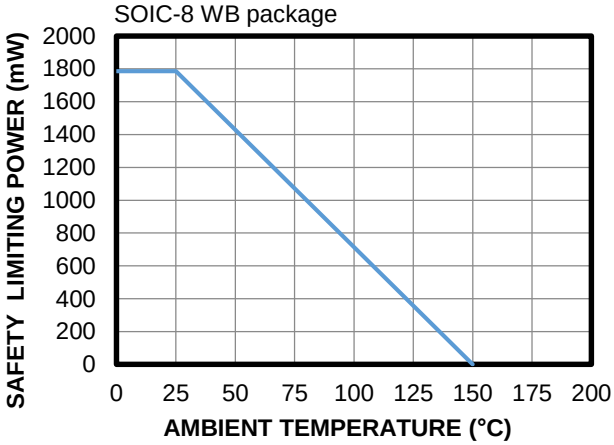
Safety Limiting Current vs. Ambient Temperature

SOIC-8 WB package



Safety Limiting Power vs. Ambient Temperature

SOIC-8 WB package

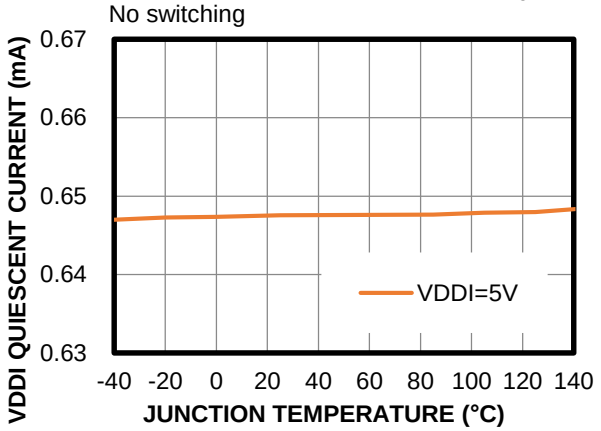


TYPICAL CHARACTERISTICS

V_{DDI} - V_{GNDI} = 5V, V_{DDO} - V_{SSO} = 15V, C_{LOAD} = 0pF, T_J = 25°C, all voltages with respect to the corresponding ground(s), unless otherwise noted.

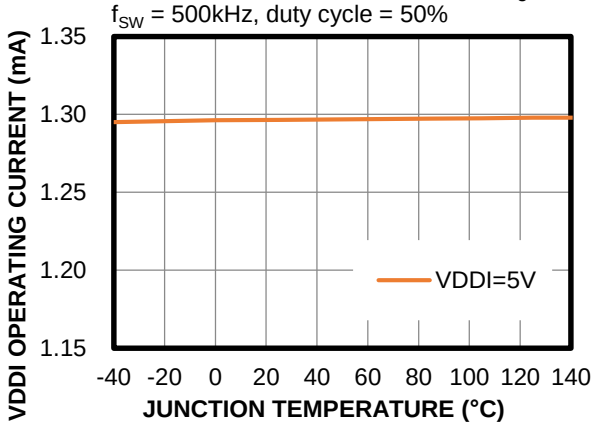
VDDI Quiescent Current vs. T_J

No switching



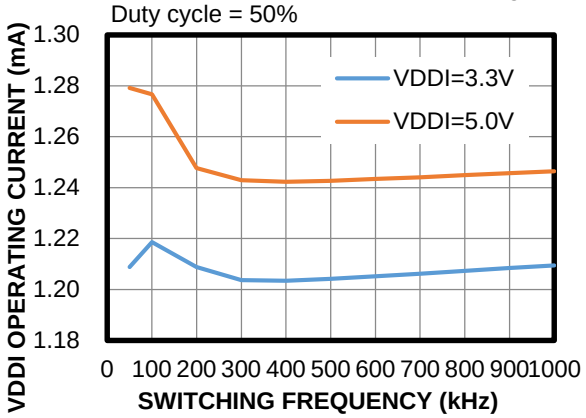
VDDI Operating Current vs. T_J

f_{SW} = 500kHz, duty cycle = 50%



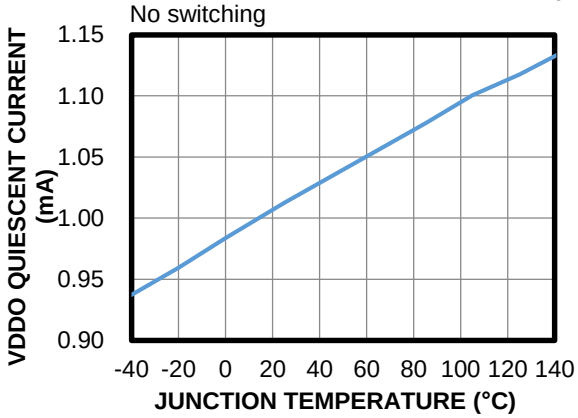
VDDI Operating Current vs. f_{SW}

Duty cycle = 50%



VDDO Quiescent Current vs. T_J

No switching



VDDO Operating Current vs. T_J

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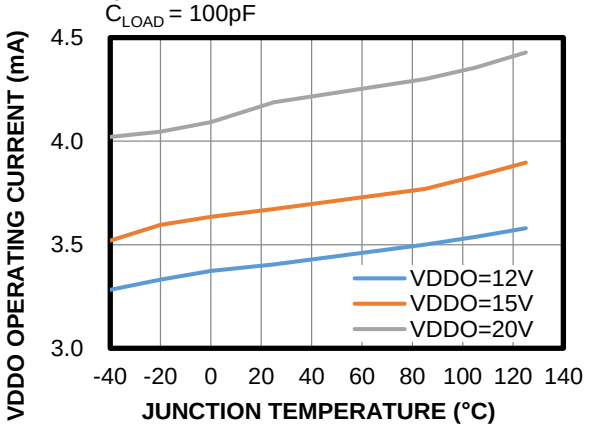
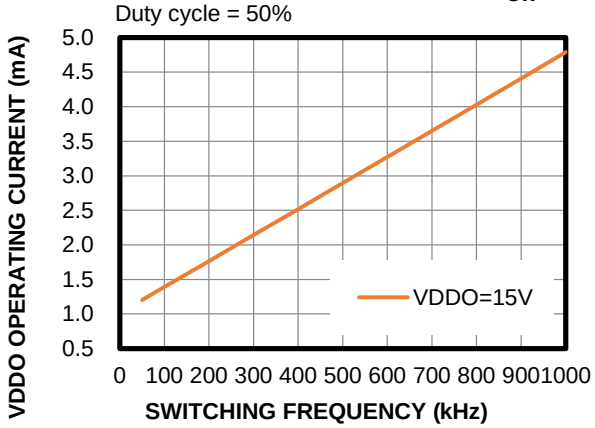
C_{LOAD} = 100pF



VDDO Operating Current vs. f_{SW}

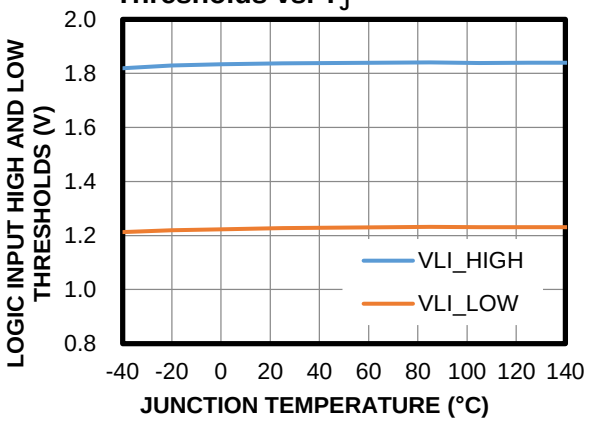
Duty cycle = 50%



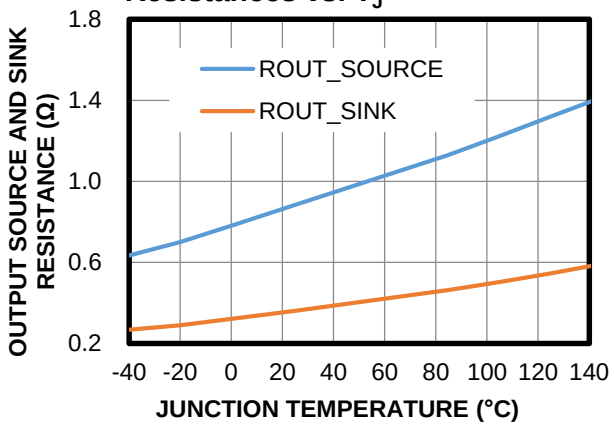
TYPICAL CHARACTERISTICS (*continued*)

V_{DDI} - V_{GNDI} = 5V, V_{DDO} - V_{SSO} = 15V, C_{LOAD} = 0pF, T_J = 25°C, all voltages with respect to the corresponding ground(s), unless otherwise noted.

Logic Input High and Low Thresholds vs. T_J

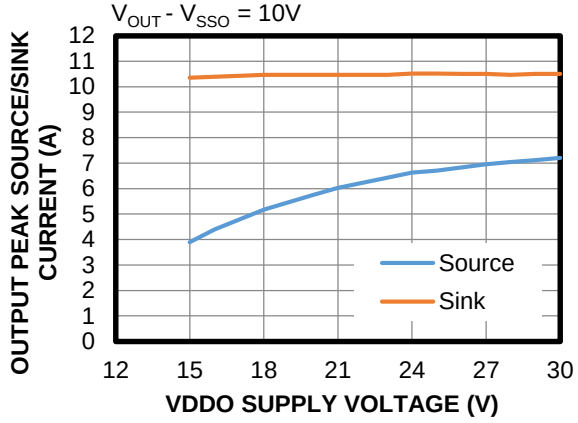


Output Source and Sink Resistances vs. T_J



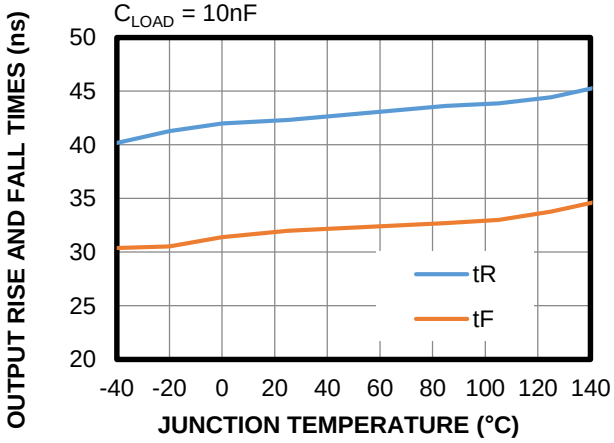
Output Peak Source/Sink Current vs. VDDO Supply Voltage

V_{OUT} - V_{SSO} = 10V

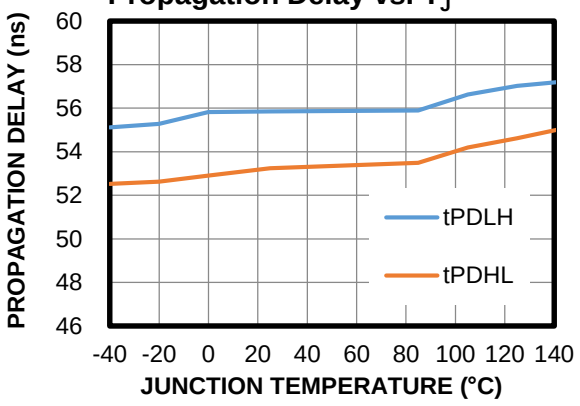


Output Rise and Fall Times vs. T_J

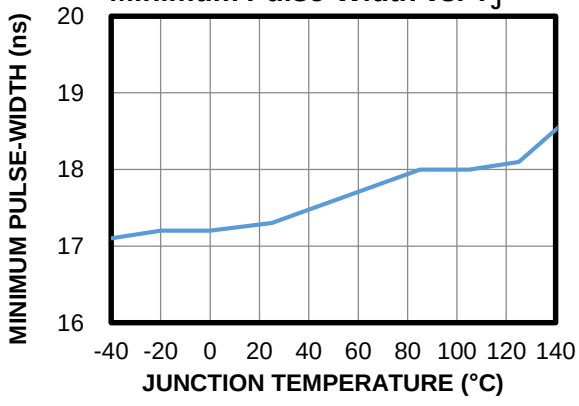
C_{LOAD} = 10nF



Propagation Delay vs. T_J

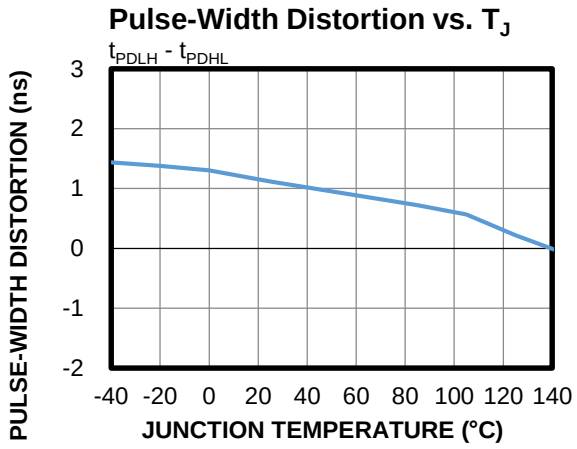


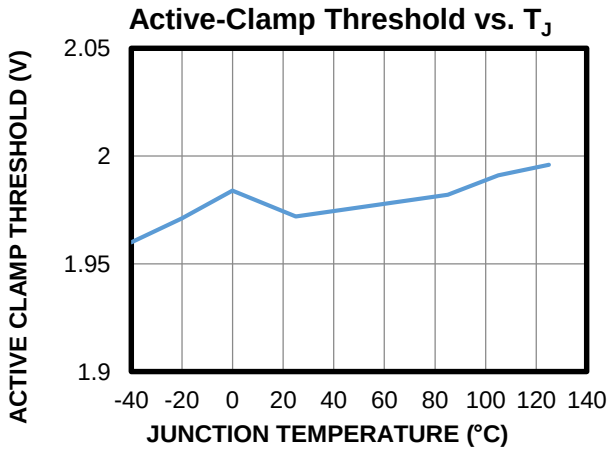
Minimum Pulse-Width vs. T_J

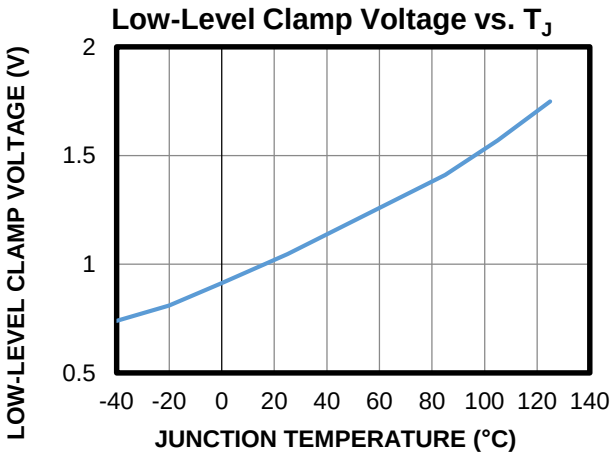


TYPICAL CHARACTERISTICS (*continued*)

V_{DDI} - V_{GNDI} = 5V, V_{DDO} - V_{SSO} = 15V, C_{LOAD} = 0pF, T_J = 25°C, all voltages with respect to the corresponding ground(s), unless otherwise noted.



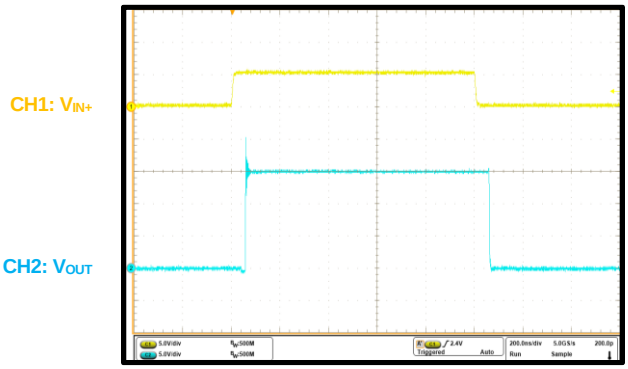




TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board. V_{DDI} - V_{GNDI} = 5V, V_{DDO} - V_{SSO} = 15V, C_{LOAD} = 0pF, T_A = 25°C, all voltages with respect to the corresponding ground(s), unless otherwise noted.

Typical Switching Waveforms



DYNAMIC PARAMETER DEFINITIONS

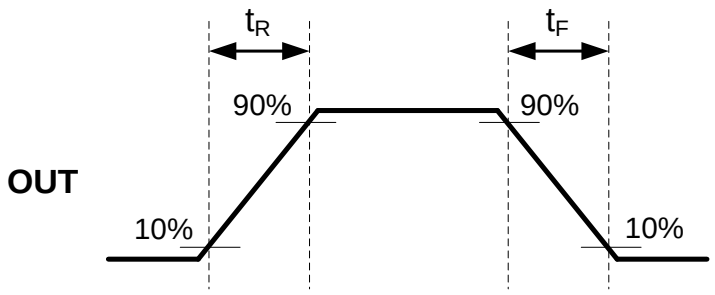


Figure 1: Output Rising and Falling Time

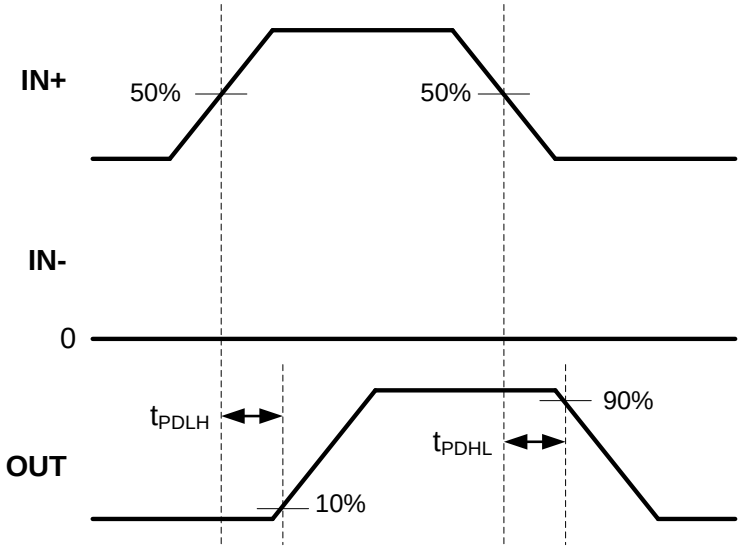


Figure 2: Non-Inverting Logic Propagation Delay

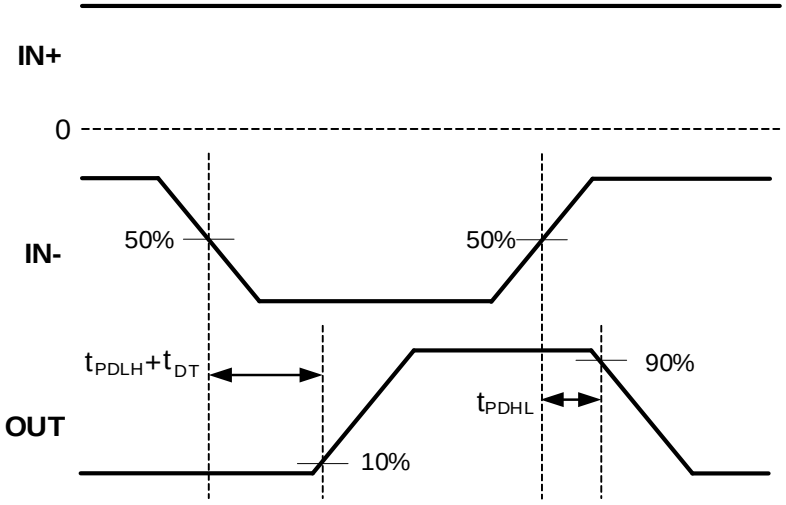


Figure 3: Inverting Logic Propagation Delay

DYNAMIC PARAMETER DEFINITIONS *(continued)*

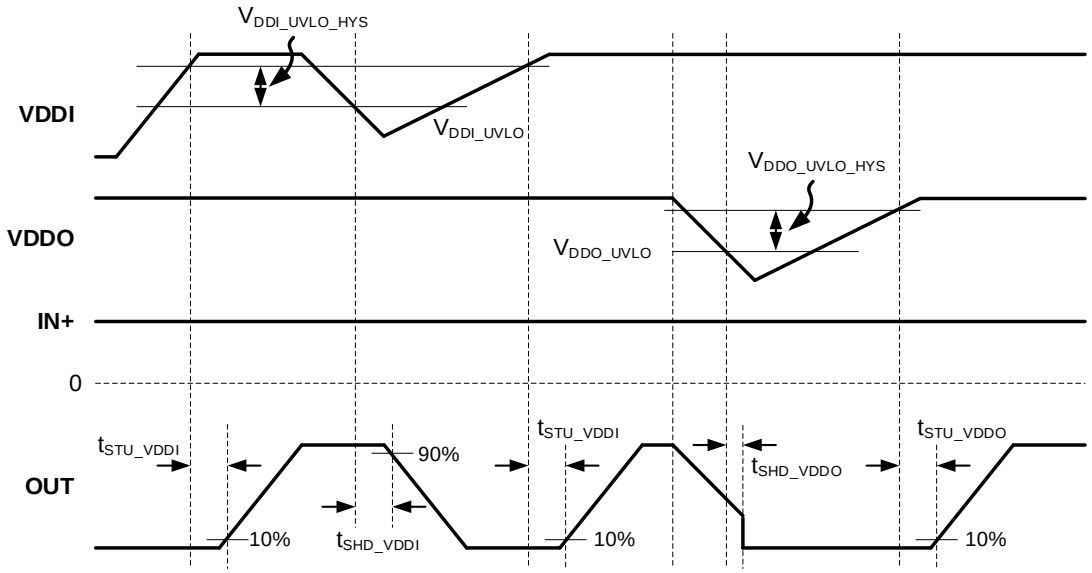


Figure 4: VDDI and VDDO Under-Voltage Lockout (UVLO)

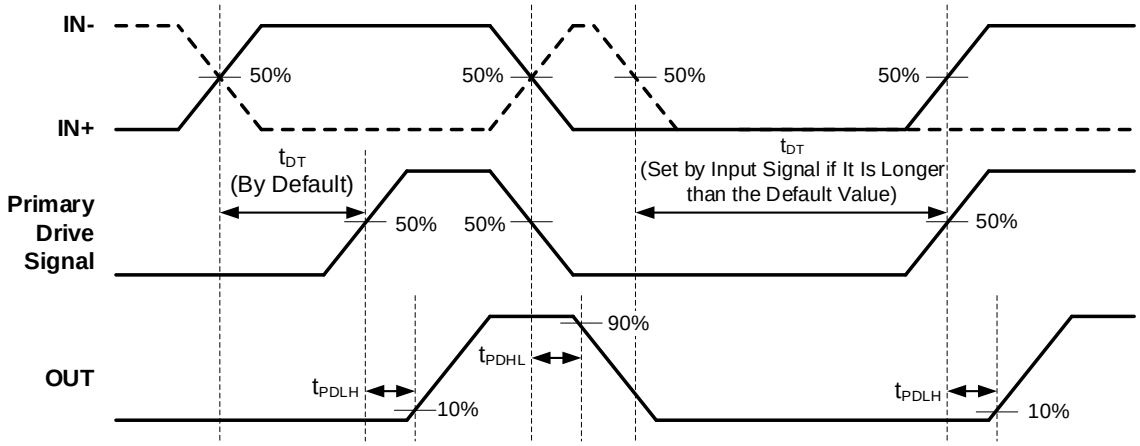


Figure 5: Dead Time (DT) Operation

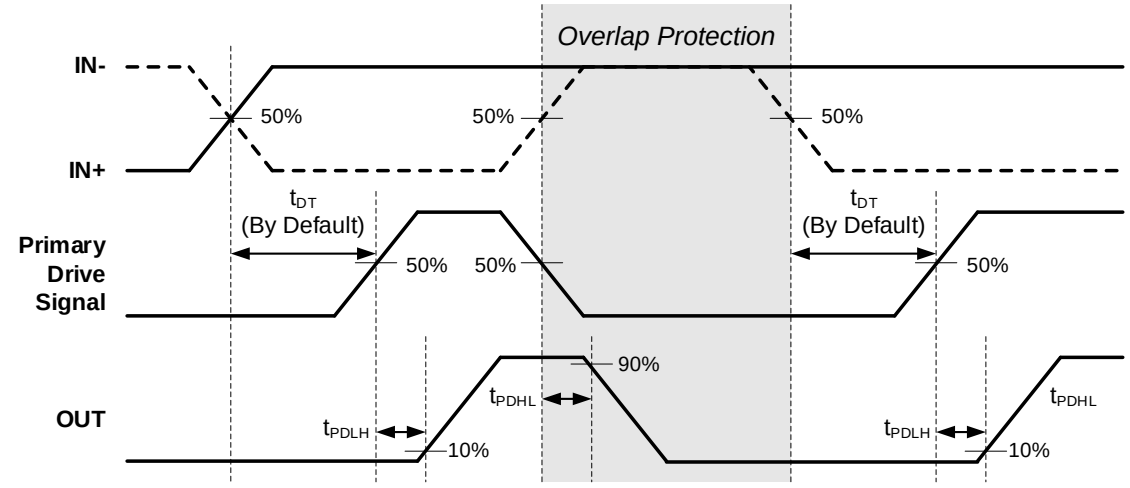


Figure 6: Overlap Protection and Recovery

DYNAMIC PARAMETER DEFINITIONS *(continued)*

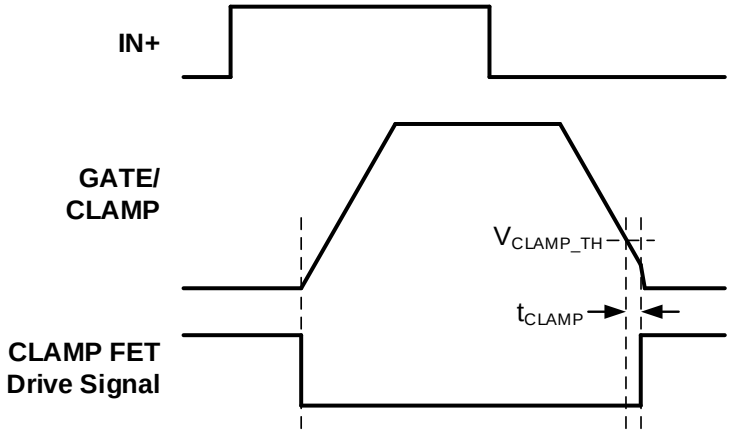


Figure 7: Active Miller Clamp during Normal Operation

DEVICE FUNCTION MODES

Table 2: Logic Truth Table for SOIC-8 Package (19) (20)

Inputs		Power Supply		Outputs		Notes
IN+	IN-	VDDI	VDDO	OUT	CLAMP	
Logic high	Logic low	Powered	Powered	Logic high	Hi-Z	Normal operation
Logic low or open	x	Powered	Powered	Logic low	Logic low	
x	Logic high or open	Powered	Powered	Logic low	Logic low	
x	x	Not powered	x	Logic low	Logic low	VDDI is not powered
x	x	Powered	Not powered	Logic low	Logic low	VDDO is not powered

Notes:

19) "x" means logic low, logic high, or open.
20) If VDDI is powered, the output can operate properly as long as VDDO is powered normally.

FUNCTIONAL BLOCK DIAGRAM

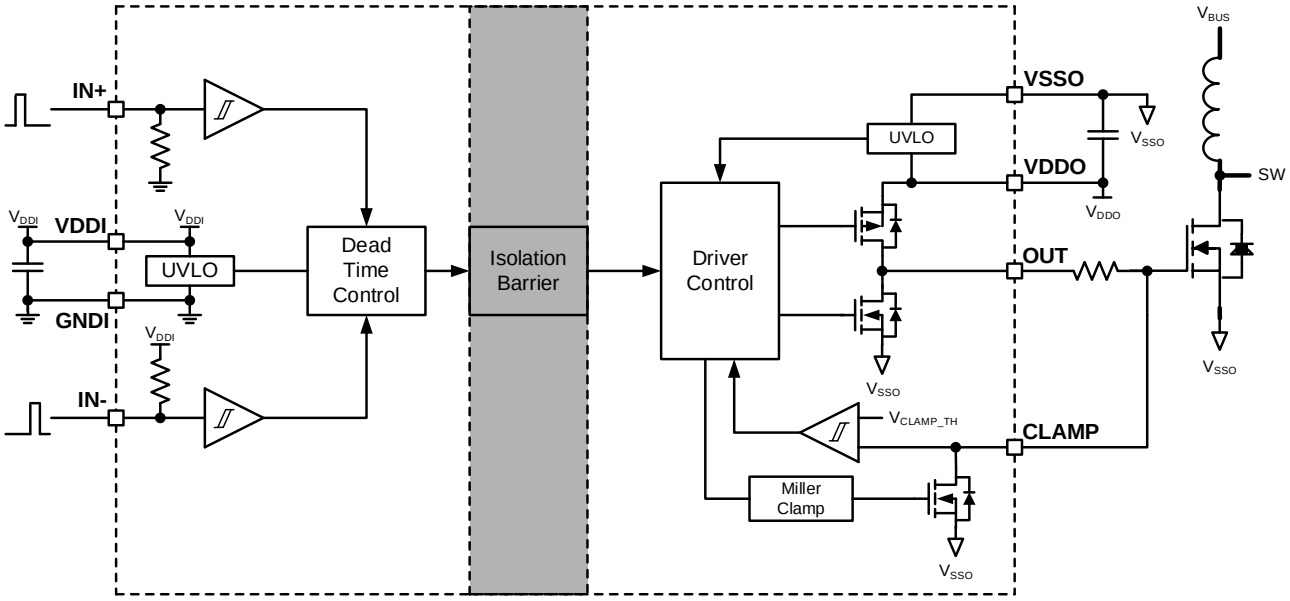


Figure 8: Functional Block Diagram

OPERATION

The MPQ18811 is an isolated, single-channel gate driver solution with up to 6A of source and up to 10A of sink peak current capacity. The gate driver is designed to drive power switching devices with short propagation delays and pulse-width distortion. With these advanced features, the MPQ18811 operates at high efficiency, with high power density and robustness in a wide variety of powered applications.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to avoid the chip or some blocks from operating at an insufficient supply voltage. The MPQ18811 incorporates an internal UVLO comparator for all input and output supply circuit blocks to monitor the VDDI voltage (V_{DDI}) and VDDO voltage (V_{DDO}). Figure 4 on page 19 shows the input and output supply UVLO time sequence diagram.

If the input bias voltage (V_{DDI}) is unpowered or is below the V_{DDI} UVLO threshold, the chip does not activate and the output stage does not receive the control signals from the input stage. Then the UVLO mechanism holds the output low, regardless of the present logic levels of the input control signals (IN+ and IN-).

When the driver's output stage is not powered or below the UVLO threshold, the driver's output is also pulled low by the internal active-low clamp circuitry, which restricts the voltage rise on the driver output (see Figure 9).

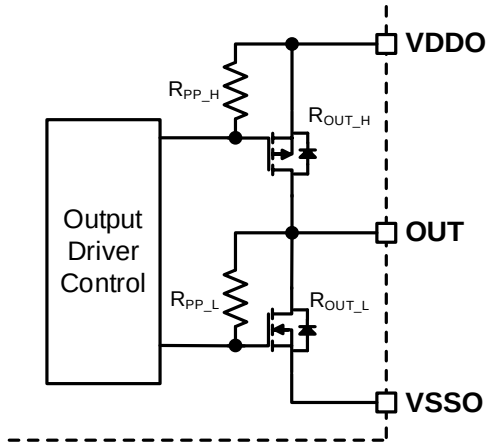


Figure 9: Output Stage and Active-Low Clamp Circuitry

The totem-pole output consists of an upper P-channel MOSFET and a lower N-channel MOSFET. The MOSFETs' gates are tied to the output stage supply and driver output via a high side pull-up resistance (R_{PP_H}) and a low side pull-up resistance (R_{PP_L}). When the bias power supply is unavailable (i.e. without drive signal) the upper MOSFET remains off to disconnect the driver output from the supply input while the lower MOSFET's gate is tied to the driver output through R_{PP_L}. This configuration prevents the driver output from exceeding the threshold voltage of the lower N-channel MOSFET device. Then the driver output is clamped to a very low level until the bias voltage returns to normal.

Input Stage

Both of the input control pins (IN+ and IN-) accept TTL/CMOS-compatible logic inputs that are reliably isolated from the driver output. These control pins can be easily driven with a common logic-level signal from a digital controller. However, any input signal applied to these control pins must not exceed the input stage supply (V_{DDI}). Tie VDDI to the same power supply as the control signal sources.

If the IN+ inputs are left open, they are forced to logic low through the internal pull-down resistors. The IN- pin is pulled up to VDDI and forced to logic high when it is floating. This configuration ensures the driver output remains low when the control input is not connected. If either logic input pin (IN+ or IN-) is not used, it is recommended to pull the pin up or down to a stable level externally for improved noise immunity and steady operation.

Output Stage

The output stage is comprised of an upper P-channel MOSFET and a lower N-channel MOSFET (see Figure 9). The effective output pull-up source resistance (R_{OUT_SOURCE}) is the upper P-channel MOSFET's on resistance, which delivers the large peak source current during the external power switch's turn-on transition. The pull-down structure is an N-channel MOSFET. The N-channel MOSFET's on resistance (R_{OUT_SINK}) is the effective output pull-down resistance when the driver's output is low.

The output stage is optimized to provide strong driving capacity to a powered device during the miller plateau interval of the switching on/off procedure. The MPQ18811 is capable of delivering 6A of source and 10A of sink peak current pulses. The rail-to-rail output ensures that the voltage is either V_{DDO} or the VSSO voltage (V_{SSO}).

Dead Time (DT) and Shoot-Through Protection

When the dual MPQ18811 devices are used in a half-bridge configuration with two opposite-polarity input pins, the single-channel driver can implement hardware interlocking to prevent cross conduction, even when the wrong input signals are generated by the MCU (see Figure 10).

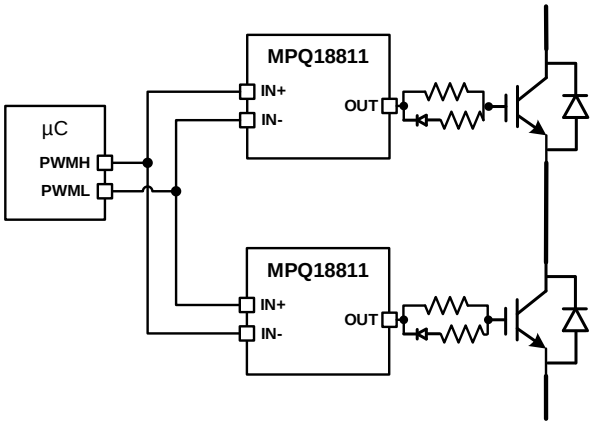


Figure 10: Dual Drivers in a Half-Bridge Configuration

In this half-bridge configuration, one driver output only goes high when its IN- input is low and the internal fixed dead time (DT) has expired. The MPQ18811 typically selects the longer delay time between the driver's DT and the input control signals' DT as the operating DT. Figure 11 shows IN+ and INT- DT control.

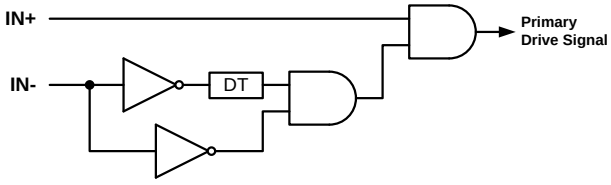


Figure 11: IN+ and IN- Dead Time Control

Active Miller Clamp

When the external power transistor is off, the driver operates to avoid the induced turn-on phenomenon that may occur when the other switch of the same leg turns on due to the miller capacitance.

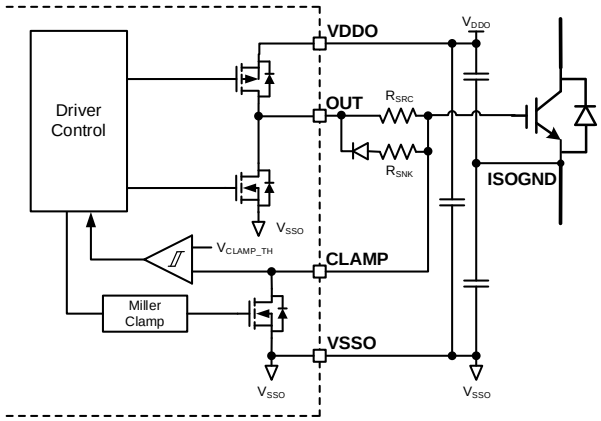


Figure 12: Active Miller Clamp

The CLAMP switch is activated when the gate voltage drops below the voltage threshold (V_{CLAMP_TH}), and creates a low impedance path between the switch gate and VSSO.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from operating at an exceedingly high temperature. When the silicon die temperature exceeds 170°C, the OTP shuts down the whole chip until the junction temperature (T_J) drops below its lower threshold, and then the chip restarts again. Both the primary-side and secondary-side feature thermal shutdown independently.

Common-Mode Transient Immunity (CMTI)

Common-mode transient immunity (CMTI) is one of the key characteristics that determines an isolator's robustness, and is especially important in high-voltage applications that utilize devices with fast transient response (e.g. SiC/GaN FETs). When a power device is switching, the high slew rate dv/dt or di/dt transient noise can corrupt the signal transmission across the isolation barrier (see Figure 13 and Figure 14 on page 25).

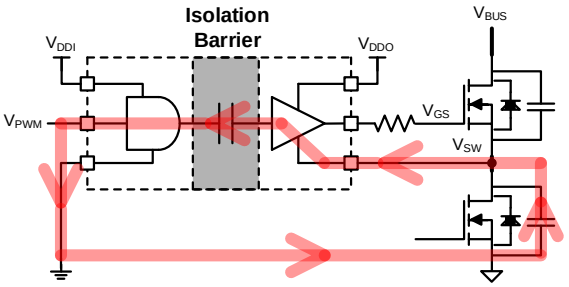


Figure 13: High Slew Rate Transient Noise Coupling Path

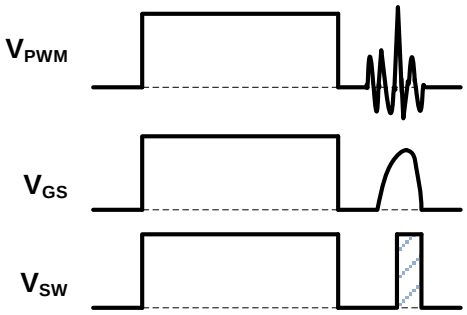


Figure 14: Abnormal Pulse Caused by Coupled Noise if dV/dt > CMTI

CMTI is defined as the maximum tolerable rate of rise/fall of a common-mode voltage applied between two isolated circuits, given in volts per second (V/ns or kV/μs). Below the maximum slew rate of a common-mode voltage, the isolator's output remains at the specified logic level and timing.

Figure 15 shows the CMTI test set-up to measure the CMTI of a coupler in both static and dynamic operation, under the specified common-mode pulse magnitude (V_{CM}), the specified slew rate for the common-mode pulse (dV_{CM}/dt), and other specified test or ambient conditions. The isolator's output should remain in the correct state as long as the pulse magnitude and the slew rate meet the CMTI specifications.

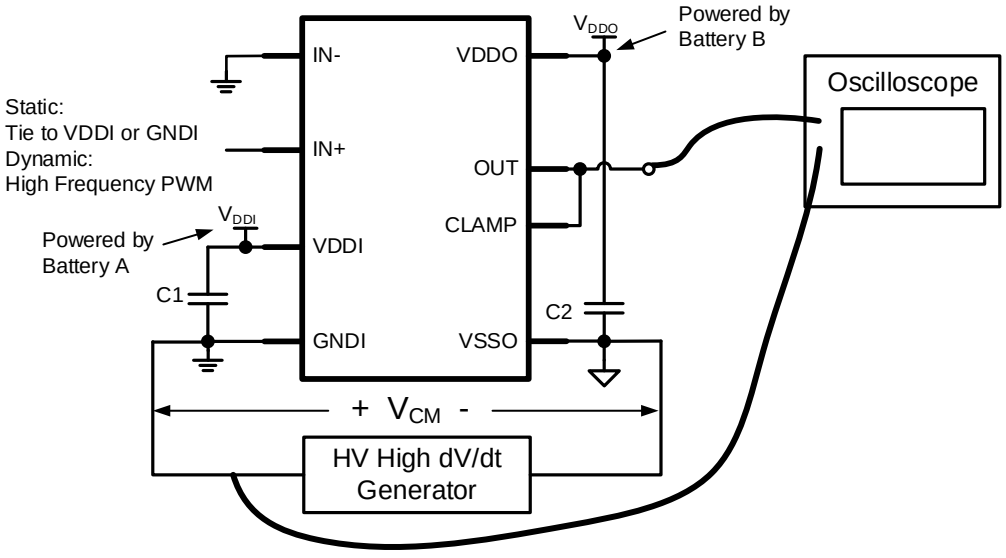


Figure 15: CMTI Test Set-Up

APPLICATION INFORMATION

Selecting the VDDI Capacitor

The VDDI capacitor (C_{VDDI}) reduces the surge current drawn from the input supply, and supports current consumption for the primary logic interface and transmitter block. Since the input side's operating current is only a few mA, a 100nF ceramic capacitor with X5R or X7R dielectrics is highly recommended due to its low ESR and small temperature coefficients. For most applications, if the real supply power is far away from the VDDI pin, then it is recommended to add a >1μF bypass capacitor in parallel with this 100nF ceramic capacitor.

Selecting the VDDO Capacitor

The VDDO capacitor (C_{VDDO}) is the bypass capacitor for the output gate driver. It supports current consumption for the driving control block, maintains a stable driving voltage, and supports up to 6A of transient source current.

Given that the allowable VDDO voltage (V_{DDO}) ripple (ΔV_{DDO}) guarantees that the driver supply voltage cannot drop close to the UVLO level, the minimum C_{VDDO} can be calculated with Equation (1):

$$C_{VDDO} = \frac{I_{VDDO} \times \frac{1}{f_{SW}} + Q_G}{\Delta V_{DDO}} \quad (1)$$

Where I_{VDDO} is the VDDO operating current, f_{SW} is the switching frequency, and Q_G is the power device's gate charge.

Note that the loop resistance, voltage drop, and DC bias voltage ripple impact the supply voltage. A 10μF ceramic capacitor is typically chosen. It is also recommended to place a secondary, high-frequency, 100nF bypass capacitor in parallel.

Selecting the IN+/IN- Input Filter

The IN+/IN- input filter is not necessary in theory, as the low-pass filter slows the pulse-width modulation (PWM) signal's rising/falling edge and affects the propagation delay. However, if there is significant high-frequency ringing introduced by the PCB traces, it is recommended to add a simple RC filter at the input, close to the IN+/IN- pin.

To avoid increasing the input resistance, a resistor below 100Ω is typically recommended. When selecting the filter capacitor, ensure that the filter's cutoff frequency is at least ten times greater than f_{SW}. A capacitance of dozens of pF is typically sufficient.

Selecting the External Driving Resistor

The external driving resistor can be applied to limit the ringing noise on the driving signal and adjust the switching speed to improve EMI performance. However, a higher driving resistance increases the switching losses, reduces system efficiency, and can introduce thermal issues. In actual applications, the turn-on and turn-off speeds can be adjusted via the respective driving resistors. Place the sink resistor in series with an anti-parallel diode, and keep it separate from the source resistor. The total driving resistance when pulling the power device low is the sum of the sink resistor in parallel with the source resistor.

The peak driving current can be used to evaluate the effect of the driving resistors. Without a driving resistor, the MPQ18811 can drive up to 6A/10A of peak source/sink currents.

Considering the driving resistor, the peak source driving current for the output (I_{OUT_SRC}) can be calculated with Equation (2):

$$I_{OUT\_SRC} = \frac{V_{DDO}}{R_{OUT\_H} + R_{G\_SRC} + R_{G\_INT}} \quad (2)$$

The peak sink driving current for the output (I_{OUT_SNK}) can be calculated with Equation (3):

$$I_{OUT\_SNK} = \frac{V_{GS\_ON}}{R_{OUT\_L} + R_{G\_SNK} + R_{G\_INT}} \quad (3)$$

Where R_{G_SRC} is the external source resistor, R_{G_SNK} is the external sink resistor, R_{G_INT} is the power device's internal gate resistance, and V_{GS_ON} is the power device's stable gate-source voltage during the turn-on interval.

V_{GS_ON} should typically be close to V_{DDO}.

Since the driving source current cannot exceed 6A, set the actual peak source driving current to be the smaller value between the estimated I_{OUT_SRC} and 6A. As for driving sink current, set

the actual peak source driving current to the smaller value between the estimated I_{OUT_SNK} and 10A.

Estimated Gate Driver Power Loss

The total gate driver power loss is used to estimate the thermal performance. The MPQ18811 must operate under the safety limiting values (see the Safety Limiting Values section on page 12 for more details).

To estimate the gate driver power loss, first the chip's operation power consumption (P_{OP}) can be calculated with Equation (4):

$$P_{OP} = V_{DDI} \times I_{VDDI} + V_{DDO} \times I_{VDDO} \quad (4)$$

The gate driver's self-power consumption is related to f_{SW} and the supply voltage. For the relationship reference between the input and output channel's current consumption vs. the operating frequency, see the Typical Characteristics section on page 14.

Next, consider the gate driver power loss during switching operation. As a conventional totem-pole gate driver, the MPQ18811 charges and discharges the power device's gate capacitance once during every switching cycle. During the charging and the discharging period, the total energy is supplied by VDDO. If there is no external gate driver resistor, the power dissipation (P_{SW}) can be calculated with Equation (5):

$$\begin{aligned} P_{SW} &= V_{DDO} \times \int_0^{t_{ON}} i_G(t)dt \times f_{SW} \\ &= V_{DDO} \times Q_G \times f_{SW} \end{aligned} \quad (5)$$

Where t_{ON} is the turn-on time, and $I_G(t)$ is the driving current.

The behavior of the external source/sink resistors adds complexity to the dynamic power dissipation estimation.

If the driving current is not saturated to 6A/10A within one switching cycle with the external gate resistors, then P_{SW} is shared between the gate driver's internal source/sink resistors and the external gate driver resistors, based on the ratio of these series resistances. Under these circumstances, P_{SW} can be calculated with Equation (6):

$$P_{SW} = \frac{V_{DDO} \times Q_G \times f_{SW}}{2} \times \left(\frac{R_{OUT\_H}}{R_{OUT\_H} + R_{G\_SRC} + R_{G\_INT}} + \frac{R_{OUT\_L}}{R_{OUT\_L} + R_{G\_SNK} + R_{G\_INT}} \right) \quad (6)$$

In some conditions, the MPQ18811 outputs the saturated 6A/10A current at the beginning of the turn-on/off interval. During this saturation time, the power loss (P_{SW_SAT}) can be calculated with Equation (7):

$$\begin{aligned} P_{SW\_SAT} = 6A \times & \int_0^{t_{ON\_SAT}} \left(V_{DDO} - V_{GS}(t)\right)dt \\ +10A \times & \int_0^{t_{OFF\_SAT}} \left(V_{GS}(t)\right)dt \end{aligned} \quad (7)$$

Where t_{ON_SAT}/t_{OFF_SAT} are the turn-on/turn-off times with a saturated 6A/10A current output, and $V_{GS}(t)$ is the power device's gate voltage during this saturation time.

The actual power loss is the sum of Equation (4) and Equation (5). Therefore, the total power loss dissipated in the MPQ18811 (P_{LOSS}) can be calculated with Equation (8):

$$P_{LOSS} = P_{OP} + P_{SW} \quad (8)$$

Multiply P_{LOSS} by the junction-to-ambient thermal resistance (θ_{JA}) to determine the junction temperature (T_J) rise above the ambient temperature. Ensure that T_J is below the maximum safety temperature (T_S).

Adding a Ferrite Bead (FB) for the Gate Driver Circuit

As f_{SW} and the power increase, the fast switching speed increases the dV/dt and spike. This results in serious noise introduced by the gate node. Unpredictable driver operating conditions may occur due to this noise.

To solve this potential problem, it is recommended to add a ferrite bead (FB) in the driving circuit (see Figure 16).

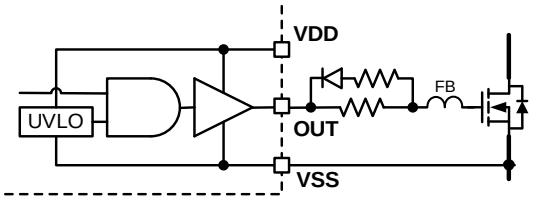


Figure 16: Adding a Ferrite Bead

An FB shows the low impedance characteristic at low frequencies; therefore, it has no effect on the driving signal. For high-frequency noise signals, an FB exhibits high-impedance characteristics and can greatly attenuate noisy signals. An FB can be used in series with traditional gate resistors. It should be placed between the gate resistors and FET, and as close to the FET as possible.

There are two key factors when selecting the FB: the rated current and the frequency characteristics.

The first factor is the rated current, which is recommended to be twice the source/sink peak current.

The frequency characteristic is the second key factor. For example, Figure 17 shows a typical impedance plot from TDK MPZ2012S221ATD25. There are three lines: the overall impedance (Z), the inductive component of the impedance (X), and the resistive component (R).

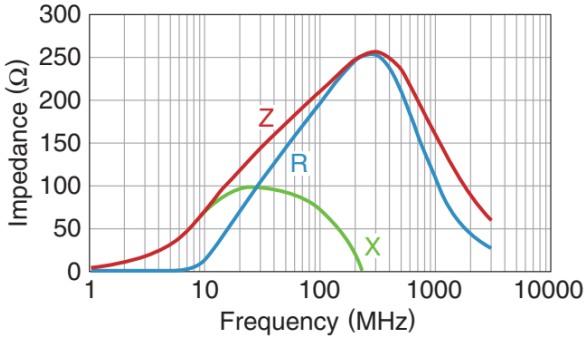


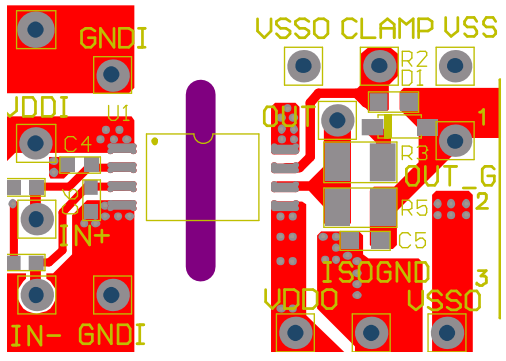
Figure 17: Typical Impedance Plot from TDK MPZ2012S221ATD25

To cover most gate driver applications, this FB should have a very low impedance characteristic at f_{SW}, such as <1MHz. For the frequency bands in which the noise is present, the FB must have high-impedance characteristics (typically about 100MHz).

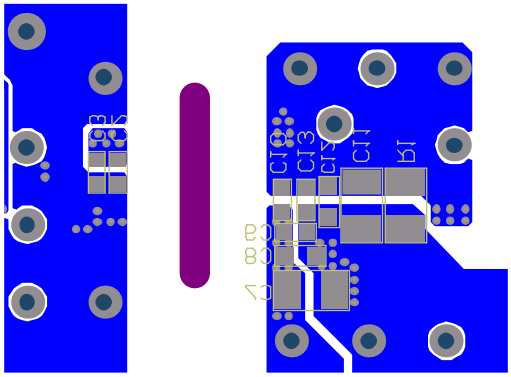
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 18 and follow the guidelines below:

1. Place the bypass/decoupling capacitors as close to the VDDI/VDDO supply pins and the corresponding grounds as possible.
2. It is recommended to add a low-ESR/ESL, high-frequency, 100nF bypass capacitor on each supply pin.
3. If an RC input filter is used, it is recommended to place this filter close to the corresponding control pin.
4. Place the high-current paths (e.g. the supply path, drive path, and the connection between the external power device source and the VSSO pin) very close to the driver chip using short, direct, and wide traces to minimize the parasitic inductance, and to avoid large transients and ringing noise.
5. It is strongly recommended to place large power and ground planes — or multiple ground layers — to help dissipate heat from the gate driver chip to the PCB, improving thermal performance. Ensure to allow for sufficient insulation distance between the different low/high-voltage planes when splitting the traces or coppers.
6. Ensure the driving loop is small between OUT, the power device's gate-to-source voltage, and the VSSO short.
7. Avoid placing the driving trace across different PCB layers using vias, as it can introduce parasitic inductance.
8. Place the driver IC as close to the power device as possible.
9. Use the recommended land pattern design for each package type to ensure adequate insulation space between the primary and secondary sides.
10. Avoid placing any components, tracks, or copper below the chip's body in any PCB layer.
11. A board cutout under the chip is recommended to extend the creepage distance on the PCB surface.



Top Layer



Bottom Layer

Figure 18: Recommended PCB Layout (21)

Note:

21) This example uses a 2-layer PCB layout.

TYPICAL APPLICATION CIRCUIT

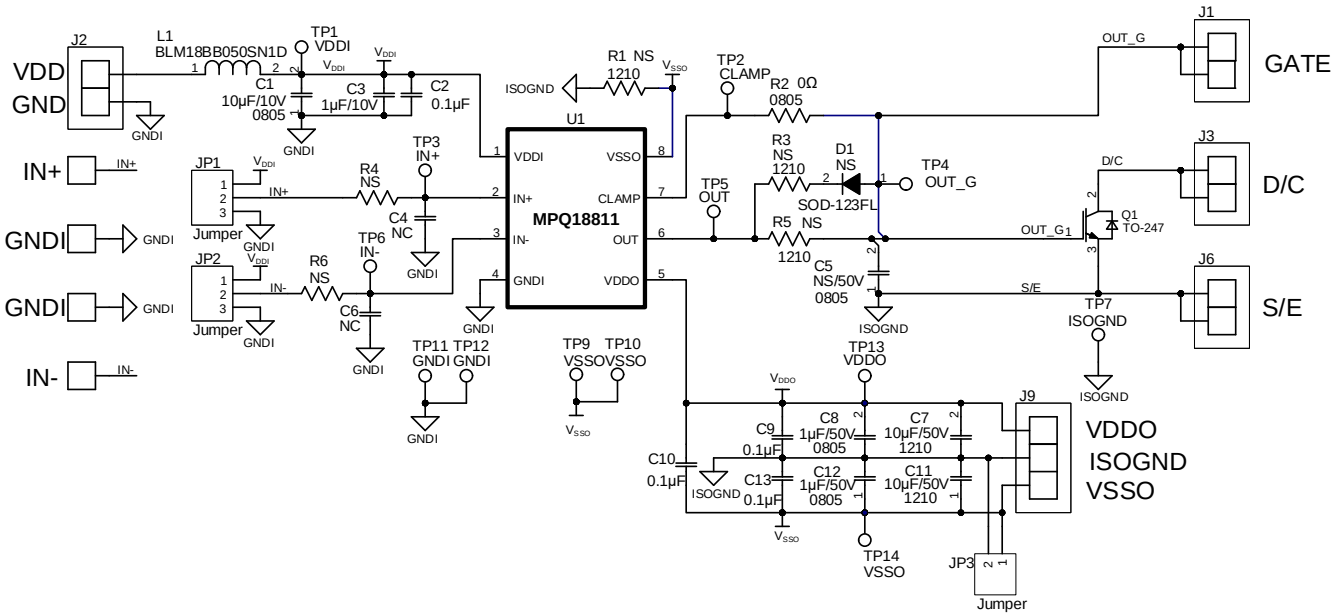
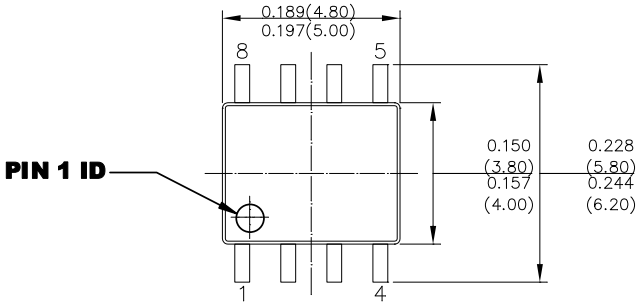


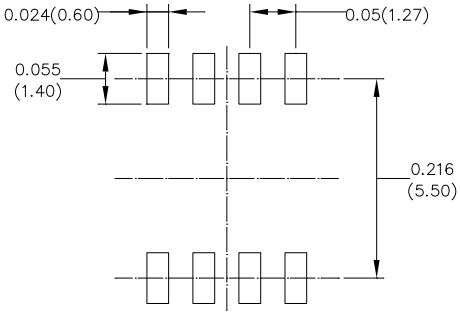
Figure 19: Typical Application Circuit

PACKAGE INFORMATION

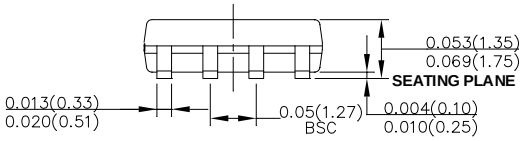
SOIC-8 NB (HV Isolation)



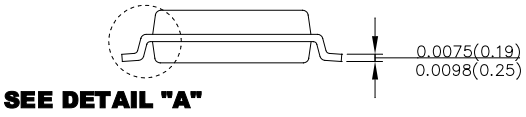
TOP VIEW



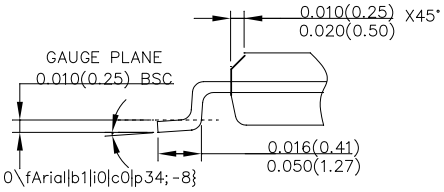
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



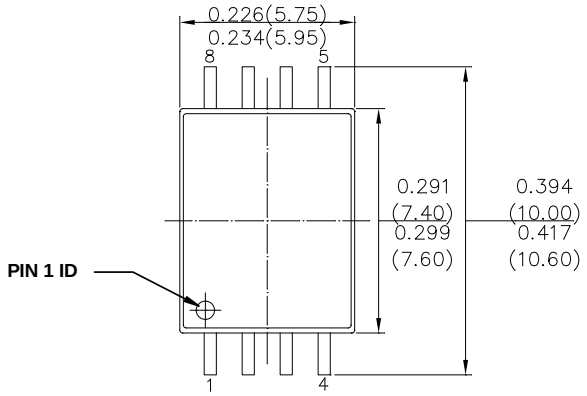
DETAIL "A"

NOTE:

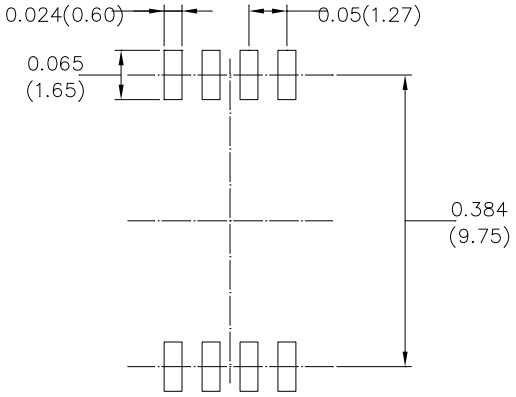
1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING REFERENCE TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

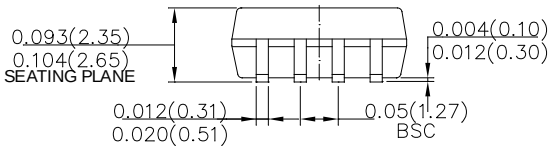
SOIC-8 WB (HV Isolation)



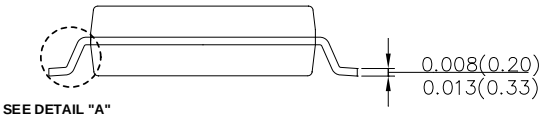
TOP VIEW



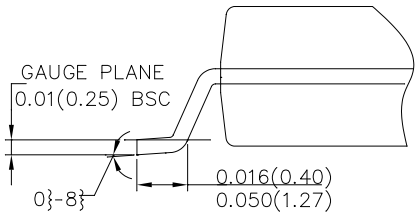
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



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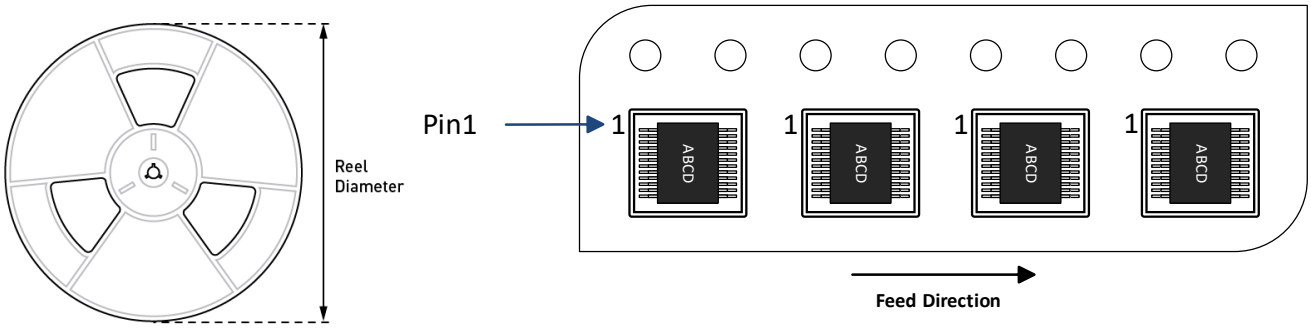
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ18811-10CGS-AEC1-Z	SOIC-8 NB	2500	N/A	N/A	13in	12mm	8mm
MPQ18811-10EGS-AEC1-Z							
MPQ18811-10FGS-AEC1-Z							
MPQ18811-10CGY-AEC1-Z	SOIC-8 WB	1000	N/A	N/A	13in	16mm	12mm
MPQ18811-10EGY-AEC1-Z							
MPQ18811-10FGY-AEC1-Z							

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/4/2024	Initial Release	-