MPQ18851

Isolated Dual-Input Control Independent Dual-Channel Gate Driver AEC-Q100 Qualified

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MPQ18851 is an isolated dual-channel gate driver solution with up to 4A source and 8A sink peak current capacity. The gate driver is designed to drive power switching devices with short propagation delay and pulse-width distortion. By utilizing MPS proprietary capacitive-based isolation technology, the driver can provide up to $5kV_{RMS}$ withstand voltage (per UL 1577) with SOIC wide-body package and greater than 150kV/μs common-mode transient immunity (CMTI) rating between the input side and output driver. With the advanced features, the drivers operate high efficiency, high power density, and robustness in a wide variety of automotive power applications.

The MPQ18851 integrates fully independent dual gate drivers in one package. Each output can be grounded to the separated grounds or connected to a positive or negative voltage reference. The secondary topology can be configured as a half-bridge high-side/low-side driver or dual drivers controlled respectively by two independent input signals.

A wide primary-side VDDI supply range makes the driver suitable to be interfaced with 3.3V or 5V digital controllers. And the secondary-side driver accepts up to 30V supply. All the supply voltage pins are with various under voltage lock-out (UVLO) level protection.

The MPQ18851 is available in narrow-/wide-body SOIC-16, wide-body SOIC16-14 and LGA-13 5mmx5mm packages.

FEATURES

- Dual-Input Independent Dual-Channel Driver
- Up to $5kV_{RMS}$ Input to Output Reinforced Isolation (Wide-body SOIC)
- $1850V_{DC}$ Functional Isolation between Two Secondary-Side Drivers (SOIC16-14 WB)
- $1500V_{DC}$ Functional Isolation between Two Secondary-Side Drivers (SOIC-16 NB/WB)
- $700V_{DC}$ Functional Isolation between Two Secondary-Side Drivers (LGA-13 5mmx5mm)
- Common-Mode Transient Immunity (CMTI) >150kV/μs
- 2.8V to 5.5V Input VDDI Range to Interface with TTL and CMOS Compatible Inputs
- Up to 30V Output Drive Supply with Several UVLO Options
- 4A Source, 8A Sink Peak Current Output
- 50ns Typical Propagation Delay with Tiny ±5ns Distribution from Part to Part
- Operating Junction Temperature Range -40°C to +150°C
- AEC-Q100 Grade 1 Qualified
- UL 1577 Certified
  - SOIC NB: $3kV_{RMS}$ Isolation for 60s
  - SOIC WB: $5kV_{RMS}$ Isolation for 60s
  - LGA: $2.5kV_{RMS}$ Isolation for 60s
- DIN EN IEC 60747-17 (VDE 0884-17): 2021-10 Certified (pending)
- CQC Certification per GB4943.1-2011 (pending)

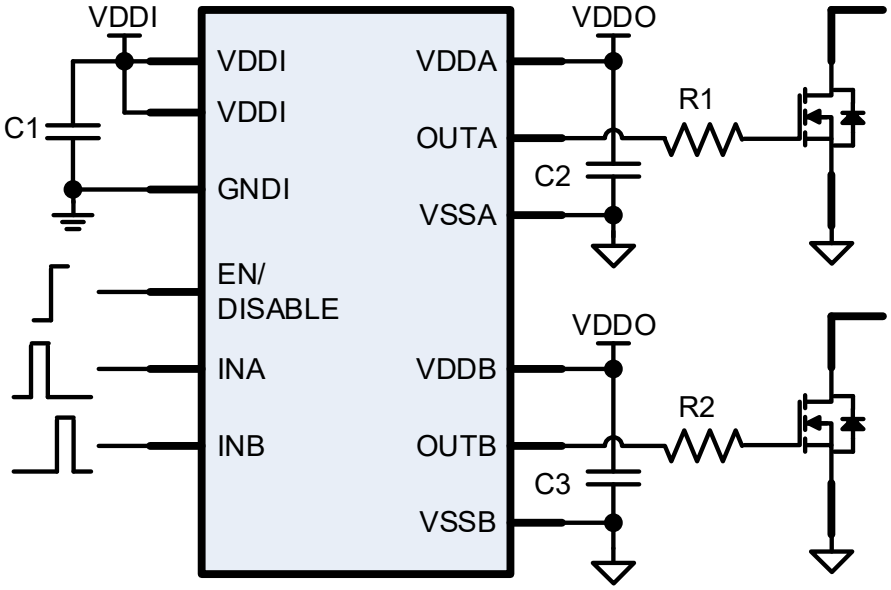
APPLICATIONS

- EV/HEV Motor Drive Inverters
- On-Board Chargers
- Half/Full-Bridge Converters
- Isolated DC/DC Converters
- Offline Isolated AC/DC Converters
- DC/AC Inverters

SELECTION GUIDE

Part Number	Peak Sink Current (A)	Output UVLO (V)	On/Off Logic	Input Logic	Configura -tion	Overlap Protection	Programm -able Dead-Time	Package Type
MPQ18851-6B	6	5	EN	INA/INB	Dual Drivers	--	--	SOIC-16 NB SOIC-16 WB SOIC16-14 WB LGA-13 (5mmx5mm)
MPQ18851-8B	8							
MPQ18851-6C	6	8						
MPQ18851-8C	8							
MPQ18851-6D	6	10						
MPQ18851-8D	8							
MPQ18851-6E	6	12						
MPQ18851-8E	8							
MPQ18851-6F	6	15						
MPQ18851-8F	8							
MPQ18851-A6B	6	5	DIS	INA/INB	Dual Drivers	--	--	SOIC-16 NB SOIC-16 WB SOIC16-14 WB LGA-13 (5mmx5mm)
MPQ18851-A8B	8							
MPQ18851-A6C	6	8						
MPQ18851-A8C	8							
MPQ18851-A6D	6	10						
MPQ18851-A8D	8							
MPQ18851-A6E	6	12						
MPQ18851-A8E	8							
MPQ18851-A6F	6	15						
MPQ18851-A8F	8							

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*/***	Package	Top Marking	MSL Rating**
MPQ18851-6BGSE-AEC1	SOIC-16 NB	*See Below*	2
MPQ18851-8BGSE-AEC1		*See Below*	
MPQ18851-6CGSE-AEC1		*See Below*	
MPQ18851-8CGSE-AEC1		*See Below*	
MPQ18851-6DGSE-AEC1		*See Below*	
MPQ18851-8DGSE-AEC1		*See Below*	
MPQ18851-6EGSE-AEC1		*See Below*	
MPQ18851-8EGSE-AEC1		*See Below*	
MPQ18851-6FGSE-AEC1		*See Below*	
MPQ18851-8FGSE-AEC1		*See Below*	
MPQ18851-6BGY-AEC1	SOIC-16 WB	*See Below*	3
MPQ18851-8BGY-AEC1		*See Below*	
MPQ18851-6CGY-AEC1		*See Below*	
MPQ18851-8CGY-AEC1		*See Below*	
MPQ18851-6DGY-AEC1		*See Below*	
MPQ18851-8DGY-AEC1		*See Below*	
MPQ18851-6EGY-AEC1		*See Below*	
MPQ18851-8EGY-AEC1		*See Below*	
MPQ18851-6FGY-AEC1		*See Below*	
MPQ18851-8FGY-AEC1		*See Below*	
MPQ18851-6BGYE-AEC1	SOIC16-14 WB	*See Below*	3
MPQ18851-8BGYE-AEC1		*See Below*	
MPQ18851-6CGYE-AEC1		*See Below*	
MPQ18851-8CGYE-AEC1		*See Below*	
MPQ18851-6DGYE-AEC1		*See Below*	
MPQ18851-8DGYE-AEC1		*See Below*	
MPQ18851-6EGYE-AEC1		*See Below*	
MPQ18851-8EGYE-AEC1		*See Below*	
MPQ18851-6FGYE-AEC1		*See Below*	
MPQ18851-8FGYE-AEC1		*See Below*	
MPQ18851-6BGLU-AEC1	LGA-13 (5mmx5mm)	*See Below*	3
MPQ18851-8BGLU-AEC1		*See Below*	
MPQ18851-6CGLU-AEC1		*See Below*	
MPQ18851-8CGLU-AEC1		*See Below*	
MPQ18851-6DGLU-AEC1		*See Below*	
MPQ18851-8DGLU-AEC1		*See Below*	
MPQ18851-6EGLU-AEC1		*See Below*	
MPQ18851-8EGLU-AEC1		*See Below*	
MPQ18851-6FGLU-AEC1		*See Below*	
MPQ18851-8FGLU-AEC1		*See Below*	

ORDERING INFORMATION *(continued)*

Part Number*/***	Package	Top Marking	MSL Rating**
MPQ18851-A6BGSE-AEC1	SOIC-16 NB	*See Below*	2
MPQ18851-A8BGSE-AEC1		*See Below*	
MPQ18851-A6CGSE-AEC1		*See Below*	
MPQ18851-A8CGSE-AEC1		*See Below*	
MPQ18851-A6DGSE-AEC1		*See Below*	
MPQ18851-A8DGSE-AEC1		*See Below*	
MPQ18851-A6EGSE-AEC1		*See Below*	
MPQ18851-A8EGSE-AEC1		*See Below*	
MPQ18851-A6FGSE-AEC1		*See Below*	
MPQ18851-A8FGSE-AEC1		*See Below*	
MPQ18851-A6BGY-AEC1	SOIC-16 WB	*See Below*	3
MPQ18851-A8BGY-AEC1		*See Below*	
MPQ18851-A6CGY-AEC1		*See Below*	
MPQ18851-A8CGY-AEC1		*See Below*	
MPQ18851-A6DGY-AEC1		*See Below*	
MPQ18851-A8DGY-AEC1		*See Below*	
MPQ18851-A6EGY-AEC1		*See Below*	
MPQ18851-A8EGY-AEC1		*See Below*	
MPQ18851-A6FGY-AEC1		*See Below*	
MPQ18851-A8FGY-AEC1		*See Below*	
MPQ18851-A6BGYE-AEC1	SOIC16-14 WB	*See Below*	3
MPQ18851-A8BGYE-AEC1		*See Below*	
MPQ18851-A6CGYE-AEC1		*See Below*	
MPQ18851-A8CGYE-AEC1		*See Below*	
MPQ18851-A6DGYE-AEC1		*See Below*	
MPQ18851-A8DGYE-AEC1		*See Below*	
MPQ18851-A6EGYE-AEC1		*See Below*	
MPQ18851-A8EGYE-AEC1		*See Below*	
MPQ18851-A6FGYE-AEC1		*See Below*	
MPQ18851-A8FGYE-AEC1		*See Below*	
MPQ18851-A6BGLU-AEC1	LGA-13 (5mmx5mm)	*See Below*	3
MPQ18851-A8BGLU-AEC1		*See Below*	
MPQ18851-A6CGLU-AEC1		*See Below*	
MPQ18851-A8CGLU-AEC1		*See Below*	
MPQ18851-A6DGLU-AEC1		*See Below*	
MPQ18851-A8DGLU-AEC1		*See Below*	
MPQ18851-A6EGLU-AEC1		*See Below*	
MPQ18851-A8EGLU-AEC1		*See Below*	
MPQ18851-A6FGLU-AEC1		*See Below*	
MPQ18851-A8FGLU-AEC1		*See Below*	

* For Tape & Reel, add suffix -Z (e.g. MPQ18851-6BGSE-AEC1-Z)

** Moisture Sensitivity Level Rating

*** Under qualification

Please contact local sales or our distributors to check the latest availability status for the ordering part numbers.

TOP MARKING

MPQ18851-nX (SOIC-16 NB, SOIC-16 WB & SOIC16-14 WB)

MPS YYWW

M18851-nX

LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
M18851-nX: Part number
n: Output peak sink current rating, where n=6 or 8
X: UVLO level code, where X= B, C, D, E or F
LLLLLLLLL: Lot number

TOP MARKING

MPQ18851-AnX (SOIC-16 NB, SOIC-16 WB & SOIC16-14 WB)

MPS YYWW

18851-AnX

LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
M18851-AnX: Part number
n: Output peak sink current rating, where n=6 or 8
X: UVLO level code, where X= B, C, D, E or F
LLLLLLLLL: Lot number

TOP MARKING

MPQ18851-nX (LGA-13 5mmx5mm)

MPSYYWW

MP18851

LLLLLLL

nX

MPS: MPS prefix
YY: Year code
WW: Week code
MP18851: Part number
LLLLLLL: Lot number
nX: The rest alphanumeric characters of part number
n: Output peak sink current rating, where n=6 or 8
X: UVLO level code, where X= B, C, D, E or F

TOP MARKING

MPQ18851-AnX (LGA-13 5mmx5mm)

MPSYYWW

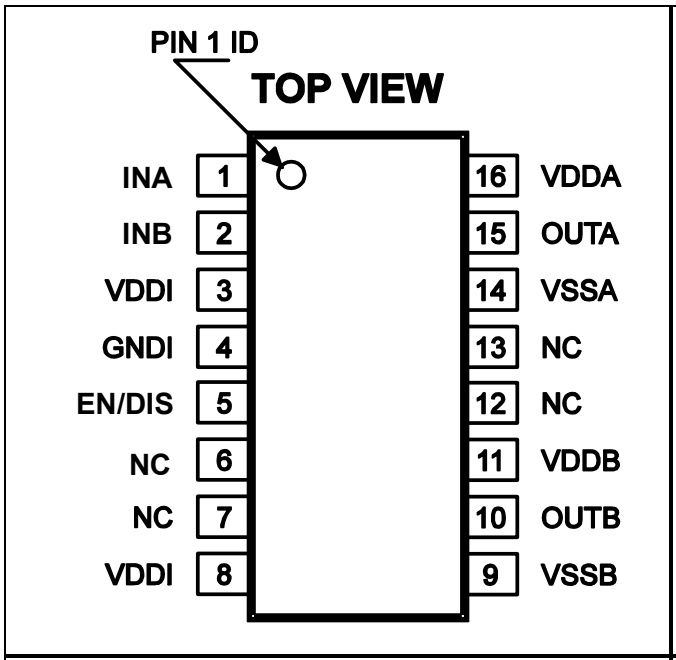
MP18851

LLLLLLL

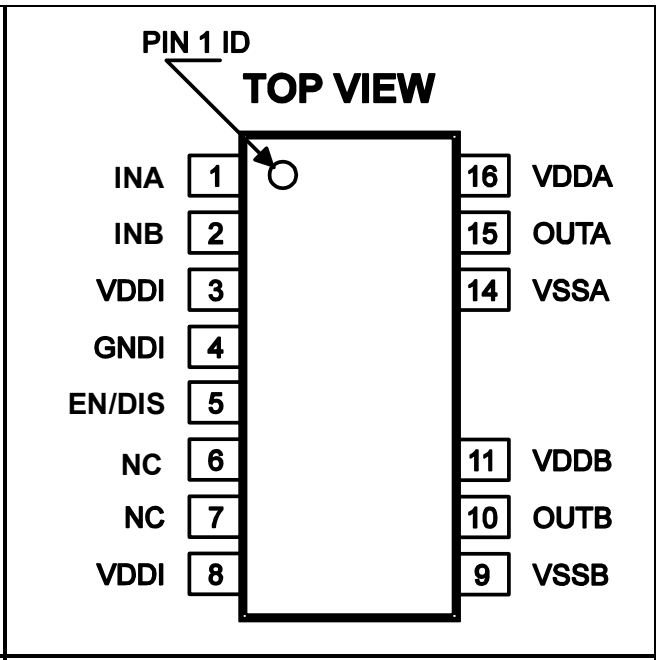
AnX

MPS: MPS prefix
YY: Year code
WW: Week code
MP18851: Part number
LLLLLLL: Lot number
AnX: The rest alphanumeric characters of part number
n: Output peak sink current rating, where n=6 or 8
X: UVLO level code, where X= B, C, D, E or F

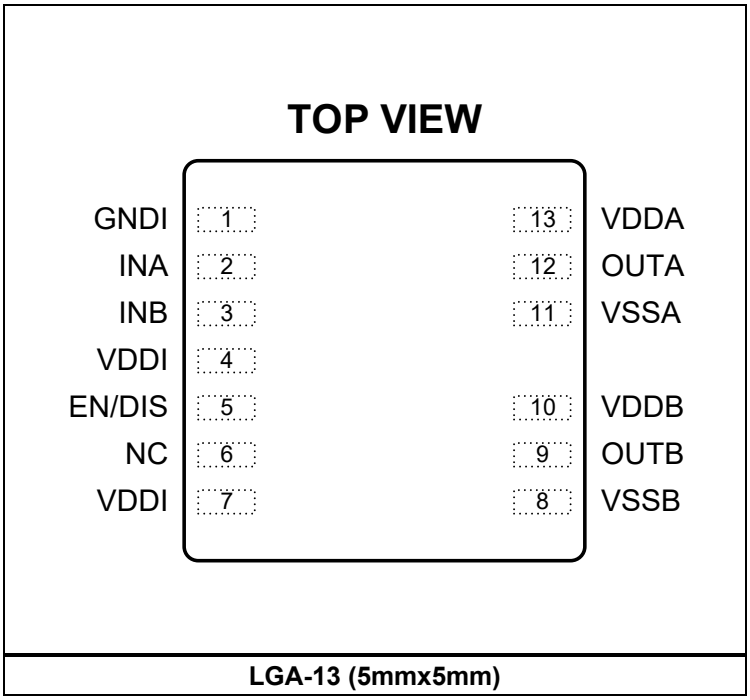
PACKAGE REFERENCE



SOIC-16 NB/SOIC-16 WB



SOIC16-14 WB



LGA-13 (5mmx5mm)

PIN FUNCTIONS

Pin #		Name	Description
SOIC	LGA		
1	2	INA	**Non-Inverting Logic Control Signal Input for Driver A.** INA pin can accept a TTL/CMOS level compatible input logic. This pin is internally pulled down to GNDI. It is recommended to tie this pin to GNDI if not used.
2	3	INB	**Non-Inverting Logic Control Signal Input for Driver B.** INB pin can accept a TTL/CMOS level compatible input logic. This pin is internally pulled down to GNDI. It is recommended to tie this pin to GNDI if not used.
3,8	4,7	VDDI	**Input-Side Power Supply Input.** These two pins are internally shorted. VDDI supplies power to the primary side control circuitry. Locally decoupled to GNDI using a low ESR/ESL bypass capacitor. The capacitor should be placed as close to the chip as possible.
4	1	GNDI	**Input-Side Ground.** Ground reference for all input-side signal and internal control blocks.
5	5	EN	**On/Off Control Input.** EN pin can be driven by an external TTL/CMOS level compatible input logic signal to enable/disable the chip. This pin is internally pulled high. Turn on the chip if set high or left open, shutdown the driver output if pulled low.
5	5	DIS	**On/Off Control Input.** DIS pin can be driven by an external TTL/CMOS level compatible input logic signal to enable/disable the chip. This pin is internally pulled low. Turn on the chip if set low or left open, shutdown the driver output if pulled high.
6,7,12,13	6	NC	**No Connection.**
9	8	VSSB	**Output-Side Ground for Driver B.** Ground reference for output driver B.
10	9	OUTB	**Gate Drive Output of Driver B.** Connect to the gate of power device in channel B.
11	10	VDDB	**Output-Side Driver Power Supply Input for Driver B.** This pin supplies power to the secondary side driver B circuitry. Locally decoupled to VSSB using a low ESR/ESL bypass capacitor. The capacitor should be placed as close to the chip as possible.
14	11	VSSA	**Output-Side Ground for Driver A.** Ground reference for output driver A.
15	12	OUTA	**Gate Drive Output of Driver A.** Connect to the gate of power device in channel A.
16	13	VDDA	**Output-Side Driver Power Supply Input for Driver A.** This pin supplies power to the secondary side driver A circuitry. Locally decoupled to VSSA using a low ESR/ESL bypass capacitor. The capacitor should be placed as close to the chip as possible.

ABSOLUTE MAXIMUM RATINGS (1)

VDDI-GNDI ..... -0.3V to 6.5V
V_{INA}, V_{INB}, $V_{EN/DIS}$,
..... (GNDI-0.3V) to (VDDI+0.3V)
V_{INA}, V_{INB}, $V_{EN/DIS}$ Transient for 50ns
..... (GNDI-5.0V) to (VDDI+0.3V)
VDDA-VSSA, VDDB-VSSB ..... -0.3V to 35V
V_{OUTA}..... (VSSA-0.3V) to (VDDA+0.3V)
V_{OUTA} Transient for 200ns
..... (VSSA-2.0V) to (VDDA+0.3V)
V_{OUTB}..... (VSSB-0.3V) to (VDDB+0.3V)
V_{OUTB} Transient for 200ns
..... (VSSB-2.0V) to (VDDB+0.3V)
VSSA-VSSB
SOIC NB/WB..... -1500V to +1500V
LGA-13 (5mmx5mm) ..... -700V to +700V
Continuous Power Dissipation (T_A = +25°C) (2)
SOIC-16 NB 2115mW
SOIC-16 WB 2215mW
SOIC16-14 WB 2215mW
LGA-13 (5mmx5mm) 1175mW
Junction Temperature..... 150°C
Lead Temperature ..... 260°C
Storage Temperature..... -65°C to +150°C

ESD Ratings

ESD Capability Human Body Mode (3)..... 4kV
CDM ESD Capability (4)..... 2kV

Recommended Operating Conditions (5)

VDDI-GNDI ..... 2.8V to 5.5V
V_{INA}, V_{INB}, $V_{EN/DIS}$..... GNDI to VDDI
VDDA-VSSA, VDDB-VSSB
..... 6.5V to 30V (5V UVLO rev.)
..... 9.2V to 30V (8V UVLO rev.)
..... 12V to 30V (10V UVLO rev.)
..... 14.5V to 30V (12V UVLO rev.)
..... 17.5V to 30V (15V UVLO rev.)
Operating Junction Temp. (T_J) .-40°C to +150°C

Thermal Resistance (6)

	θ_{JA}	θ_{JC}	
SOIC-16 NB	59	35	°C/W
SOIC-16 WB	56	30	°C/W
SOIC16-14 WB	56	30	°C/W
LGA-13 (5mmx5mm)	106	45	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AECQ100-002.
4) Per AECQ100-011.
5) The device is not guaranteed to function outside of its operating conditions.
6) Measured on MP(Q)18851 evaluation board, 2-layer PCB.

ELECTRICAL CHARACTERISTICS

2.8V ≤ VDDI-GNDI ≤ 5.5V, VDDA-VSSA = VDDB-VSSB = 12V/15V/20V (7), T_J = -40°C to +150°C, typical value is tested at T_J = +25°C, all voltages with respect to the corresponding grounds, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Side Supply Voltage						
VDDI Under-Voltage Lockout Threshold	$VDDI_{UVLO}$	(VDDI-GNDI) falling	2.42	2.6	2.78	V
VDDI Under-Voltage Lockout Hysteresis	$VDDI_{UVLO\_HYS}$		100	120	140	mV
Input Side Supply Current						
VDDI Shutdown Current	I_{VDDI_SD}	V_{EN}=GNDI or V_{DIS}=VDDI		1.0	1.5	mA
VDDI Quiescent Current	I_{VDDI_Q}	V_{EN}=VDDI or V_{DIS}=GNDI, $V_{INA/INB}$=GNDI		1.0	1.5	mA
VDDI Operation Current	I_{VDDI}	f=500kHz, 50% duty, C_{LOAD}=100pF		2.0	2.5	mA
Logic Input (INA, INB, EN/DIS)						
Logic Input High Threshold	V_{LI_H}	(V_{LI}-GNDI) rising		1.8	2.0	V
Logic Input Low Threshold	V_{LI_L}	(V_{LI}-GNDI) falling	0.8	1.2		V
Logic Input Hysteresis Voltage	V_{LI_HYS}		560	600	640	mV
Internal Pull-Up Resistance	R_{LI_PU}	EN to VDDI		200		kΩ
Internal Pull-Down Resistance	R_{LI_PD}	INA/INB/DIS to GNDI		200		kΩ
Output Side Supply Voltage						
VDDA/VDDB Under-Voltage Lockout Threshold (VDDA-VSSA)/(VDDB-VSSB) falling	$VDDA_{UVLO}$ $VDDB_{UVLO}$	-B, 5V threshold	5	5.5	6	V
		-C, 8V threshold	7.5	8	8.5	V
		-D, 10V threshold	9.3	10	10.7	V
		-E, 12V threshold	11	12	13	V
		-F, 15V threshold	13.8	15	16.2	V
VDDA/VDDB Under-Voltage Lockout Hysteresis	$VDDA_{UVLO\_HYS}$ $VDDB_{UVLO\_HYS}$	-B, 5V threshold	200	300	400	mV
		-C, 8V threshold	400	500	600	mV
		-D/-E/-F, 10V/12V/15V threshold	0.8	1	1.2	V
Output Side Supply Current						
VDDA/VDDB Shutdown Current	I_{VDDA_SD} I_{VDDB_SD}	V_{EN}=GNDI or V_{DIS}=VDDI		1.0	1.5	mA
VDDA/VDDB Quiescent Current (current per channel)	I_{VDDA_Q} I_{VDDB_Q}	V_{EN}=VDDI or V_{DIS}=GNDI, $V_{INA/INB}$=GNDI		1.0	1.5	mA

ELECTRICAL CHARACTERISTICS *(continued)*

2.8V ≤ VDDI-GNDI ≤ 5.5V, VDDA-VSSA = VDDB-VSSB = 12V/15V/20V [7], T_J = -40°C to +150°C, typical value is tested at T_J = +25°C, all voltages with respect to the corresponding grounds, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Output Side Supply Current *(continued)*						
VDDA/VDDB Operation Current (current per channel)	I_{VDDA} I_{VDDB}	f=500kHz,C_{LOAD}=100pF, VDDA-VSSA= VDDB-VSSB=12V		3.0	3.5	mA
		f=500kHz,C_{LOAD}=100pF, VDDA-VSSA= VDDB-VSSB=15V		3.5	4.0	mA
		f=500kHz,C_{LOAD}=100pF, VDDA-VSSA= VDDB-VSSB=20V		3.9	4.3	mA
Gate Driver						
Logic High Output Voltage	V_{OUTA_H} V_{OUTB_H}	$I_{OUTA/OUTB}$=-200mA	VDDA/ VDDB -0.5	VDDA/ VDDB -0.24		V
Logic Low Output Voltage	V_{OUTA_L} V_{OUTB_L}	6A rev., $I_{OUTA/OUTB}$=200mA		VSSA/ VSSB +86	VSSA/ VSSB +180	mV
		8A rev., $I_{OUTA/OUTB}$=200mA		VSSA/ VSSB +70	VSSA/ VSSB +146	mV
		VDDA/VDDB open/unpowered, $I_{OUTA/OUTB}$=1A		VSSA/ VSSB +1.5	VSSA/ VSSB +2.0	V
Output Peak Source Current	I_{OUTA_SRC} I_{OUTB_SRC}	VDDA-VSSA= VDDB-VSSB=15V, $V_{OUTA/OUTB}$-VSSA/VSSB =5V (5V miller plateau) f=1kHz		-4		A
Output Peak Sink Current	I_{OUTA_SNK} I_{OUTB_SNK}	6A rev., VDDA-VSSA= VDDB-VSSB=15V, $V_{OUTA/OUTB}$-VSSA/VSSB =5V (5V miller plateau) f=1kHz		6		A
		8A rev., VDDA-VSSA= VDDB-VSSB=15V, $V_{OUTA/OUTB}$-VSSA/VSSB =5V (5V miller plateau) f=1kHz		8		A
Output Source Resistance	R_{OUTA_H} R_{OUTB_H}	$I_{OUTA/OUTB}$=-200mA		1.2	2.4	Ω
Output Sink Resistance	R_{OUTA_L} R_{OUTB_L}	6A rev., $I_{OUTA/OUTB}$=200mA		0.43	0.8	Ω
		8A rev., $I_{OUTA/OUTB}$=200mA		0.35	0.7	Ω

ELECTRICAL CHARACTERISTICS *(continued)*

2.8V ≤ VDDI-GNDI ≤ 5.5V, VDDA-VSSA = VDDB-VSSB = 12V/15V/20V (7), T_J = -40°C to +150°C, typical value is tested at T_J = +25°C, all voltages with respect to the corresponding grounds, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Thermal Shutdown						
Primary Thermal Shutdown Threshold	T_{SD_PRI}	Junction temperature rising		170		°C
Primary Thermal Shutdown Hysteresis	T_{HYS_PRI}			20		°C
Secondary Thermal Shutdown Threshold	T_{SD_SEC}	Junction temperature rising		170		°C
Secondary Thermal Shutdown Hysteresis	T_{HYS_SEC}			20		°C
Switching (Refer to the time sequence diagram for details)						
Output Rise Time ($V_{OUTA/OUTB}$-VSSA/VSSB) rising	t_R	C_{LOAD}=1.8nF		10	20	ns
Output Fall Time ($V_{OUTA/OUTB}$-VSSA/VSSB) falling	t_F	6A rev., C_{LOAD}=1.8nF		10	20	ns
		8A rev., C_{LOAD}=1.8nF		8	18	ns
Minimum Pulse Width	t_{PW_MIN}	Output pulse off if shorter than t_{PW_MIN}, C_{LOAD}=0pF		15	20	ns
Propagation Delay from INA/INB High to OUTA/OUTB Rising Edge	t_{PDLH}	V_{EN}=VDDI or V_{DIS}=GNDI, C_{LOAD}=0pF		50	65	ns
Propagation Delay from INA/INB Low to OUTA/OUTB Falling Edge	t_{PDHL}	V_{EN}=VDDI or V_{DIS}=GNDI, C_{LOAD}=0pF		50	65	ns
Propagation Delay from Enable True to OUTA/OUTB Rising Edge	t_{PDEN}	$V_{INA/INB}$=VDDI, C_{LOAD}=0pF		50	65	ns
Propagation Delay from Disable True to OUTA/OUTB Falling Edge	t_{PDDIS}	$V_{INA/INB}$=VDDI, C_{LOAD}=0pF		50	65	ns
Pulse Width Distortion $\lvert t_{PDLH}-t_{PDHL}\rvert$	t_{PWD}	C_{LOAD}=0pF		1	6	ns
Propagation Delay Matching (Channel-to-Channel)	t_{PDM}	C_{LOAD}=0pF		1	6	ns
Propagation Delay Part-to-Part Skew (9)	t_{PDS}	C_{LOAD}=0pF			10	ns

ELECTRICAL CHARACTERISTICS *(continued)*

2.8V ≤ VDDI-GNDI ≤ 5.5V, VDDA-VSSA = VDDB-VSSB = 12V/15V/20V [7], T_J = -40°C to +150°C, typical value is tested at T_J = +25°C, all voltages with respect to the corresponding grounds, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Switching (Refer to the time sequence diagram for details)						
Startup Delay from Input Supply UVLO Exit to Output Rising Edge	t_{STU_VDDI}	V_{EN}=VDDI or V_{DIS}=GNDI, $V_{INA/INB}$=VDDI, C_{LOAD}=0pF	20	30	40	μs
Shutdown Delay from Input Supply UVLO Entry to Output Falling Edge[10]	t_{SHD_VDDI}	V_{EN}=VDDI or V_{DIS}=GNDI, $V_{INA/INB}$=VDDI, C_{LOAD}=0pF		500		ns
Startup Delay from Output Supply UVLO Exit to Output Rising Edge	t_{STU_VDDA} t_{STU_VDDB}	V_{EN}=VDDI or V_{DIS}=GNDI, $V_{INA/INB}$=VDDI, C_{LOAD}=0pF	10	16	22	μs
Shutdown Delay from Output Supply UVLO Entry to Output Falling Edge[10]	t_{SHD_VDDA} t_{SHD_VDDB}	V_{EN}=VDDI or V_{DIS}=GNDI, $V_{INA/INB}$=VDDI, C_{LOAD}=0pF		500		ns
Static Common-Mode Transient Immunity	$CMTI_{STC}$	V_{EN}=VDDI or V_{DIS}=GNDI, $V_{INA/INB}$=GNDI or VDDI, slew rate of GNDI versus VSSA/VSSB, V_{CM}=1500V	150			kV/μs
Dynamic Common-Mode Transient Immunity	$CMTI_{DYN}$	V_{EN}=VDDI or V_{DIS}=GNDI, f=100kHz pulse at INA/INB, slew rate of GNDI versus VSSA/VSSB, V_{CM}=1500V	150			kV/μs

Notes:

7) For the test condition, VDDA-VSSA=VDDB-VSSB=12V is used for 5V and 8V UVLO devices; VDDA-VSSA=VDDB-VSSB=15V is used for 10V and 12V UVLO devices; VDDA-VSSA=VDDB-VSSB=20V is used for 15V UVLO devices.
8) Guaranteed by characterization, not production tested.
9) Propagation delay part-to-part skew is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
10) Guaranteed by design.

INSULATION & SAFETY-RELATED SPECIFICATIONS

Parameters	Symbol	Condition	SOIC-16/14 WB	SOIC-16 NB	LGA-13 5x5	Units
External Air Gap (Clearance) (11)	CLR	Shortest pin-to-pin distance through air between primary and secondary side	>8	>4	3.5	mm
External Tracking (Creepage) (11)	CPG	Shortest pin-to-pin distance across the package surface between primary and secondary side	>8	>4	3.5	mm
Internal Gap (Internal Clearance)	DTI	Insulation distance through insulation	>25	>12	>12	μm
Tracking Resistance (Comparative Tracking Index)	CTI	IEC60112	>600	>600	>600	V
Isolation Group		Material Group according to IEC 60664-1	I	I	I	
Installation Classification per IEC 60664-1		Rated mains voltages ≤ 150V_{RMS}	I-IV	I-IV	I-IV	
		Rated mains voltages ≤ 300V_{RMS}	I-IV	I-III	I-III	
		Rated mains voltages ≤ 600V_{RMS}	I-IV	I-II	--	
		Rated mains voltages ≤ 1000V_{RMS}	I-III	--	--	
UL 1577, 5th Ed						
Recognized under UL 1577 Component Recognition Program, Single Protection. File number: E322138						
Dielectric Withstand Insulation Voltage	V_{ISO}	V_{TEST}=V_{ISO} for t=60 sec. (qualification), V_{TEST}=1.2 x V_{ISO} for t=1 sec. (100% production)	5000	3000	2500	V_{RMS}
DIN EN IEC 60747-17 (VDE 0884-17): 2021-10						
Certified according to DIN EN IEC 60747-17 (VDE 0884-17): 2021-10; EN IEC 60747-17:2020+AC: 2021. Certification number: pending						
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	AC voltage (bipolar)	2121	990	792	V_{PK}
Maximum Working Isolation Voltage	V_{IOWM}	AC voltage (sine wave), Time Dependent Dielectric Breakdown test method (TDDB)	1500	700	560	V_{RMS}
		DC voltage	2121	990	792	V_{DC}
Maximum Transient Isolation Voltage	V_{IOTM}	V_{TEST}=V_{IOTM} for t=60 sec (qualification); V_{TEST}=1.2 x V_{IOTM} for t=1 sec (100% production)	8000	4242	3535	V_{PK}

INSULATION & SAFETY-RELATED SPECIFICATIONS *(continued)*

Parameters	Symbol	Condition	SOIC-16/14 WB	SOIC-16 NB	LGA-13 5x5	Units
DIN EN IEC 60747-17 (VDE 0884-17): 2021-10 *(continued)*						
Apparent Charge (12) Measuring Voltage	$V_{pd(m)}$	Method b1; at routine test (100% production) and preconditioning (type test). $V_{pd(ini)}$=1.2 x V_{IOTM}, t_{ini}=1 sec; $V_{pd(m)}$=1.5 x V_{IORM} (basic insulation), t_m=1 sec; partial discharge<5 pC	--	1485	1188	V_{PK}
		Method b1; at routine test (100% production) and preconditioning (type test). $V_{pd(ini)}$=1.2 x V_{IOTM}, t_{ini}=1 sec; $V_{pd(m)}$=1.875 x V_{IORM} (reinforced insulation), t_m=1 sec; partial discharge<5 pC	3977	--	--	V_{PK}
Maximum Surge Isolation Voltage (13)	V_{IOSM}	Tested per IEC 62368-1 with 1.2/50µs pulse, V_{TEST}=1.3 x V_{IMP} (basic insulation, qualification)	--	6000	3500	V_{PK}
		Tested per IEC 62368-1 with 1.2/50µs pulse, V_{TEST}=1.3 x V_{IMP}, tested with 10kV (reinforced insulation, qualification)	8000	--	--	V_{PK}
Barrier Capacitance (14)	C_{IO}	f=1MHz	~1	~1	~1	pF
Insulation Resistance (14)	R_{IO}	V_{IO}=500V, T_A=25°C	$>10^{12}$			Ω
		V_{IO}=500V, 100°C≤T_A≤125°C	$>10^{11}$			Ω
		V_{IO}=500V, T_A=T_S=150°C	$>10^{9}$			Ω
Pollution Degree			2			
Climatic Category			40/125/21			

Notes:
11) Refer to package information for detailed dimensions. As isolated solution, the recommended land pattern is helpful to keep enough safety creepage and clearance distances on a printed-circuit board.
12) Electrical discharge caused by a partial discharge in the coupler.
13) Surge test is carried out in oil.
14) The primary side terminals as well as the secondary side terminals of the barrier are connected together forming a two-terminal device. Then C_{IO} and R_{IO} are measured between the two terminals of the coupler.

SAFETY LIMITING VALUES (15)

Parameters	Symbol	Condition	SOIC-16/14 WB	SOIC-16 NB	LGA-13 5x5	Units
Maximum Safety Temperature (16)	T_S		150	150	150	°C
Maximum Output Safety Current (current per channel)	I_{S_O}	VDDA-VSSA=VDDB-VSSB =12V (17), T_J=150°C, T_A=25°C	91	87	48	mA
		VDDA-VSSA=VDDB-VSSB=30V, T_J=150°C, T_A=25°C	36	35	19	mA
Safety Power Dissipation (18)	P_S	Input side	15	15	15	mW
		Output side, channel A	1100	1050	580	mW
		Output side, channel B	1100	1050	580	mW
		Total	2215	2115	1175	mW

Notes:

15) Maximum value allowed in the event of a failure.

16) The maximum safety temperature T_S has the same value as the maximum junction temperature T_J (MAX) specified in ABSOLUTE MAXIMUM RATINGS.

17) Tested for 5V and 8V UVLO devices

18) Test condition: VDDI-GNDI=5.5V, VDDA-VSSA=VDDB-VSSB=30V, T_J=150°C, T_A=25°C.
The safety power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A:
$T_S=T_J(MAX)=T_A+(\theta_{JA} \times P_S)$,
$P_S=I_S \times V_I$, where V_I is the input voltage.

DEFINITIONS OF DYNAMIC PARAMETERS

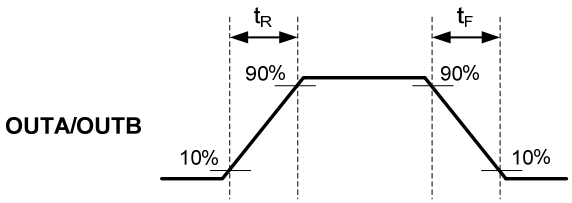


Figure 1: Output Rising and Falling Time

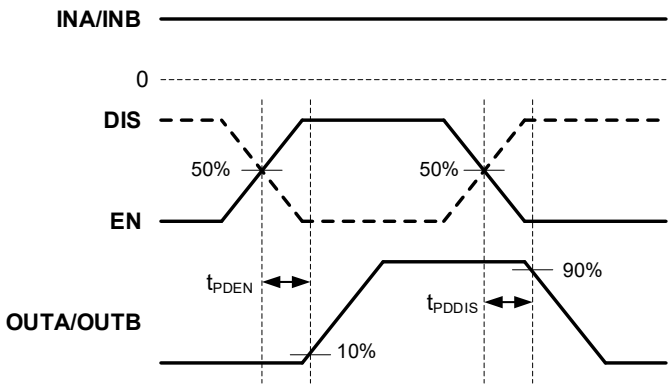


Figure 2: Enable/Disable Response Time

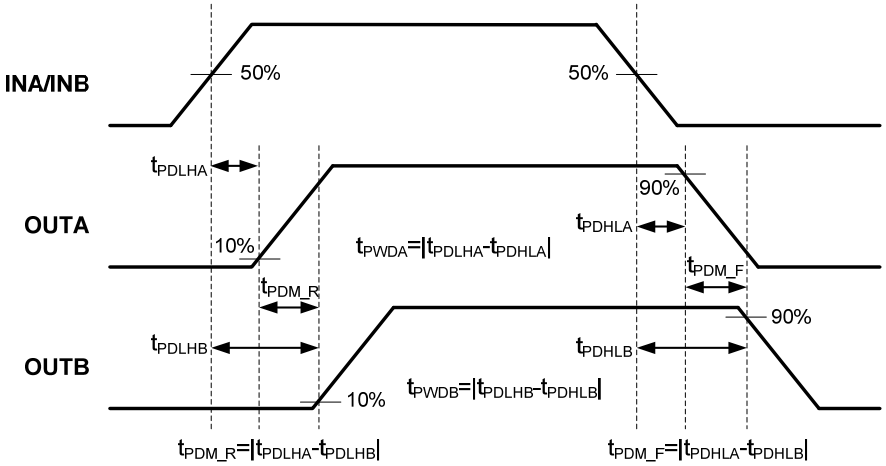


Figure 3: Propagation Delay Matching and Pulse Width Distortion

DEFINITIONS OF DYNAMIC PARAMETERS *(continued)*

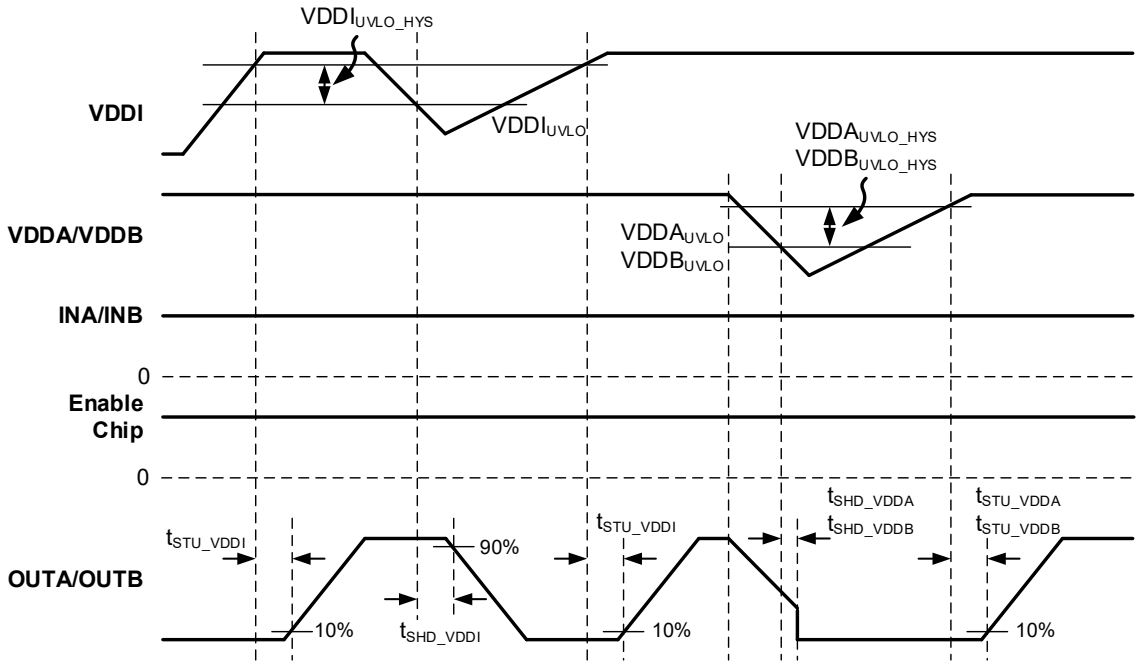


Figure 4: VDDI and VDDA/VDDB Under-Voltage Lockout (UVLO)

DEVICE FUNCTIONAL MODES

Table 1: Logic True Table

Inputs				*Power Supply*			*Outputs*		*Notes*
INA	*INB*	*EN*	*DIS*	*VDDI*	*VDDA*	*VDDB*	*OUTA*	*OUTB*	
L or O	L or O	H or O	L or O	P	P	P	L	L	Output transition occurs immediately.
L or O	H	H or O	L or O	P	P	P	L	H	
H	L or O	H or O	L or O	P	P	P	H	L	
H	H	H or O	L or O	P	P	P	H	H	
X	X	L	H	P	X	X	L	L	Disable chip
X	X	X	X	UP	X	X	L	L	VDDI is unpowered
X	L or O	H or O	L or O	P	UP	P	L	L	VDDA is unpowered
X	H	H or O	L or O	P	UP	P	L	H	
L or O	X	H or O	L or O	P	P	UP	L	L	VDDB is unpowered
H	X	H or O	L or O	P	P	UP	H	L	

Notes:
19) L: Logic Low; H: Logic High; O: Left Open; X: Irrelevant; P: Powered; UP: Unpowered, UVLO condition.
20) If VDDI is powered, the output can operate functionally as long as this channel is powered normally.

BLOCK DIAGRAM

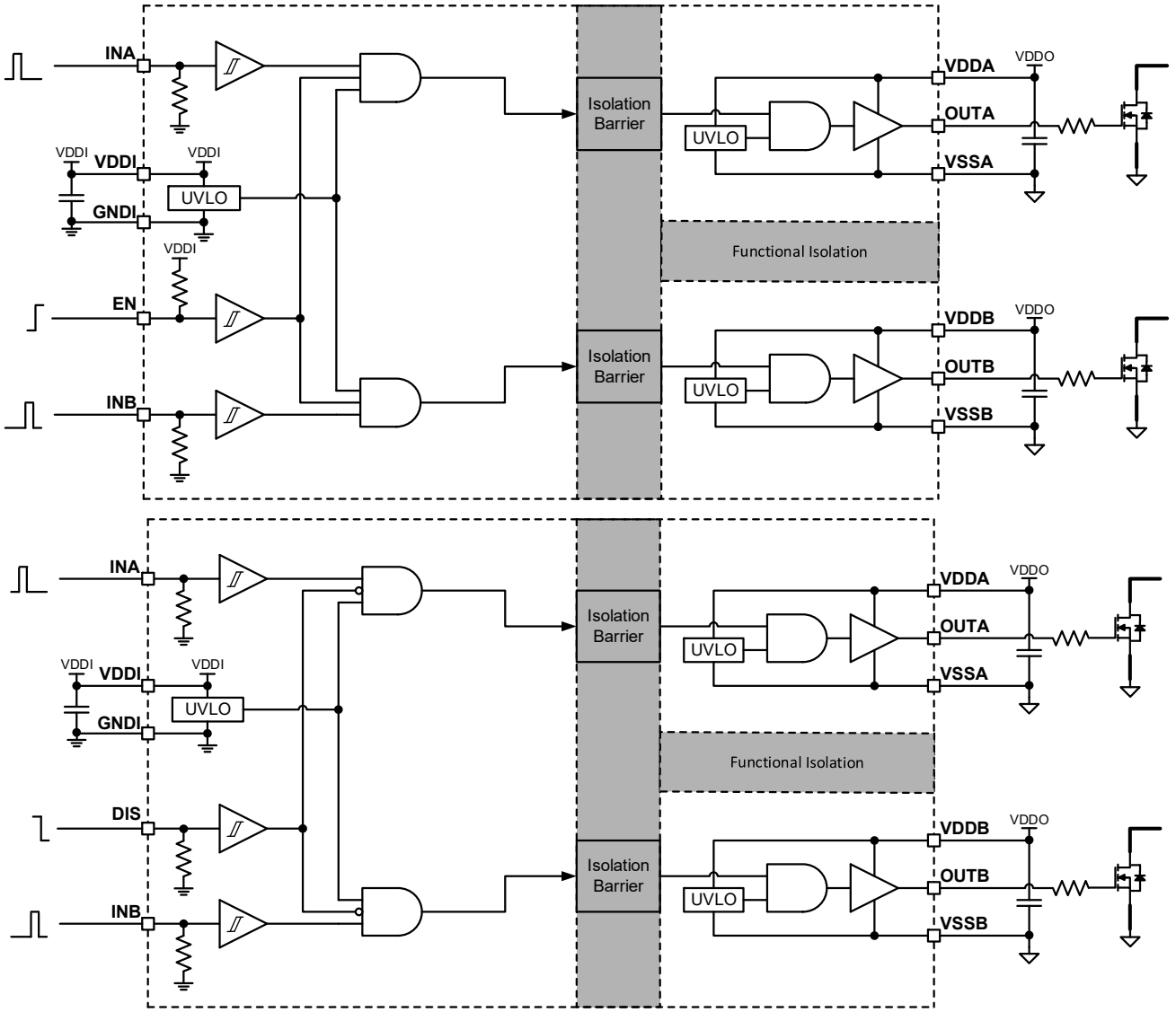


Figure 5: Functional Block Diagram

OPERATION

The MPQ18851 is an isolated dual-input control, independent dual-channel gate driver solution with up to 4A source/8A sink peak output current capacity. This chip is designed to drive power switching devices with short propagation delay and pulse-width distortion. With the advanced features, the MPQ18851 operates high efficiency, high power density, and robustness in a wide variety of automotive power applications.

Please see Table 1 for whole device functional modes.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to avoid the chip or some blocks from operating at insufficient supply voltage. The MPQ18851 incorporates the internal UVLO comparators for all input and output supply circuit blocks to monitor VDDI, VDDA and VDDB, respectively. Figure 4 shows the input and output supply UVLO time sequence diagram.

If the input bias voltage VDDI is unpowered or under supply UVLO level, the chip is not activated and the output stages does not receive the control signals from the input stage. Then the UVLO mechanism holds the output forced low, regardless of the present logic levels of the input signals (including EN/DIS and INA/INB).

When either output stage of the driver is unpowered or below UVLO level, the corresponding channel's output is also pulled low. As long as either channel is powered normally, the corresponding channel can accept the related control signal functionally

Input Stage and On/Off Control

All of the control input pins (EN/DIS and INA/INB) accept a TTL/CMOS compatible logic inputs that is reliably isolated from each output. These control pins are easy to be driven with common logic-level signals from a digital controller. But, any input signal applied to these control pins must never be at a higher level than the input stage supply VDDI. So, it is recommended to tie VDDI to the same power supply of the control signal sources. The control logics of EN/INA/INB are active-high while the control logic of DIS are active-low.

If the INA/INB inputs are left open, they are forced logic low thru the internal pull-down resistors. This configuration ensures the corresponding output keeps low if the control input is not connected. If either logic input pin INA/INB is not being used, it is still recommended to externally ground it for better noise immunity and stable operation.

Similarly, for on/off control, the EN pin is tied to VDDI thru the internal pull-up resistor while the DIS pin is connected to GNDI thru the internal pull-down resistor. Although leaving EN/DIS pin floating enables the chip to operate normally after start-up, it is still recommended to provide stable external signal input for on/off control in actual applications.

Output Stage

The output stage comprises an upper P-channel MOSFET and a lower N-channel MOSFET (refer to Figure 6). The effective output pull-up source resistance R_{OUTA_H}/R_{OUTB_H} is the on-resistance of the upper P-channel MOSFET, which delivers the large peak source current during the external power-switch turn-on transition. The pull-down structure is simply an N-channel MOSFET, whose on-resistance R_{OUTA_L}/R_{OUTB_L} is the output effective pull-down impedance during the drive-low state of the device.

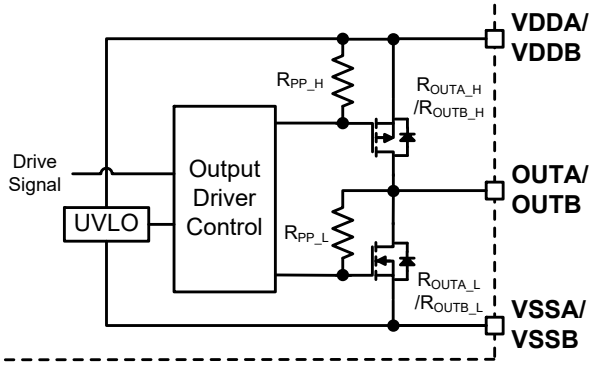


Figure 6: Output Stage

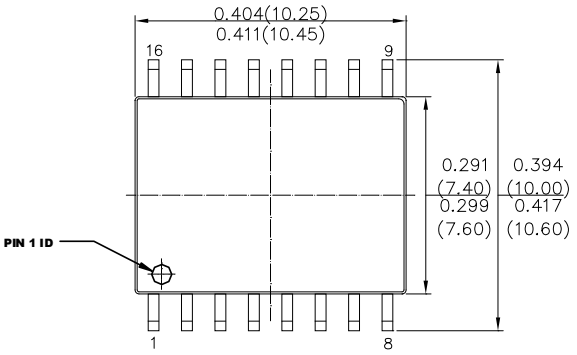
The output stage is optimized to provide strong driving capacity to a power device during the miller plateau interval of the switching on/off procedure. So the MPQ18851 is capable of delivering 4A/8A peak source/sink current pulses. And the rail-to-rail output ensures the voltage swings between VDDA/VDDB and VSSA/VSSB, respectively.

Thermal Shutdown

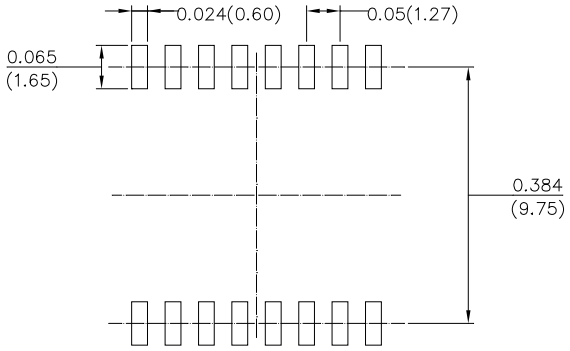
Thermal shutdown is implemented to prevent the chip from operating at exceeding high temperature. When the silicon die temperature is higher than 170°C, the OTP shuts down the whole chip until the junction temperature drops below its lower threshold, then the chip restarts again. Both of the primary- and secondary-side features thermal shutdown independently.

PACKAGE INFORMATION

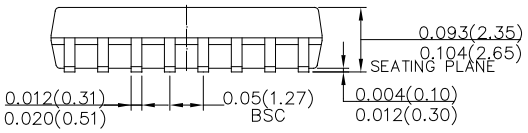
SOIC-16 WB (HV ISOLATION)



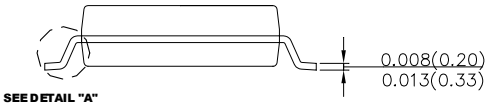
TOP VIEW



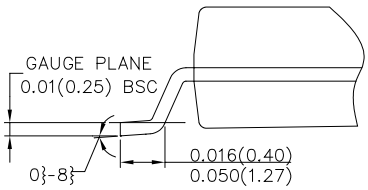
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



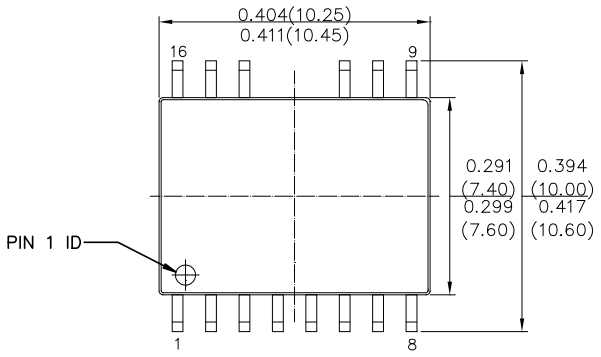
DETAIL "A"

NOTE:

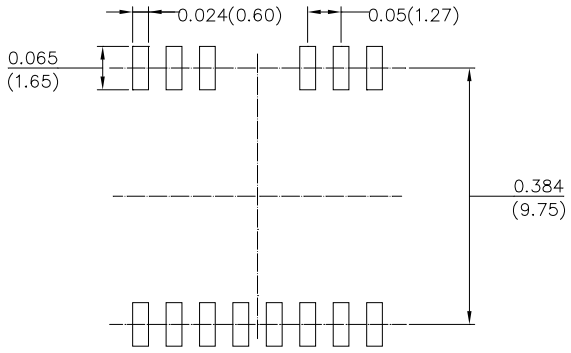
1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-013, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

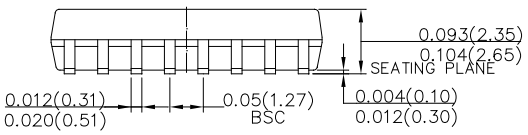
SOIC16-14 WB (HV ISOLATION)



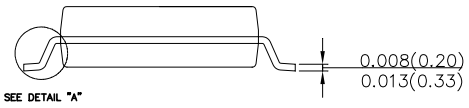
TOP VIEW



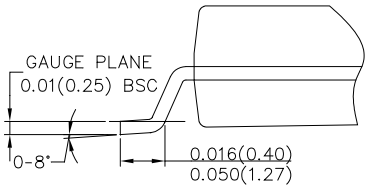
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

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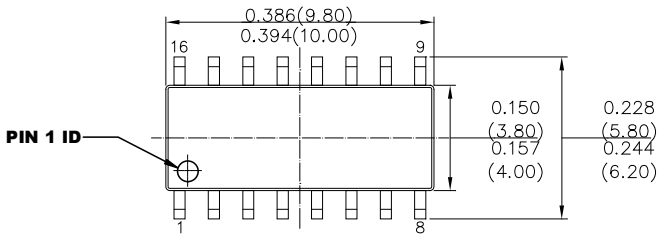
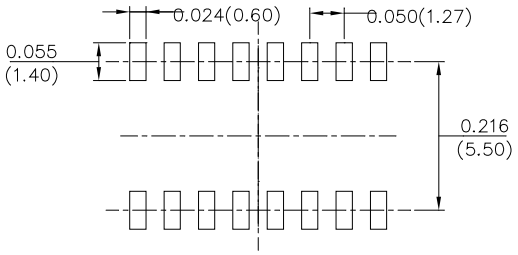
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING REFERENCE TO JEDEC MS-013, VARIATION AD.
6) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

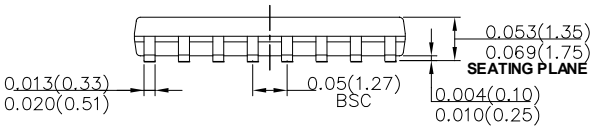
SOIC-16 NB (HV ISOLATION)



TOP VIEW



RECOMMENDED LAND PATTERN



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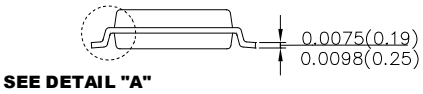

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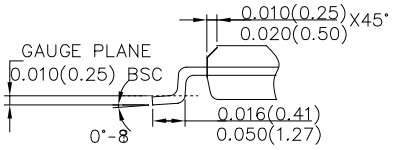

DETAIL "A"

NOTE:

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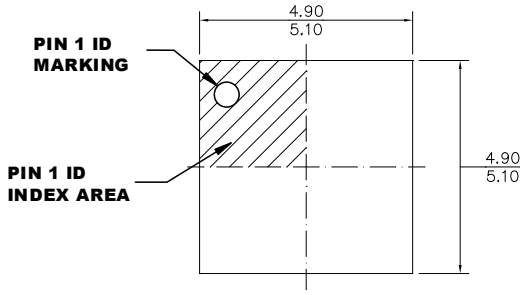
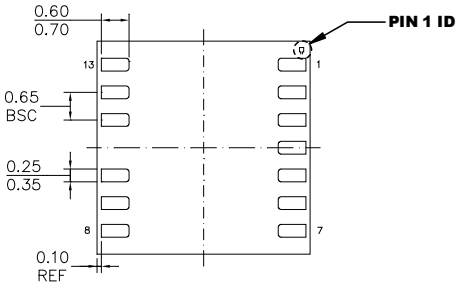
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BC.
6) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

LGA-13 (5mmx5mm)

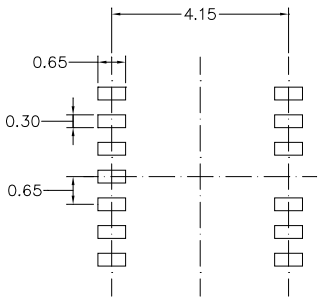


TOP VIEW



BOTTOM VIEW

SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.