MPQ4276A

36V, 6A, Configurable Frequency Buck Converter with Dual USB Charging Ports and PFM Mode under Light Loads, AEC-Q100

DESCRIPTION

The MPQ4276A integrates a monolithic, step-down switch-mode converter with two USB current-limit switches, as well as USB Type-C 5V @ 3A mode configuration channels for each port. The MPQ4276A achieves 6A of output current (I_{OUT}) across a wide input supply range, with excellent load and line regulation.

The USB switch's output is current-limited. Both USB ports support USB Type-C 5V @ 3A DFP mode, which eliminates the need for external user interaction.

The MPQ4276A uses peak current control mode to regulate the output voltage (V_{OUT}). Under light-load conditions, the device enters pulse-frequency modulation (PFM) mode to improve light-load efficiency.

Full protection features include hiccup current limiting, output over-voltage protection (OVP), and thermal shutdown.

The MPQ4276A requires a minimal number of readily available, standard external components, and is available in a QFN-26 (5mmx5mm) package.

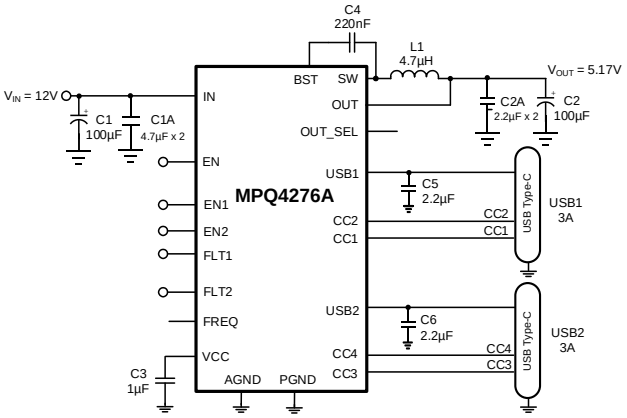
FEATURES

- Passes USB-IF Type-C Certification Test
- Passes Apple MFI Certification Test
- Automatic Pulse-Frequency Modulation (PFM) and Pulse-Width Modulation (PWM) Modes
- Enables Output when EN is Pulled High or CC1, CC2, CC3, and CC4 Are Connected
- EN1 and EN2 Pulled Active Low Controls USB1 and USB2 On/Off
- 135°C Load-Shedding vs. Temperature
- Accurate 5A USB1 and USB2 Output Current (I_{OUT}) Limit
- Wide 6V to 36V Operating Input Voltage (V_{IN}) Range
- Selectable Output Voltage (V_{OUT})
- Line Drop Compensation
- 21mΩ and 15mΩ Low On Resistance ($R_{DS(ON)}$) Internal Power MOSFETs for the Buck Converter
- 18mΩ and 18mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs for USB1 and USB2
- Adjustable 200kHz to 2.2MHz Frequency
- Hiccup Current Limit for Both the Buck Converter and USB Switches
- Fault Indication for USB1 and USB2
- Supports USB Type-C 5V @ 3A Mode
- ±8kV Human Body Model (HBM) ESD Rating for USB1 and USB2
- Available in a QFN-26 (5mmx5mm) Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

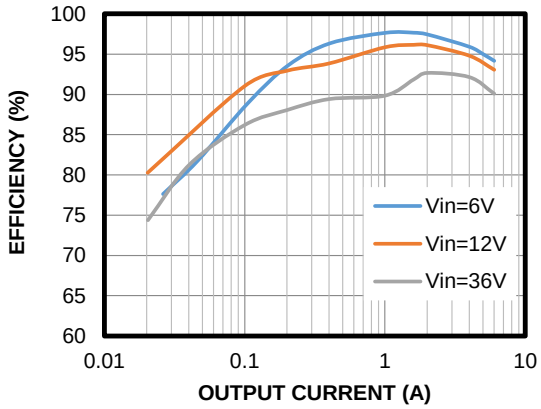
- USB Hubs
- USB Type-C Charging Ports

TYPICAL APPLICATION



Efficiency vs. Load Current

V_{OUT} = 5.17V, f_{SW} = 450kHz, L = 4.7µH, DCR = 7mΩ



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ4276AGU-AEC1	QFN-26 (5mmx5mm)	*See Below*	1

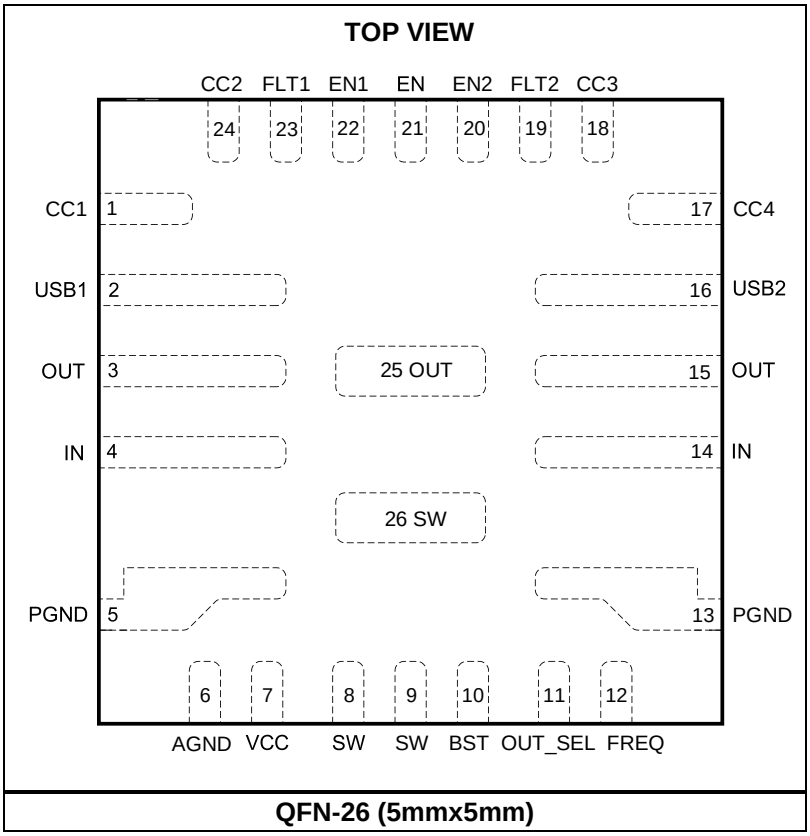
* For Tape & Reel, add suffix -Z (e.g. MPQ4276AGU-AEC1-Z).

TOP MARKING

MPSYYWW
MP4276A
LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP4276A: Part number
LLLLLLL: Lot number

PACKAGE REFERENCE



QFN-26 (5mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
1	CC1	**Configuration channel 1.** The CC1 pin detects connections and configures the interface across the USB1 Type-C cables and connectors. Once a connection is established, CC1 or CC2 is reassigned to provide power to the plug's VCONN pin.
2	USB1	**USB1 output.**
3, 15, 25	OUT	**Buck output.** The OUT pin is the power input for USB1 and USB2.
4, 14	IN	**Supply voltage.** The IN pin is the internal power device's drain, and provides power to the entire chip. The MPQ4276A operates from a 6V to 36V input voltage (V_{IN}) range. Place an input capacitor (C_{IN}) as close to the IC as possible to prevent large voltage spikes at the input.
5, 13	PGND	**Power ground.** The PGND pin is the regulated output voltage (V_{OUT})'s reference ground, and requires additional consideration during PCB layout. Connect PGND to the PCB using copper traces and vias.
6	AGND	**Analog ground.** Connect the AGND pin to PGND.
7	VCC	**Internal 4.5V low-dropout (LDO) regulator output.** Decouple the VCC pin using a 1µF capacitor.
8, 9, 26	SW	**Switch output.** Connect the SW pin using a wide PCB trace.
10	BST	**Bootstrap (BST).** Connect a 0.22µF capacitor between SW and BST to form a floating supply across the high-side MOSFET (HS-FET) driver.
11	OUT_SEL	**Buck converter V_{OUT} setting.** If the OUT_SEL pin is pulled low, then V_{OUT} is 5.1V. If OUT_SEL is pulled high, then V_{OUT} is 5.3V. If OUT_SEL is floating, then V_{OUT} is 5.17V.
12	FREQ	**Switching frequency configurable input.** Connect a resistor from the FREQ pin to GND to set the switching frequency (f_{SW}). Float FREQ or connect the pin to VCC for a default 450kHz f_{SW}. Connect FREQ to ground for an internal 235kHz f_{SW}.
16	USB2	**USB2 output.**
17	CC4	**Configuration channel 4.** The CC4 pin detects connections and configures the interface across the USB2 Type-C cables and connectors. Once a connection is established, CC3 or CC4 is reassigned to provide power to the plug's VCONN pin.
18	CC3	**Configuration channel 3.** The CC3 pin detects connections and configures the interface across the USB2 Type-C cables and connectors. Once a connection is established, CC3 or CC4 is reassigned to provide power to the plug's VCONN pin.
19	FLT2	**USB2 fault indication.** The FLT2 pin indicates over-current (OC) or over-temperature (OT) conditions. FLT2 is an open drain under normal conditions. If a fault occurs, then FLT2 is pulled low.
20	EN2	**USB2 on/off control input.** EN2 is an active low pin and has an internal 1MΩ pull-down resistor by default. EN2 also controls when the USB1 Type-C detection circuitry is on or off. When EN2 is high, the USB2 detection circuit is disabled.
21	EN	**On/off control of the buck converter's output.** The EN pin controls when the buck converter's output is on or off. The Type-C connection logic also can enable the converter's output, even if EN is low.
22	EN1	**USB1 on/off control input.** EN1 is an active low pin and has an internal 1MΩ pull-down resistor by default. EN1 also controls when the USB1 Type-C detection circuitry is on or off. When EN1 is high, the USB1 detection circuit is disabled.
23	FLT1	**USB1 fault indication.** The FLT1 pin indicates OC or OT conditions. FLT1 is an open drain under normal conditions. If a fault occurs, then FLT1 is pulled low.
24	CC2	**Configuration channel 2.** The CC2 pin detects connections and configures the interface across the USB1 Type-C cables and connectors. Once a connection is established, CC1 or CC2 is reassigned to provide power to the plug's VCONN pin.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) ..... -0.4V to +40V
V_{SW} .....-0.3V (-5V for <10ns)
……...to V_{IN} + 0.3V (+43V for <10ns)
V_{BST} .....V_{SW} + 5.5V
V_{EN}……-0.3V to +10V (2)
V_{OUT}, V_{USB} ..... -0.3V to +6.5V
All other pins..... -0.3V to +5.5V
Continuous power dissipation (T_A = 25°C) (3) (7)
QFN-26 (5mmx5mm).....6.25W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature..... -65°C to +150°C

ESD Ratings (4)

Human body model (HBM)
USB1 and USB2 (5).....±8kV
CC1/CC2/CC3/CC4 (5)…….....±7kV
All other pins…….....±2kV
Charged device model (CDM)
All pins…….....±2kV

Recommended Operating Conditions (6)

Operating input voltage (V_{IN}) range.....6V to 36V
Output current (I_{OUT})……
……..3A for USB1, 3A for USB2
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-26 (5mmx5mm)			
EVQ4276A-U-00A (7)	20	2	°C/W
JESD51-7 (8)	44	9	°C/W

Notes:

1) The absolute maximum ratings are rated under room temperature, unless otherwise noted. Exceeding these ratings may damage the device.
2) For details on the EN pin's absolute maximum rating, see the Enable (EN) Control section on page 14.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101, AEC specification AECQ100-011. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
5) HBM with regard to GND.
6) The device is not guaranteed to function outside of its operating conditions. Operating devices at a junction temperature exceeding 125°C is possible. Contact MPS for details.
7) Measured on the EVQ4276A-U-00A, a 4-layer PCB (50mmx50mm).
8) Measured on JESD51-7, a 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, CC1 connected to ground via a 5.1kΩ resistor, CC3 connected to ground via a 5.1kΩ resistor, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown supply current	I_{IN1}	V_{EN} = 0V, V_{EN1} = V_{EN2} = high		150		μA
	I_{IN2}	V_{EN} = V_{EN1} = V_{EN2} = 0V		180		μA
Quiescent supply current	I_{Q1}	V_{EN} = high or low, Type-C connected, V_{OUT} = 5.4V, no switching for buck converter		0.8		mA
	I_{Q2}	V_{EN} = high, USB Type-C disconnected, V_{OUT} = 5.4V, no switching for buck converter, T_J = 25°C		300		μA
EN rising threshold	V_{EN_R}		-3%	1.235	+3%	V
EN hysteresis	V_{EN_HYS}			230		mV
Thermal shutdown (9)	T_{TSD}			165		°C
Thermal hysteresis (9)	T_{TSD_HYS}			20		°C
VCC regulator	V_{CC}		4.2	4.5	4.9	V
VCC load regulation	V_{CC_LOG}	I_{CC} = 50mA		1	3	%
Step-Down Converter						
Input volage (V_{IN}) under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_R}$		4.6	5	5.4	V
V_{IN} UVLO hysteresis	$V_{IN\_UVLO\_HYS}$			650		mV
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$			21	35	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$			15	30	mΩ
Output voltage	V_{OUT}	OUT_SEL = low	-2%	5.1	+2%	V
		OUT_SEL = float, T_J = 25°C	-1%	5.17	+1%	
		OUT_SEL = float, T_J = -40°C to +125°C	-2%	5.17	+2%	
		OUT_SEL = high	-2%	5.3	+2%	
Output over-voltage protection (OVP)	V_{OVP_R}		5.45	5.85	6.25	V
Output OVP recovery	V_{OVP_F}		5.3	5.7	6.1	V
Output-to-ground resistance	R_{FB}	EN = 0V, T_J = 25°C	120	175	230	kΩ
Low-side (LS) current limit	I_{LS_LIMIT}			-2		A

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, CC1 connected to ground via a 5.1kΩ resistor, CC3 connected to ground via a 5.1kΩ resistor, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 36V, T_J = 25°C			1	μA
		V_{EN} = 0V, V_{SW} = 36V, T_J = -40°C to +125°C			5	
High-side (HS) current limit	I_{LIMIT}	V_{OUT} = 0V	9	13	17	A
Switching frequency	f_{SW1}	Pull R_{FREQ} to GND	170	235	300	kHz
	f_{SW2}	R_{FREQ} = 66.5kΩ	250	350	450	
	f_{SW3}	R_{FREQ} = 9.53kΩ	1800	2200	2600	
	f_{SW4}	R_{FREQ} = float	350	450	530	
Maximum duty cycle	D_{MAX}	FREQ = 450kHz	91	95	99	%
Minimum off time	t_{OFF_MIN}			110		ns
Minimum on time (9)	t_{ON_MIN}			130		ns
Soft-start time	t_{SS}	Output from 10% to 90%	1	2	3.4	ms
USB Switch (USB1 and USB2)						
UVLO rising threshold	$V_{USB\_UVLO\_R}$		3.7	4	4.3	V
UVLO hysteresis	$V_{USB\_UVLO\_HYS}$			220		mV
Switch on resistance	$R_{DS(ON)\_SW}$			18	30	mΩ
Output-to-ground resistance	R_{DIS_USB}	Apply 5V on the USB output, float CCx	250	500	750	kΩ
USB OVP clamp	V_{USB_OVP}		5.3	5.6	5.9	V
Current limit	I_{LIMIT}	V_{OUT} drops by 10%, USB Type-C mode, T_J = 25°C	-6%	5	+6%	A
Line drop compensation	V_{DROP_COM}	At 2.4A load, V_{OUT} = 5.17V	20	70	120	mV
Bus voltage (V_{BUS}) soft-start time	t_{SS}	Output from 10% to 90%	1	2	3	ms
Hiccup mode on time	t_{HICP_ON2}	Over-current (OC) condition, V_{OUT} drops by 10%, T_J = 25°C	3.5	5	6.5	ms
		OC condition, V_{OUT} drops by 10%, T_J = -40°C to +125°C	3	5	7	
Hiccup mode off time	t_{HICP_OFF}	VOUT connected to GND	1	2	3	s
EN1 and EN2 logic high input	$V_{EN\text{-}SW\_H}$	Disable USBx	0.95	1	1.05	V
EN1 and EN2 logic low input	$V_{EN\text{-}SW\_L}$	Enable USBx	0.85	0.9	0.95	V
EN1 and EN2 pull-down resistor	R_{EN1}			1		MΩ
	R_{EN2}					
FLT1 and FLT2 output low voltage	V_{FLT_LOW}	Fault condition, sink 1mA			150	mV
FLT1 and FLT2 leakage	I_{FLT_LKG}	V_{FAULT} = 5V			1	μA
FLT1 and FLT2 deglitch time	t_{FLT_DEG}	OC condition	3	5	7	ms

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, CC1 connected to ground via a 5.1kΩ resistor, CC3 connected to ground via a 5.1kΩ resistor, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
USB Type-C 5V @ 3A Mode (CC1, CC2, CC3, and CC4)						
CCx voltage to enable the VCONN voltage (V_{CONN})	V_{RA}				0.75	V
CCx voltage to enable V_{BUS}	V_{RD}		0.9		2.45	V
CCx detach threshold	V_{OPEN}		2.75			V
CCx voltage falling debounce timer	$t_{CC\_DEBOUNCE}$	V_{BUS} enable deglitch time	100	144	200	ms
CCx voltage rising debounce timer	$t_{PD\_DEBOUNCE}$	V_{BUS} disable deglitch time	10	15	20	ms
V_{CONN} output power	P_{VCONN}	V_{CONN} comes from the buck output with some series resistance, T_J = 25°C	1			W

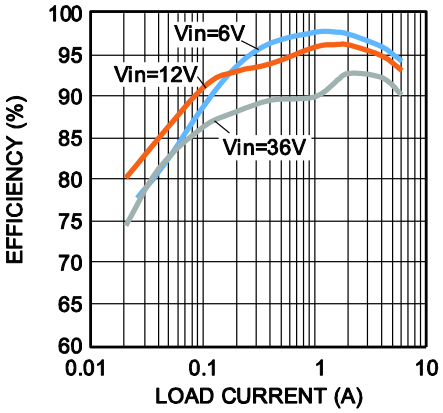
Note:

9) Guaranteed by engineering sample characterization.

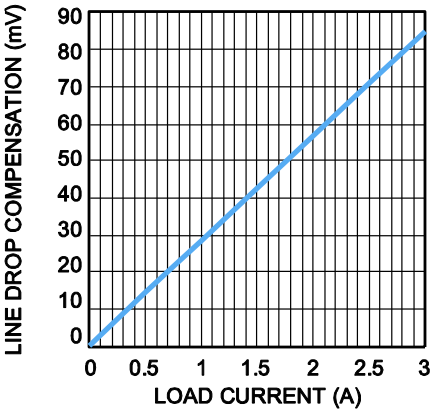
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5.17V, f_{SW} = 450kHz, L = 4.7µH, T_A = 25°C, CC1 connected to ground via a 5.1kΩ resistor, CC3 connected to ground via a 5.1kΩ resistor, unless otherwise noted.

Efficiency vs. Load Current

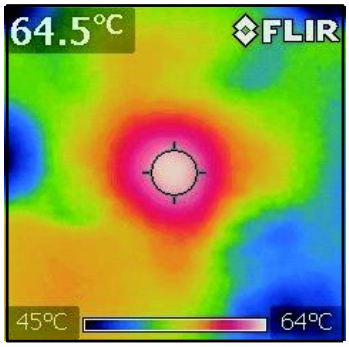


Line Drop Compensation vs. Load Current



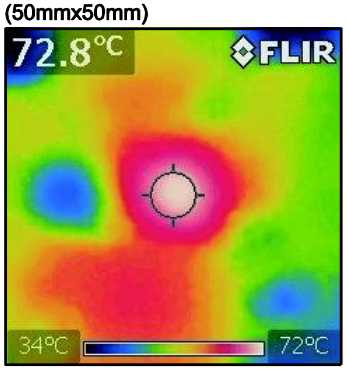
Thermal Image

V_{IN} = 12V, USB1 I_{OUT} = USB2 I_{OUT} = 2.4A, 4-layer PCB (50mmx50mm)



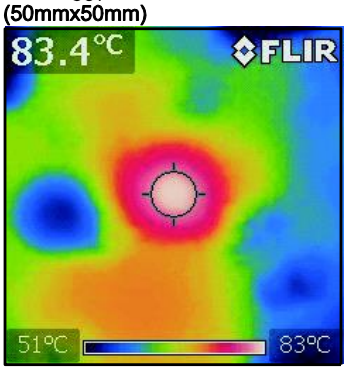
Thermal Image

V_{IN} = 12V, USB1 I_{OUT} = 2.4A, USB2 I_{OUT} = 3A, 4-layer PCB (50mmx50mm)



Thermal Image

V_{IN} = 12V, USB1 I_{OUT} = 3A, USB2 I_{OUT} = 3A, 4-layer PCB (50mmx50mm)

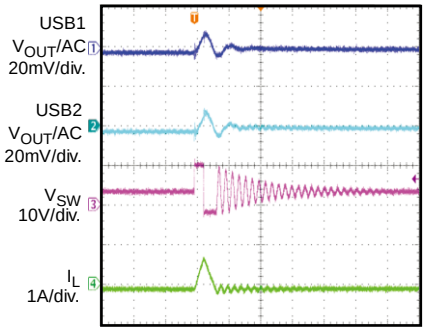


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5.17V, f_{SW} = 450kHz, L = 4.7µH, T_A = 25°C, CC1 connected to ground via a 5.1kΩ resistor, CC3 connected to ground via a 5.1kΩ resistor, unless otherwise noted.

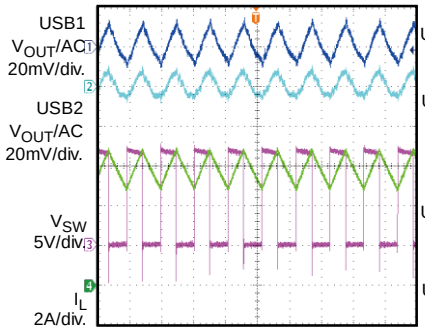
Output Ripple

V_{IN} = 12V, V_{OUT} = 5.17V,
USB1 I_{OUT} = USB2 I_{OUT} = 0A



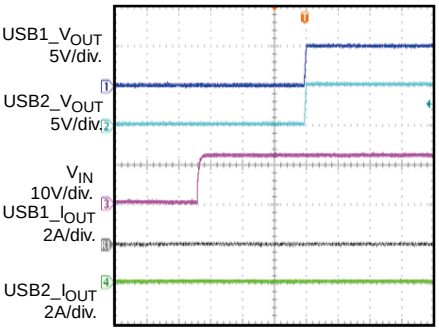
Output Ripple

V_{IN} = 12V, V_{OUT} = 5.17V,
USB1 I_{OUT} = USB2 I_{OUT} = 3A



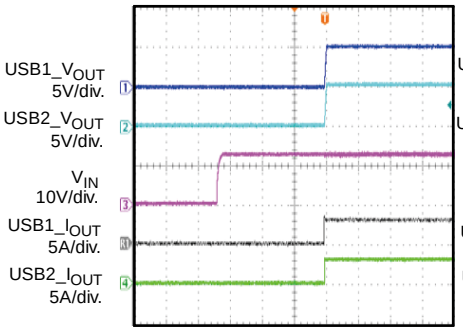
Start-Up

V_{IN} = 12V, V_{OUT} = 5.17V,
USB1 I_{OUT} = USB2 I_{OUT} = 0A



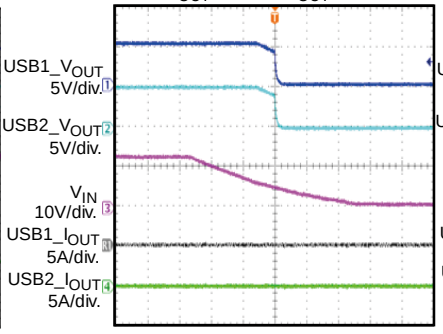
Start-Up

V_{IN} = 12V, V_{OUT} = 5.17V,
USB1 I_{OUT} = USB2 I_{OUT} = 3A



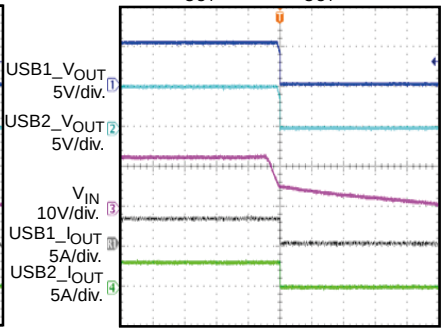
Shutdown

V_{IN} = 12V, V_{OUT} = 5.17V,
USB1 I_{OUT} = USB2 I_{OUT} = 0A

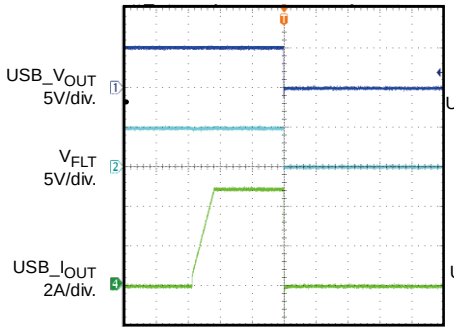


Shutdown

V_{IN} = 12V, V_{OUT} = 5.17V,
USB1 I_{OUT} = USB2 I_{OUT} = 3A

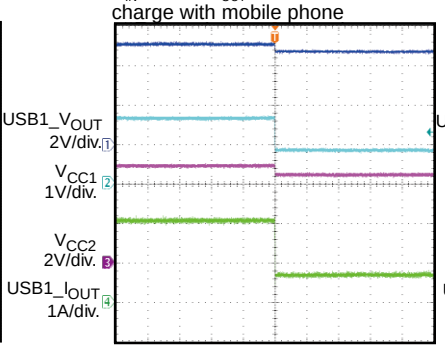


USB Over-Current Protection



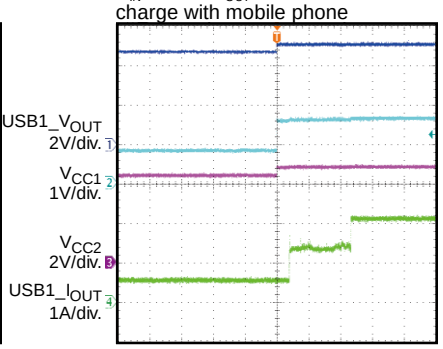
Load-Shedding Entry

V_{IN} = 12V, V_{OUT} = 5.17V,
charge with mobile phone



Load-Shedding Recovery

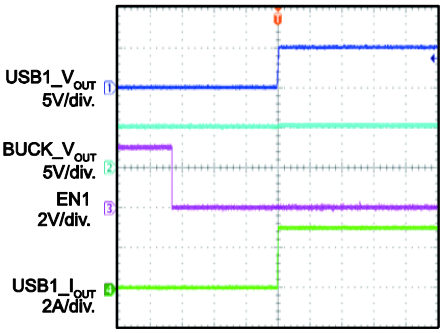
V_{IN} = 12V, V_{OUT} = 5.17V,
charge with mobile phone



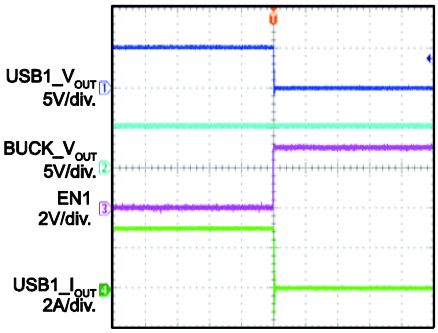
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5.17V, f_{SW} = 450kHz, L = 4.7µH, T_A = 25°C, CC1 connected to ground with a 5.1kΩ resistor, CC3 connected to ground via a 5.1kΩ resistor, unless otherwise noted.

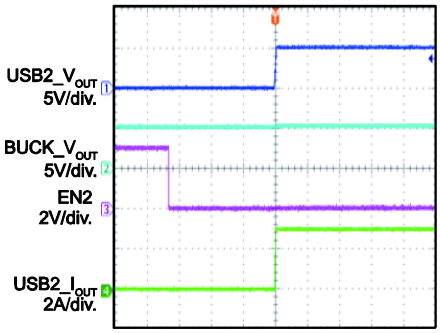
Start-Up through EN1
EN = high, USB1 connected, USB2 disconnected, USB1 I_{OUT} = 3A;
CH2 label, BUCK_V_{OUT}



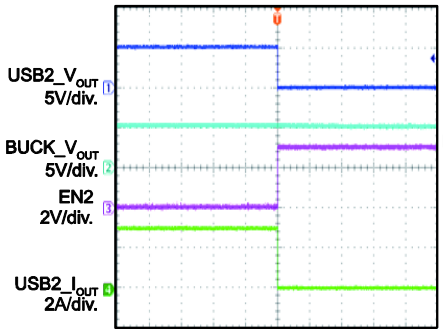
Shutdown through EN1
EN = high, USB1 connected, USB2 disconnected, USB1 I_{OUT} = 3A;
CH2 label, BUCK_V_{OUT}



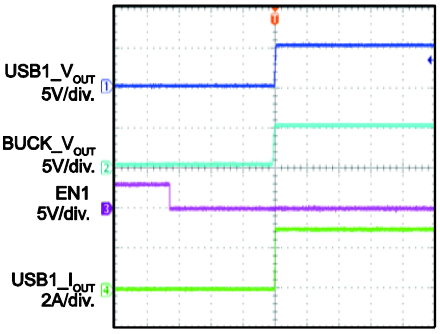
Start-Up through EN2
EN = high, USB1 disconnected, USB2 connected, USB2 I_{OUT} = 3A ;
CH2 label, BUCK_V_{OUT}



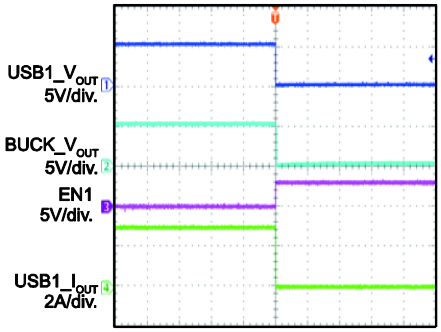
Shutdown through EN2
EN = high, USB1 disconnected, USB2 connected, USB2 I_{OUT} = 3A ;
CH2 label, BUCK_V_{OUT}



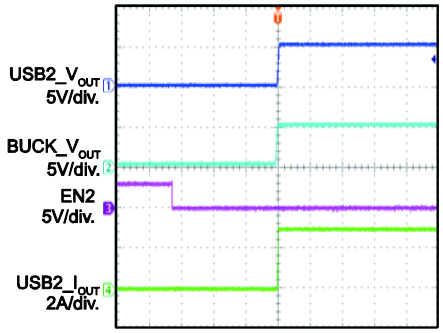
Start-Up through EN1
EN = low, USB1 connected, USB2 disconnected, USB1 I_{OUT} = 3A ;
CH2 label, BUCK_V_{OUT}



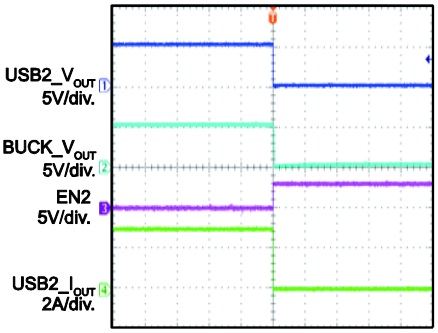
Shutdown through EN1
EN = low, USB1 connected, USB2 disconnected, USB1 I_{OUT} = 3A ;
CH2 label, BUCK_V_{OUT}



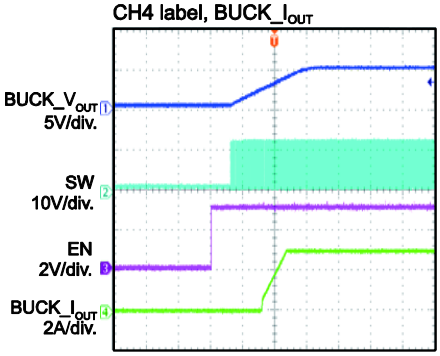
Start-Up through EN1
EN = low, USB1 disconnected, USB2 connected, USB2 I_{OUT} = 3A ;
CH2 label, BUCK_V_{OUT}



Shutdown through EN2
EN = low, USB1 disconnected, USB2 connected, USB2 I_{OUT} = 3A ;
CH2 label, BUCK_V_{OUT}



Start-Up through EN
USB1 disconnected, USB2 disconnected, buck I_{OUT} = 3A ;
CH1 label, BUCK_V_{OUT} ;
CH4 label, BUCK_I_{OUT}

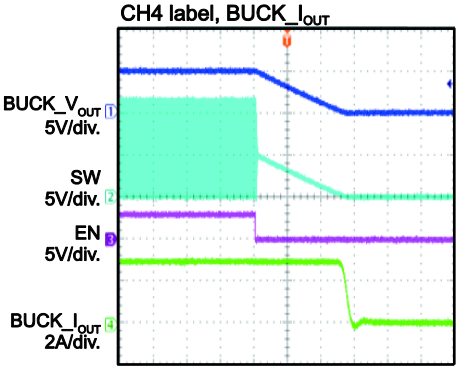


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5.17V, f_{SW} = 450kHz, L = 4.7µH, T_A = 25°C, CC1 connected to ground via a 5.1kΩ resistor, CC3 connected to ground via a 5.1kΩ resistor, unless otherwise noted.

Shutdown through EN

USB1 disconnected, USB2 disconnected, buck I_{OUT} = 3A ;
CH1 label, BUCK_V_{OUT} ;
CH4 label, BUCK_I_{OUT}



FUNCTIONAL BLOCK DIAGRAM

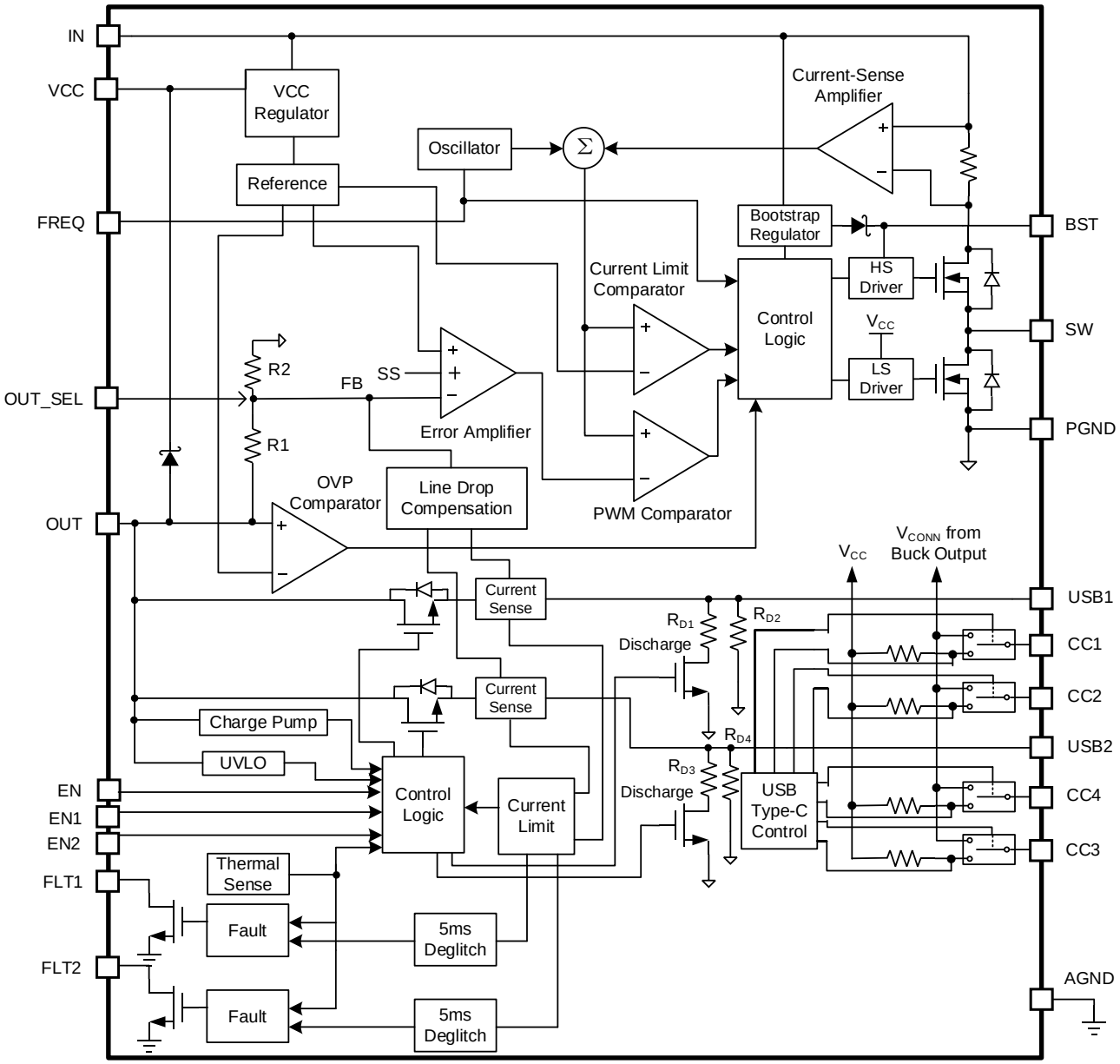


Figure 1: Functional Block Diagram

OPERATION

Buck Converter

The MPQ4276A integrates a monolithic, synchronous, rectified, step-down switch-mode converter with internal power MOSFETs, as well as two USB current-limit switches with charging port auto-detection. The MPQ4276A offers a compact solution to achieve 6A of continuous output current (I_{OUT}) across a wide input supply range, with excellent load and line regulation.

The MPQ4276A operates in fixed-frequency, peak current control mode to regulate the output voltage (V_{OUT}). The internal clock initiates the pulse-width modulation (PWM) cycle, which turns on the integrated high-side power MOSFET (HS-FET). The HS-FET remains on until its current reaches the value set by the COMP voltage (V_{COMP}). When the power MOSFET is off, it remains off until the next clock cycle begins. If the duty cycle reaches 95% (when switching frequency, f_{SW}, is 450kHz) within one PWM period, then the power MOSFET turns off even if its current does not reach the value set by COMP. To improve efficiency, the device enters pulse-frequency modulation (PFM) mode under light loads.

Error Amplifier (EA)

The error amplifier (EA) compares the internal feedback (FB) voltage (V_{FB}) to the internal reference voltage (V_{REF}) and outputs V_{COMP}, which controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies control loop design.

Internal VCC Regulator

The 4.5V internal regulator powers most of the internal circuitries. This regulator uses the input voltage (V_{IN}) and operates across the full V_{IN} range. If V_{IN} exceeds 4.5V, then the regulator's output is in full regulation. If V_{IN} drops below 4.5V, then the output falls with V_{IN}. VCC requires an external 1µF ceramic decoupling capacitor.

After the MPQ4276A's buck converter output starts up, the internal VCC low-dropout (LDO) output is biased by the buck converter output via a Schottky diode.

VCC begins to work when V_{IN} ramps up, even if EN is low.

Enable (EN) Control

The MPQ4276A has an enable (EN) control pin. Pull EN high to enable the buck converter's output; pull EN low or float the pin to disable the output. Once EN is pulled high, the buck converter output is enabled regardless of the statuses of EN1, EN2, CC1, CC2, CC3, and CC4. When EN is pulled low, the buck converter output can also be enabled by connecting USB1 or USB2. Table 2 on page 19 shows the device's output control logic.

EN is clamped internally using a 7.6V series Zener diode. The ESD cell has a 10V breakdown voltage (see Figure 2).

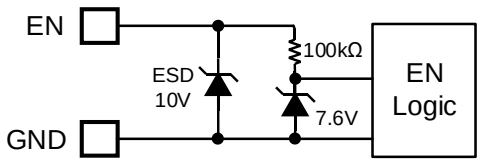


Figure 2: 7.6V Series Zener Diode between EN and GND

It is recommended to connect EN to VIN and GND via resistor dividers to enhance EN's pull-up current ability. If the EN pull-up voltage exceeds 10V, then EN must be limited to below 10V, and the EN current must be below 100µA.

For example, if the EN pull-up resistor is 100kΩ and the pull-down resistor is 34.8kΩ, then the MPQ4276A starts up once V_{IN} exceeds its under-voltage lockout (UVLO) rising threshold. If any of the following conditions are met, the converter shuts down:

- V_{IN} drops below the UVLO falling threshold
- EN goes low when CC1, CC2, CC3, and CC4 are disconnected

Setting the Switching Frequency (f_{SW})

Connect a resistor from FREQ to ground to set f_{SW} (see Table 1 on page 15). f_{SW} can be calculated using Equation (1):

$$f_{SW}\ (kHz) = \frac{1000000}{42.5 \times R_{FREQ}\ (k\Omega) + 53.7} \quad (1)$$

Figure 3 shows the relationship between f_{SW} and the frequency-configurable resistor (R_{FREQ}).

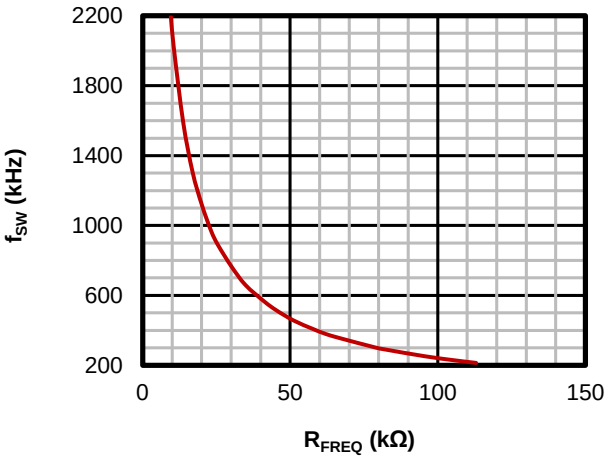


Figure 3: f_{SW} vs. R_{FREQ}

Table 1 shows the recommended resistance for typical switching frequencies.

Table 1: Recommended Resistance for Typical Switching Frequencies

R_{FREQ} (kΩ)	f_{SW} (kHz)
0	235
66.5	350
NS	450
45.8	500
22.3	1000
14.6	1500
9.53	2200

When the device operates at a high f_{SW} (about 2.2MHz), consider the minimum on time, minimum off time, and the temperature rise.

Two internal comparators monitor FREQ's logic voltage. These comparators can float FREQ or short the pin to GND.

During start-up, there is another internal source current on FREQ. f_{SW} is clamped at 450kHz when a voltage exceeding 2V is sensed on FREQ for longer than 8μs. f_{SW} is clamped at 235kHz when a voltage below 0.1V is sensed on FREQ for longer than 8μs. Float FREQ or connect the pin to VCC to achieve the default 450kHz f_{SW}. Short FREQ to ground to achieve a 235kHz f_{SW} (see Figure 4).

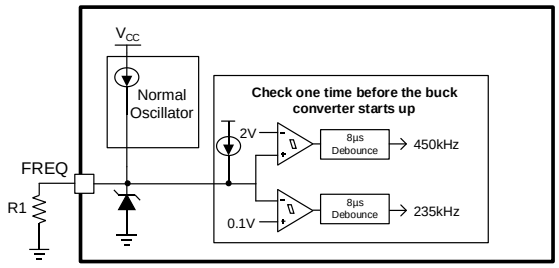


Figure 4: Switching Frequency Functional Block

Light-Load Operation

The MPQ4276A works in continuous conduction mode (CCM) under heavy loads. When the load decreases, the MPQ4276A first enters discontinuous conduction mode (DCM) with a fixed frequency while the inductor current (I_L) approaches 0A. If the load decreases further or there is no load, then the peak I_L may drop below the advanced asynchronous modulation (AAM) mode peak current. If this occurs, then the MPQ4276A enters sleep mode to improve light-load efficiency while consuming a low quiescent current (I_Q).

In sleep mode, the internal clock is blocked, and the MPQ4276A skips a few pulses. When V_{FB} falls below V_{REF}, V_{COMP} ramps up until the peak I_L exceeds the AAM mode threshold. Then the internal clock is reset, and the crossover time is used as the benchmark for the next clock cycle. This control scheme helps achieve high efficiency by scaling down the frequency to reduce switching and gate driver losses.

As I_{OUT} increases under light-load conditions, V_{COMP} and f_{SW} also increase. If I_{OUT} exceeds the critical level set by V_{COMP}, then the MPQ4276A resumes fixed-frequency PWM control (see Figure 5).

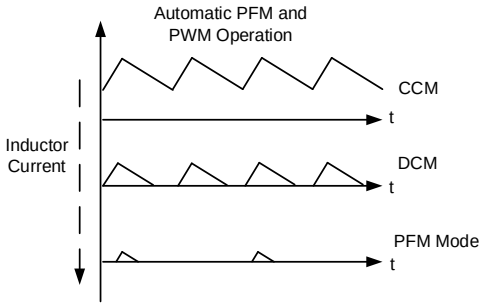


Figure 5: Automatic PFM and PWM Operation

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors V_{IN}. The UVLO rising threshold is 5V, and its falling threshold is 4.35V.

Internal Soft Start (SS)

Soft start (SS) prevents the converter V_{OUT} from overshooting during start-up. When the chip starts up, the internal circuitry generates an SS voltage (V_{SS}) that ramps up from 0V to 5V. When V_{SS} is below V_{REF}, the EA uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the EA uses V_{REF} as the reference.

The SS time (t_{SS}) is set to 2ms internally. If the MPQ4276A's output is pre-biased to a certain voltage during start-up, then the IC disables the switching of the high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET) until the voltage on the internal SS capacitor (C_{SS}) exceeds the internal V_{FB}.

Over-Current Protection (OCP)

The MPQ4276A has a cycle-by-cycle over-current (OC) limit when the peak I_L exceeds the current limit threshold and V_{FB} drops below the under-voltage (UV) threshold. Once the UV condition is triggered, the MPQ4276A enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground. This greatly reduces the average short-circuit current, alleviates thermal issues, and protects the regulator. Once the over-current (OC) condition is removed, the MPQ4276A exits hiccup mode and resumes normal operation.

Output Over-Voltage Protection (OVP)

The MPQ4276A has V_{OUT} over-voltage protection (OVP). If V_{OUT} exceeds 5.85V, the HS-FET stops turning on. The LS-FET turns on to discharge V_{OUT} until it falls to 5.7V. Then the chip resumes normal operation.

Floating Driver and Bootstrap (BST) Charging

An external bootstrap (BST) capacitor (C_{BST}) powers the floating power MOSFET driver, which has its own UVLO protection. The UVLO rising threshold is 2.2V, with a 150mV hysteresis. The C_{BST} voltage is regulated internally by V_{IN} and VCC through D1, D2, M1, C4, L1, and C2 (see Figure 6). C_{BST} (C4) is quickly charged by turning on M1 when the LS-FET turns on. If the LS-FET does not turn on, the 2.5μA input-to-BST current source can charge C_{BST}.

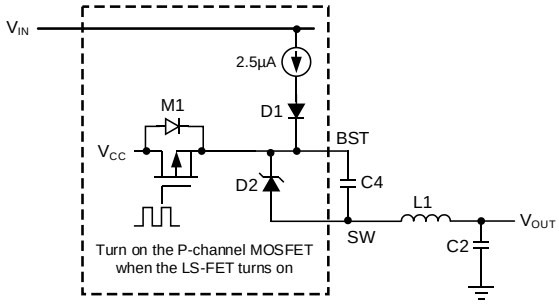


Figure 6: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both IN and EN exceed their respective thresholds, the buck converter is enabled. The reference block starts first, generating a stable V_{REF} and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Four events can shut down the converter:

- EN1 and EN2 going high while and EN goes low
- EN1 and EN2 going low, and CC1, CC2, CC3, and CC4 are disconnected when EN goes low
- IN going low
- Thermal shutdown

During shutdown, the signaling path is blocked to avoid any accidental fault triggering. Then V_{COMP} and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

Output Impedance

The MPQ4276A does not provide an output discharge function during EN shutdown. After EN shuts down, there are only two FB resistors connected to OUT. These resistors have a typical resistance of 175kΩ.

USB Current-Limit Switch

The MPQ4276A integrates two USB current-limit switches. The MPQ4276A provides built-in SS circuitry to control the V_{OUT} rising slew rate to limit inrush current and voltage surges.

When the load current reaches the current-limit threshold, the USB power MOSFET works in constant-current limit mode (see Figure 7). If the OC condition lasts longer than 5ms (V_{OUT} does not drop too low), then the corresponding USB channel enters hiccup mode. Hiccup mode has a 5ms on time and a 2s off time. The second USB switch and buck converter output operate normally.

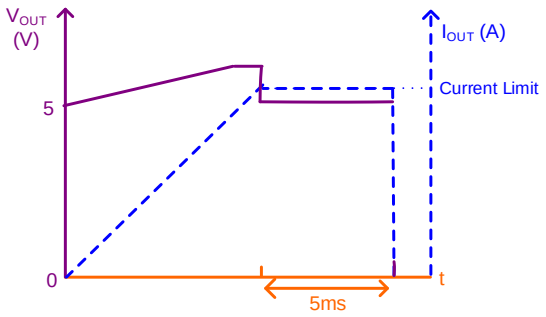


Figure 7: Over-Current Limit

If the USB V_{OUT} is below 3.5V for longer than 50µs after SS, then the MPQ4276A enters hiccup mode without having to wait 5ms (see Figure 8). This prevents an abnormal temperature rise during the constant resistor (CR) load OC condition.

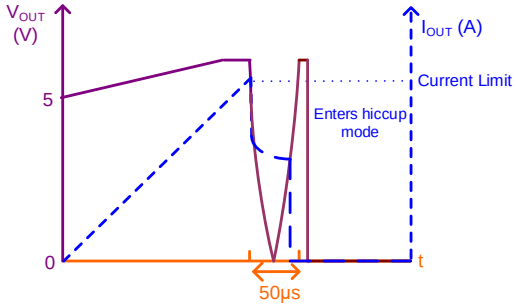


Figure 8: Over-Current Limit for CR Load

Fast Response for Short-Circuit Protection (SCP)

If the load current increases rapidly due to a short-circuit event, then the current may exceed the current-limit threshold before the control loop is able to respond. If the current reaches the 7A secondary current-limit level, then a fast turn-off circuit activates to turn off the power MOSFET. This limits the peak current through the MOSFET to prevent the converter's output from dropping so low that it affects the other USB channel. The total short-circuit response time is shorter than 1µs.

When the fast turn-off function is triggered, the MOSFET turns off for 100µs and restarts with SS. If the short remains during the restart process, the MPQ4276A regulates the gate voltage to maintain the current at a normal current limit level.

Output Line Drop Compensation

The MPQ4276A can compensate for a V_{OUT} drop (e.g. high impedance caused by a long trace) to maintain a fairly constant V_{OUT}.

The internal comparator compares the current-sense V_{OUT} of the two current-limit switches and uses the greater current-sense V_{OUT} to compensate for the line drop voltage.

The line drop compensation amplitude increases linearly as the load current increases. The line drop compensation is 70mV when I_{OUT} is 2.4A.

USB Output Over-Voltage (OV) Clamp

To protect the device at the cable terminal, the USB switch output has a fixed over-voltage protection (OVP) threshold. If V_{IN} exceeds the OVP threshold, then V_{OUT} is clamped to its OVP threshold.

USB Output Discharge and Impedance

Each USB switch has a fast discharge path that can quickly discharge the external output capacitor (C_{OUT}) during shutdown. This function is active when the CCx pins are released or the part is disabled (V_{IN} is below the UVLO threshold, EN1 and EN2 pull high, or EN1 and EN2 pull low while CC1, CC2, CC3, and CC4 are disconnected). If the USB V_{OUT} is discharged below 50mV, the discharge path turns off. After the fast discharge path turns off, there is only a high-impedance resistor (typically 500kΩ) connected from USB1 or USB2 to ground.

USB Enable On/Off Control (EN1 and EN2)

EN1 and EN2 are the on and off control input pins for USB1 and USB2, respectively. When EN1 and EN2 are pulled low, the USB switch is active. Pull V_{EN1} and V_{EN2} high to shut down the USB switch with an output discharge. For automatic start-up, EN1 and EN2 are pulled low by an internal 1MΩ resistor. EN1 and EN2 can also be controlled by an external on/off signal (see Table 2 on page 19).

Fault Indication (FLT1 and FLT2)

FLT1 and FLT2 are the fault indication pins for USB1 and USB2, respectively. FLT is an open drain during shutdown, start-up, and normal conditions. If the USB switch enters hiccup mode or over-temperature protection (OTP) is triggered, then FLT is pulled low. FLT asserts logic low on an individual USB switch during an OC or over-temperature (OT) condition. Once the fault condition is removed and the USB V_{OUT} goes high again, FLT switches high.

USB Type-C Mode and VCONN Voltage (V_{CONN})

For a USB Type-C solution, two pins on the connector (CC1 and CC2) establish and manage the source-to-sink connection. A blocking circuit prevents leakage from the CCx pin to VCC, and passes USB-IF Type-C certification testing. The general concept for setting up a valid connection between a source and sink is based on detecting terminations within the connected device. To help define the CCx pin's functional behavior, a pull-up resistor (R_P) and pull-down resistor (R_D, about 5.1kΩ) termination model is utilized (see Figure 9).

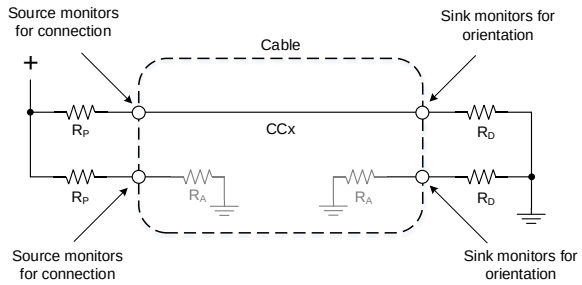


Figure 9: Current Source and Pull-Down CCx Model

Initially, a source exposes independent R_P terminations on its CC1 and CC2 pins, and a sink exposes independent R_D terminations on its CC1 and CC2 pins. The circuit configuration's source-to-sink combination represents a valid connection. To detect this connection, the source monitors CC1 and CC2 for a voltage below its unterminated voltage. Choose R_P based on the pull-up termination voltage and the source's detection circuit, which indicate a connection with a sink, a powered cable, or a sink connected via a powered cable.

Prior to applying V_{CONN}, a powered cable exposes R_A (typically 1kΩ) on its VCONN pin. R_A represents the load on VCONN in addition to any resistive elements connected to ground. In some cable plugs, this might be a pure resistance, while in other plugs, it may simply be the load.

The source must be able to differentiate between the presence of R_D and R_A to detect whether a sink is connected, and where to apply V_{CONN}. The source is not required to source V_{CONN} unless R_A is detected.

Two special termination combinations on the CCx pins, as seen by a source, are defined for directly connected accessory modes: R_A/R_A for audio adapter accessory mode, and R_D/R_D for debug accessory mode. V_{BUS} is disabled in both scenarios (see Figure 10).

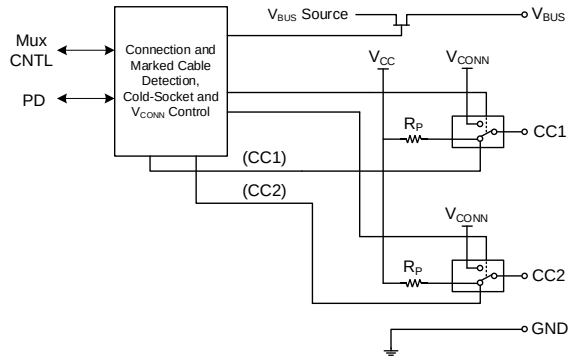


Figure 10: CCx Functional Block

The CC1 and CC2 functional block is described in further detail below:

1. The source uses a MOSFET to enable and disable power delivery across V_{BUS}. The source is disabled initially.
2. The source supplies pull-up resistors (R_P) on CC1 and CC2, then monitors both pins to detect a sink. The presence of a pull-down resistor (R_D) on either pin indicates that a sink is connected. R_P indicates the

initial USB Type-C current level supported by the host. The MPQ4276A's default R_P is 10kΩ, which represents a 3A current level.

3. The source uses CCx's pull-down characteristics to detect and determine which CC pin is intended to supply power to VCONN when R_A is detected.
4. Once a sink is detected, the source enables V_{BUS} and V_{CONN}.
5. The source can dynamically adjust R_P to indicate a change in the available USB Type-C current to the sink (e.g. at higher temperatures, the MPQ4276A changes R_P to 22kΩ to indicate a 1.5A current ability).
6. The source monitors the continued presence of R_D to detect whether the sink is disconnected. When a disconnect event is detected, the source is removed, and V_{BUS} and V_{CONN} return to step 2.

Load-Shedding vs. Temperature

The MPQ4276A monitors the die temperature and dynamically changes its I_{OUT} capability. If the die temperature exceeds 135°C, then the USB port's CCx pull-up resistance (R_P) changes to 22kΩ to indicate that its source capability has changed to 1.5A. Meanwhile, V_{BUS} changes to 4.77V.

If the die temperature drops below 110°C for 16 seconds, then V_{BUS} reverts to the normal voltage set by OUT_SEL. Meanwhile, the USB Type-C current capability changes back to 3A (R_P = 10kΩ). The current-limit threshold remains at 5A during this period.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the silicon die temperature exceeds 165°C, the entire chip shuts down. Once the temperature falls below its lower threshold (typically 145°C), the chip is enabled and resume normal operation.

Table 2: CCx Logic Truth Table

EN	EN1	EN2	USB1 CCx (10)	USB2 CCx (10)	Buck Converter	VCONN (USB1)	USB1	VCONN (USB2)	USB2
0	1	1	-	-	Disabled	Disabled	Disabled	Disabled	Disabled
0	0	1	Connected	-	Enabled	Enabled	Enabled	Disabled	Disabled
			Disconnected	-	Disabled	Disabled	Disabled	Disabled	Disabled
0	1	0	-	Connected	Enabled	Disabled	Disabled	Enabled	Enabled
			-	Disconnected	Disabled	Disabled	Disabled	Disabled	Disabled
0	0	0	Connected	Connected	Enabled	Enabled	Enabled	Enabled	Enabled
			Connected	Disconnected	Enabled	Enabled	Enabled	Disabled	Disabled
			Disconnected	Connected	Enabled	Disabled	Disabled	Enabled	Enabled
			Disconnected	Disconnected	Disabled	Disabled	Disabled	Disabled	Disabled
1	1	1	-	-	Enabled	Disabled	Disabled	Disabled	Disabled
1	1	0	-	Connected	Enabled	Disabled	Disabled	Enabled	Enabled
			-	Disconnected	Enabled	Disabled	Disabled	Disabled	Disabled
1	0	1	Connected	-	Enabled	Enabled	Enabled	Disabled	Disabled
			Disconnected	-	Enabled	Disabled	Disabled	Disabled	Disabled
1	0	0	Connected	Connected	Enabled	Enabled	Enabled	Enabled	Enabled
			Connected	Disconnected	Enabled	Enabled	Enabled	Disabled	Disabled
			Disconnected	Connected	Enabled	Disabled	Disabled	Enabled	Enabled
			Disconnected	Disconnected	Enabled	Disabled	Disabled	Disabled	Disabled

Note:

10) USB1 and USB2 are symmetrical to each other. "Connected" means that R_D and R_A are connected to the CCx pins. "Disconnected" means audio, debug, or open status. "-" means that any connections to the CCx pins are ignored.

APPLICATION INFORMATION

Selecting the Inductor

For most applications, it is recommended to use an inductor with a DC current rating at least 25% greater than the maximum load current. Select an inductor with a small DC resistance for optimal efficiency. For most designs, the inductance (L_1) can be estimated using Equation (2):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (2)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% to 50% of the maximum load current. The maximum inductor peak current ($I_{L(MAX)}$) can be calculated using Equation (3):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (3)$$

Selecting the Buck Converter's Input Capacitor (C_{IN})

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply AC current to the converter while maintaining the DC V_{IN}. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For automotive applications with a 450kHz f_{SW}, it is recommended to use a 100µF electrolytic capacitor and two 4.7µF ceramic capacitors.

Since C_{IN} (C1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in C_{IN} (I_{C1}) can be estimated using Equation (4):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated using Equation (5):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (5)$$

For simplification, choose C_{IN} with an RMS current rating greater than half of the maximum load current.

C_{IN} can be electrolytic, tantalum, or ceramic. When using an electrolytic capacitor, place two additional high-quality ceramic capacitors as close to IN as possible. The input voltage ripple caused by the capacitance (ΔV_{IN}) can be estimated using Equation (6):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

Selecting the Buck Converter's Output Capacitor (C_{OUT})

The step-down converter requires C_{OUT} (C2) to maintain the DC V_{OUT}. The output voltage ripple (ΔV_{OUT}) can be estimated using Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (7)$$

Where L_1 is the inductance, and R_{ESR} is the C_{OUT} ESR value.

For an electrolytic capacitor, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be calculated using Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (8)$$

For the application, it is recommended to use a 100µF to 270µF capacitor with an ESR below 50mΩ (e.g. polymer or tantalum capacitors) and two 2.2µF ceramic capacitors (see Table 3 on page 21).

Table 3: Recommended External Components

f_{SW}	Inductor	C_{IN}	C_{OUT}
235kHz	8µH	2 x 4.7µF ceramic capacitor + 100µF electrolytic capacitor	2 x 2.2µF ceramic capacitor + 100µF polymer capacitor
450kHz	4.7µH	2 x 4.7µF ceramic capacitor + 100µF electrolytic capacitor	2 x 2.2µF ceramic capacitor + 100µF polymer capacitor

ESD Protection for I/O Pins

Higher ESD levels should be considered for all USB I/O pins. The MPQ4276A features high ESD protection up to ±7kV on a human body model (HBM) on USB1 and USB2, and ±1.8kV on a HBM on CC1, CC2, CC3, and CC4. The ESD structures can withstand high ESD during normal operation and when the device is turned off. To further extend CCx's ESD level for most application environments, additional ESD diodes can be placed on the CCx pins (see Figure 11).

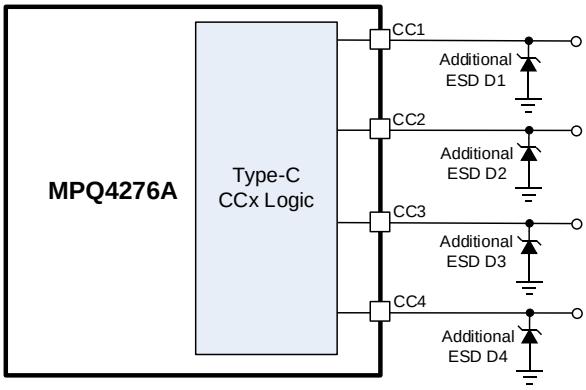


Figure 11: Enhancing ESD on the CCx Pins

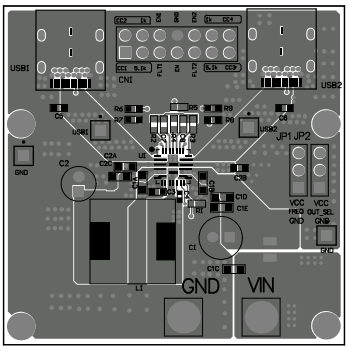
PCB Layout Guidelines (11)

Efficient PCB layout is critical for stable operation and thermal dissipation. For the best results, refer to Figure 12 and follow the guidelines below:

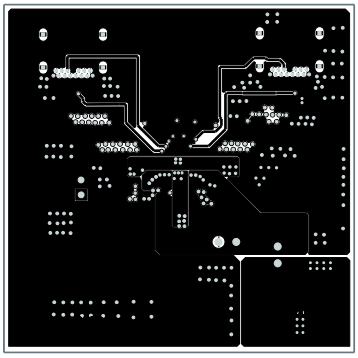
1. Connect the OUT pin to the PCB using short, direct, and wide traces.
2. Add vias under the IC.
3. Route the OUT trace on both PCB layers.
4. Place the buck converter's ceramic C_{OUT} (C2A) on the left side of the MPQ4276A, then place the second C_{OUT} (C2B) on the right side of the MPQ4276A.
5. Add a large copper plane for PGND.
6. Add multiple vias to improve thermal dissipation.
7. Connect AGND to PGND.
8. Place a large copper plane on the PCB for SW, USB, and USB2.
9. Route the USB1 and USB2 traces on both PCB layers.
10. Place two ceramic, decoupling C_{IN} as close to IN and PGND as possible to improve EMI performance.
11. Place the symmetric C_{IN} on each side of the IC.
12. Place C_{BST} close to BST and SW.
13. Place the VCC decoupling capacitor as close to VCC as possible.

Note:

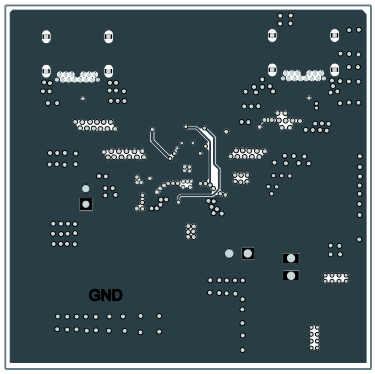
11) The recommended layout is based on Figure 13 on page 23.



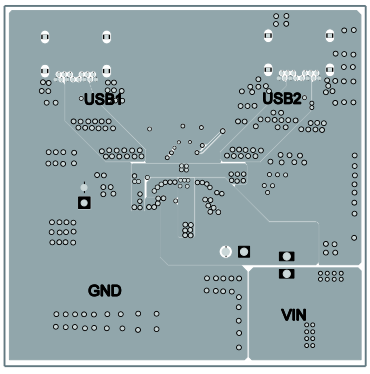
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 12: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

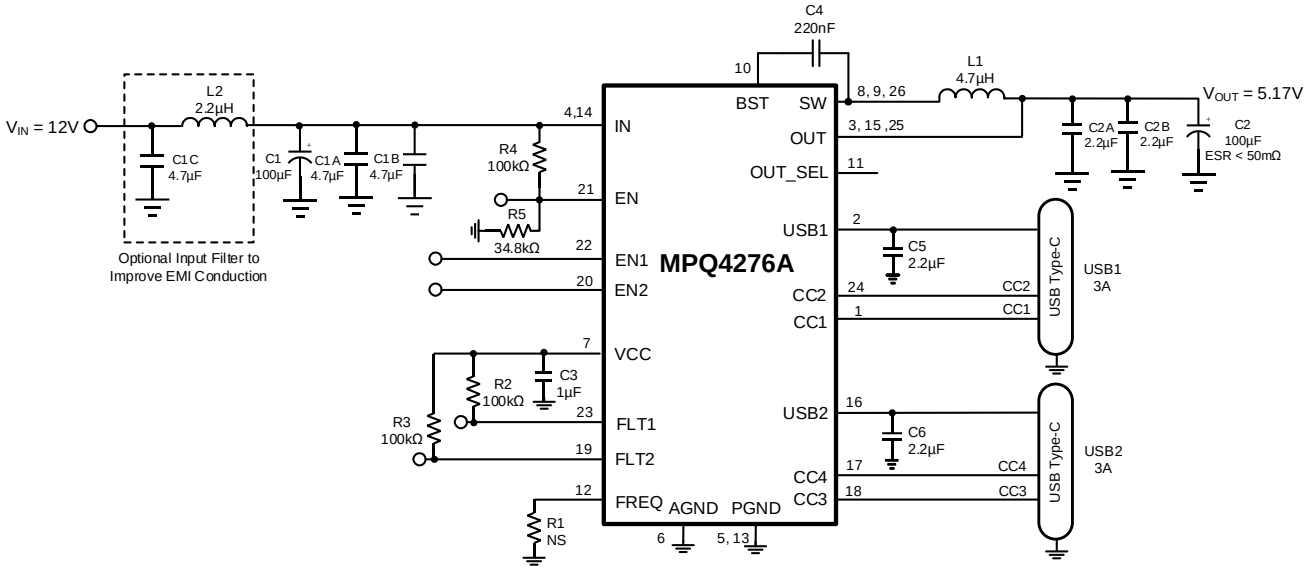


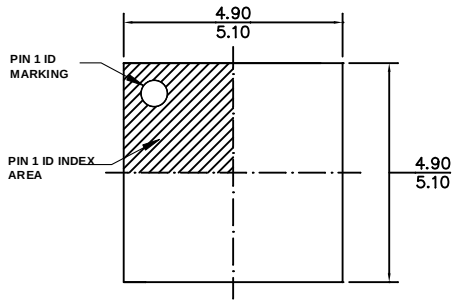
Figure 13: Dual USB Type-C 5V/3A DFP Ports (12)

Note:

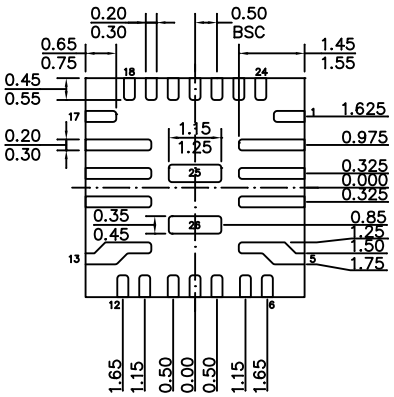
12) See Figure 11 on page 21 for details on how to enhance the ESD protection ratings on the CCx pins.

PACKAGE INFORMATION

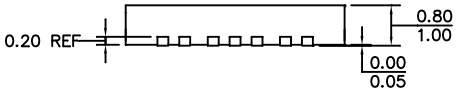
QFN-26 (5mmx5mm)



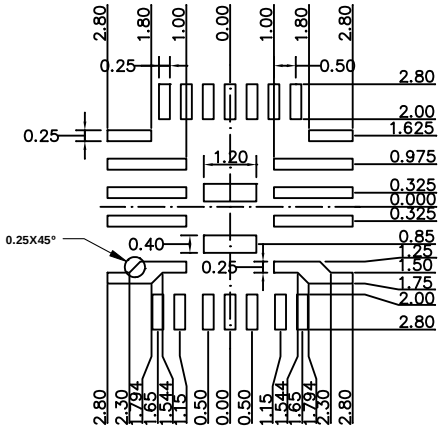
TOP VIEW



BOTTOM VIEW



SIDE VIEW

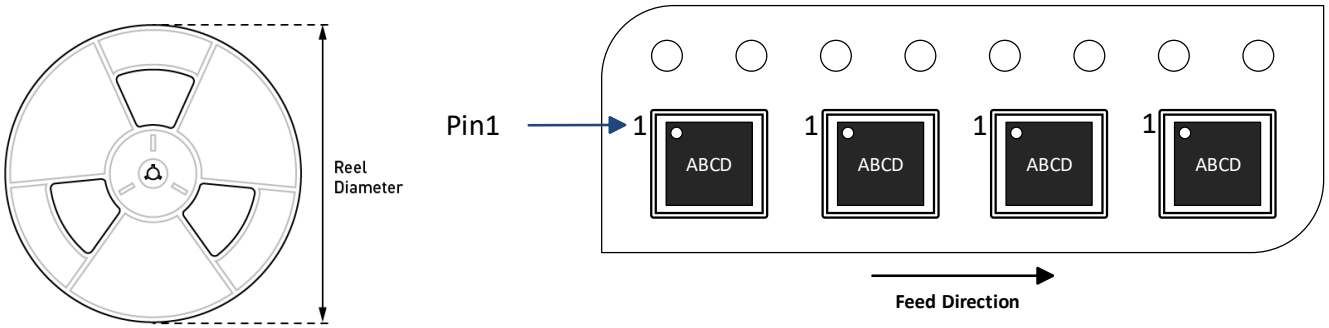


RECOMMENDED LAND PATTERN

NOTE:

1) THE LAND PATTERNS OF PINS 2, 3, AND 4, AS WELL AS PINS 14, 15, AND 16 HAVE THE SAME LENGTH AND WIDTH.
2) THE LAND PATTERNS OF PIN 5 AND PIN 13 HAVE THE SAME LENGTH AND WIDTH.
3) ALL DIMENSIONS ARE IN MILLIMETERS.
4) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
5) REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4276AGU-AEC1-Z	QFN-26 (5mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/9/2022	Initial Release	-