MPQ4312

45V, 2A, Low I_Q, Synchronous Step-Down Converter with Frequency Spread Spectrum, AEC-Q100 Qualified

DESCRIPTION

The MPQ4312 is a configurable-frequency, synchronous step-down switching converter with integrated internal high-side and low-side power MOSFETs (HS-FET and LS-FET, respectively). It provides up to 2A of highly efficient output current (I_{OUT}) with current mode control for fast loop response.

The wide 3.3V to 45V input voltage (V_{IN}) range accommodates a variety of step-down applications in automotive input environments. A 1.7µA shutdown mode quiescent current allows the device to be used in battery-powered applications.

High power conversion efficiency across a wide load range is achieved by scaling down the switching frequency (f_{SW}) under light-load conditions to reduce the switching and gate driver losses. An open-drain power good (PG) signal indicates whether the output is within 95% to 105% of its nominal voltage.

Frequency foldback helps prevent inductor current runaway during start-up. Thermal shutdown provides reliable, fault-tolerant operation. High-duty cycle and low-dropout mode are provided for automotive cold-crank conditions.

The MPQ4312 is available in a QFN-20 (4mmx4mm) package.

MPQ4312 FAMILY VERSIONS

Part Number	Output Current	Package Options
MPQ4312	2A	QFN-20 (4mmx4mm) WF (1)
MPQ4313	3A	
MPQ4314	4A	
MPQ4315	5A	
MPQ4316	6A	
MPQ4317	7A	

Note:

1) WF means wettable flank.

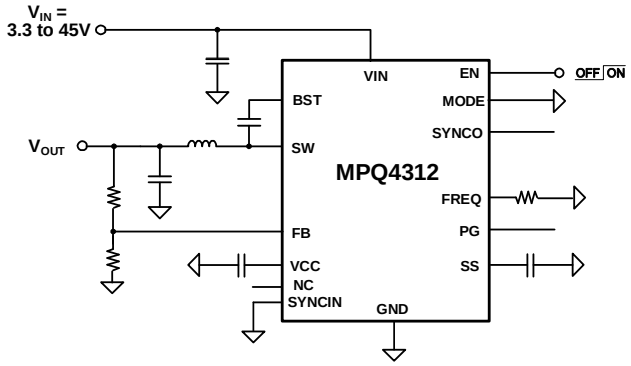
FEATURES

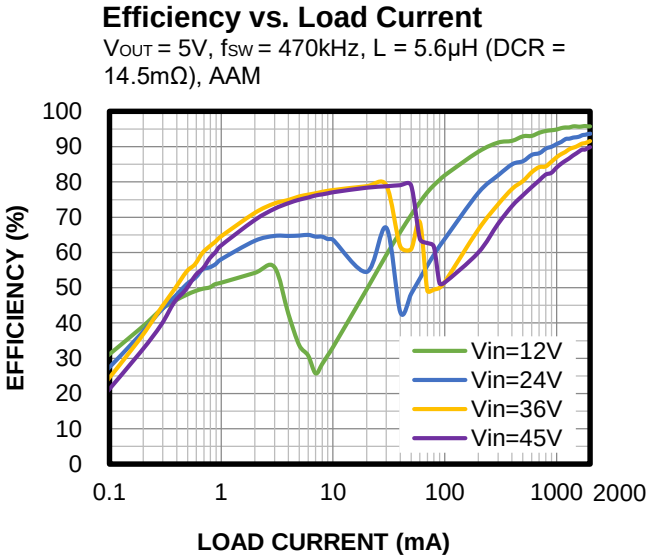
- Wide 3.3V to 45V Operating Input Voltage (V_{IN}) Range
- 2A Continuous Output Current (I_{OUT})
- 1.7µA Low Shutdown Supply Current (I_{SHDN})
- 18µA Sleep Mode Quiescent Current
- Internal 48mΩ High-Side and 20mΩ Low-Side MOSFETs
- 350kHz to 1000kHz Configurable Switching Frequency (f_{SW}) for Car Battery Applications
- Synchronizable with External Clock
- Out-of-Phase Synchronized Clock Output
- Frequency Spread Spectrum (FSS) for Low EMI
- Symmetric V_{IN} for Low EMI
- Power Good (PG) Output
- External Soft Start (SS)
- 100ns Minimum On Time
- Selectable Advanced Asynchronous Mode (AAM) or Forced Continuous Conduction Mode (FCCM)
- Low-Dropout Mode
- Hiccup Over-Current Protection (OCP)
- Available in a QFN-20 (4mmx4mm) Package
- Available in a Wettable Flank Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Automotive Infotainment
- Automotive Clusters
- Advanced Driver Assistance Systems (ADAS)
- Industrial Power Systems

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ4312GRE-AEC1***	QFN-20 (4mmx4mm)	*See Below*	1

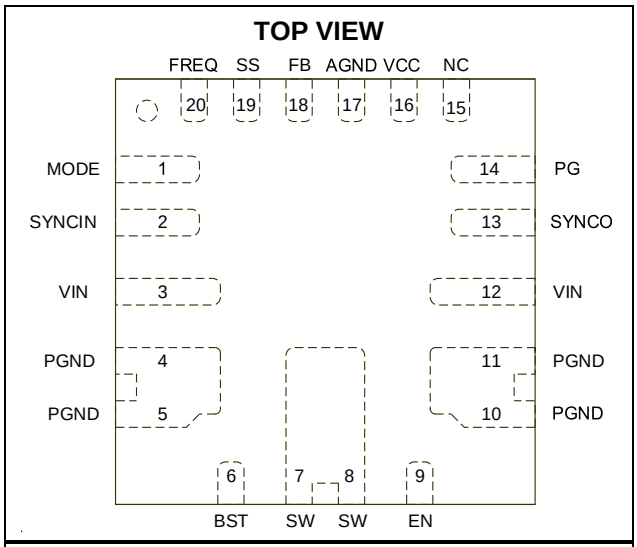
* For Tape & Reel, add suffix -Z (e.g. MPQ4312GRE-AEC1-Z).
** Moisture Sensitivity Level Rating
*** Wettable Flank

TOP MARKING (MPQ4312GRE-AEC1)

MPSYWW
MP4312
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
MP4312: Part number
LLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-20 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	MODE	**AAM or FCCM selection pin.** Pull this pin high to make the MPQ4312 operate in forced continuous conduction mode (FCCM). Pull it low to make it operate in advanced asynchronous modulation (AAM) mode under light-load conditions. Do not float this pin.
2	SYNCIN	**SYNC input.** Apply a 350kHz to 1000kHz clock signal to this pin to synchronize the internal oscillator frequency to the external clock. This pin is also used for multi-phase operation. This pin is internally high impedance. Do not float this pin under any circumstances. If used, ensure that the external sync clock has adequate pull-up and pull-down capability. It is recommended to place a $\leqslant$51kΩ resistor between the pin and GND in case the external sync clock's pull-down capability is not strong enough or the pin enters a high-impedance (Hi-Z) state.
3, 12	VIN	**Input supply.** VIN supplies power to all of the internal control circuitry, as well as the power MOSFET, which is connected to SW. To minimize switching spikes, it is recommended to connect a decoupling capacitor from VIN to ground, as close to VIN as possible.
4, 5, 10, 11	PGND	**Power ground.**
6	BST	**Bootstrap.** BST is the positive power supply for the high-side MOSFET (HS-FET) driver connected to SW. Connect a bypass capacitor between this BST and SW. See the Application Information section on page 32 to calculate the size for this capacitor.
7, 8	SW	**Switch node.** SW is the output of the internal power MOSFET.
9	EN	**Enable.** Pull this pin below the specified threshold (0.85V) to shut down the chip. Pull it above the specified threshold (1V) to enable the chip.
13	SYNCO	**SYNC output.** The SYNCO pin outputs a clock signal that is 180° out of phase with the internal oscillator signal. It can also output a signal that is opposite to the clock signal applied at the SYNCIN pin. Float this pin if it is not used.
14	PG	**Power good indicator.** PG is an open-drain output. Use a pull-up resistor when connecting PG to a power source. If the output voltage (V_{OUT}) is within 95% to 105% of the nominal voltage, PG goes high. If V_{OUT} is above 106.5% or below 93% of the nominal voltage, then PG goes low.
15	NC	**Not connected.** Float this pin.
16	VCC	**Bias supply.** This pin supplies power to the internal control circuitry and gate drivers. A decoupling capacitor connected to ground must be placed close to this pin. See the Selecting the VCC Capacitor section on page 33 to calculate the size for this capacitor.
17	AGND	**Analog ground.**
18	FB	**Feedback input.** Connect FB to the midpoint of the external resistor feedback divider, between the output and AGND. This sets the output voltage. The feedback threshold voltage is 0.815V. Place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces.
19	SS	**Soft-start input.** Place a capacitor from SS to GND to set the soft-start time (t_{SS}). The MPQ4312 sources 13μA from the SS pin to the soft-start capacitor (C_{SS}) during start-up. As the SS voltage (V_{SS}) rises, the feedback threshold voltage increases to limit inrush current during start-up.
20	FREQ	**Switching frequency selection.** Connect a resistor from this pin to ground to set the switching frequency (f_{SW}). To set the frequency, see the f_{SW} vs. R_{FREQ} curves on page 15.

ABSOLUTE MAXIMUM RATINGS (2)

VIN, EN ..... -0.3V to +50V
SW .....-0.3V to $V_{IN\ (MAX)}$ +0.3V
BST .....V_{SW} +5.5V
All other pins..... -0.3V to +5.5V
Continuous power dissipation (T_A= 25°C) (3) (5)
QFN-20 (4mmx4mm).....5.4W
Operating junction temperature.....150°C
Lead temperature .....260°C
Storage temperature.....-65°C to +150°C

Electrostatic Discharge (ESD) Rating

Human body model (HBM)..... ±2kV
Charged device model (CDM) ..... ±750V

Recommended Operating Conditions

Supply voltage (V_{IN}) ..... 3.3V to 45V
Output voltage (V_{OUT}).....0.815V to 0.95 x V_{IN}
Operating junction temp (T_J) ....-40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-20 (4mmx4mm)
JESD51-7 (4).....44.....9....°C/W
EVQ4312-R-00A (5)..... 23.....2.5...°C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
5) Measured on an MPS standard EVB: 9cmx9cm, 2-oz copper, 4-Layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VIN under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$		2.8	3	3.2	V
VIN UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$		2.5	2.7	2.9	V
VIN UVLO hysteresis	$V_{IN\_UVLO\_HYS}$			280		mV
VCC voltage	V_{CC}	I_{VCC} = 0A	4.6	4.9	5.2	V
VCC regulation		I_{VCC} = 30mA		1	4	%
VCC current limit	I_{LIMIT_VCC}	V_{CC} = 4V	100			mA
VIN quiescent current	I_Q	FB = 0.85V, no load, (sleep mode)		18	26	µA
VIN quiescent current (switching) (6)	I_{Q_ACTIVE}	MODE = GND (AAM), switching, no load, R_{FB_UP} = 1MΩ, R_{FB_DOWN} = 316kΩ		20		µA
		MODE = high (FCCM), switching, f_{SW} = 2MHz, no load		40		mA
		MODE = high (FCCM), switching, f_{SW} = 470kHz, no load		9.5		mA
VIN shutdown current	I_{SHDN}	EN = 0V		1.7	3.5	µA
FB reference voltage	V_{FB}	V_{IN} = 3.3V to 45V, T_J = 25°C	0.807	0.815	0.823	V
		V_{IN} = 3.3V to 45V	0.799	0.815	0.831	V
FB current	I_{FB}	V_{FB} = 0.85V	-50	0	+50	nA
Switching frequency	f_{SW}	R_{FREQ} = 62kΩ	420	470	520	kHz
		R_{FREQ} = 26.1kΩ	820	1000	1180	
Minimum on time (6)	t_{ON_MIN}			100		ns
Minimum off time (6)	t_{OFF_MIN}			80		ns
SYNCIN voltage rising threshold	V_{SYNC_RISING}		1.8			V
SYNCIN voltage falling threshold	$V_{SYNC\_FALLING}$				0.4	V
SYNCIN clock range	f_{SYNC}	External clock	350		1000	kHz
SYNCO high voltage	V_{SYNCO_HIGH}	I_{SYNCO} = -1mA	3.3	4.5		V
SYNCO low voltage	V_{SYNCO_LOW}	I_{SYNCO} = 1mA			0.4	V
SYNCO phase shift		Tested under SYNCIN		180		deg
High-side (HS) current limit	I_{LIMIT}	Duty cycle = 30%	4.4	5.5	6.6	A
Low-side (LS) valley current limit	I_{LIMIT_VALLEY}		3.2	4	4.8	A

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Zero-current detection (ZCD) current	I_{ZCD}	AAM	-0.15	0.10	+0.35	A
LS reverse current limit	$I_{LIMIT\_REVERSE}$	FCCM	2	4.5	7	A
Switch leakage current	I_{SW_LKG}			0.01	1	µA
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	V_{BST} - V_{SW} = 5V		48	80	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	V_{CC} = 5V		20	40	mΩ
Soft-start current	I_{SS}	V_{SS} = 0V	8	13	19	µA
EN rising threshold	V_{EN_RISING}		0.8	1.0	1.2	V
EN falling threshold	$V_{EN\_FALLING}$		0.65	0.85	1.05	V
EN hysteresis voltage	V_{EN_HYS}			190		mV
MODE rising threshold	V_{MODE_RISING}		1.8			V
MODE falling threshold	$V_{MODE\_FALLING}$				0.4	V
PG rising threshold (V_{FB} / V_{REF})	PG_{RISING}	V_{FB} rising	92%	95%	98%	V_{REF}
		V_{FB} falling	102%	105%	108%	
PG falling threshold (V_{FB} / V_{REF})	$PG_{FALLING}$	V_{FB} falling	90.5%	93.5%	96.5%	
		V_{FB} rising	103.5%	106.5%	109.5%	
PG output voltage low	V_{PG_LOW}	I_{SINK} = 1mA		0.1	0.3	V
PG rising delay	$t_{PG\_R\_DELAY}$			35		µs
PG falling delay	$t_{PG\_F\_DELAY}$			35		µs
Thermal shutdown (6)	T_{SD}			170		°C
Thermal shutdown hysteresis (6)	T_{SD_HYS}			20		°C

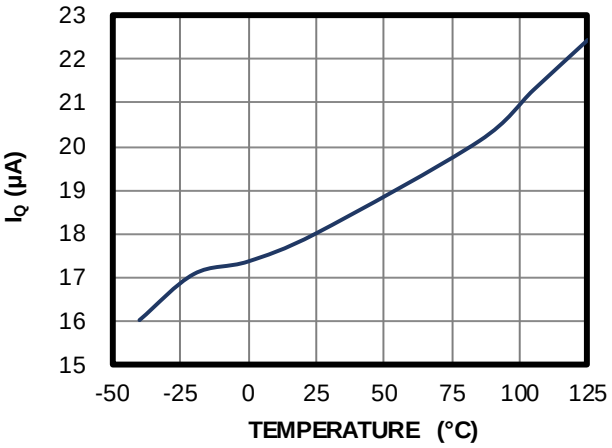
Note:

6) Derived from bench characterization. Not tested in production.

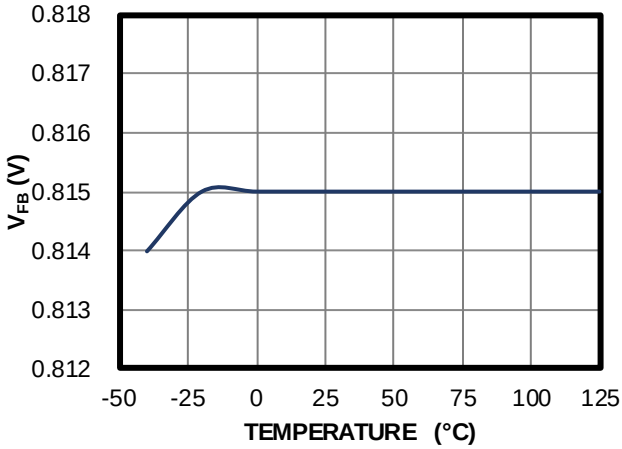
TYPICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

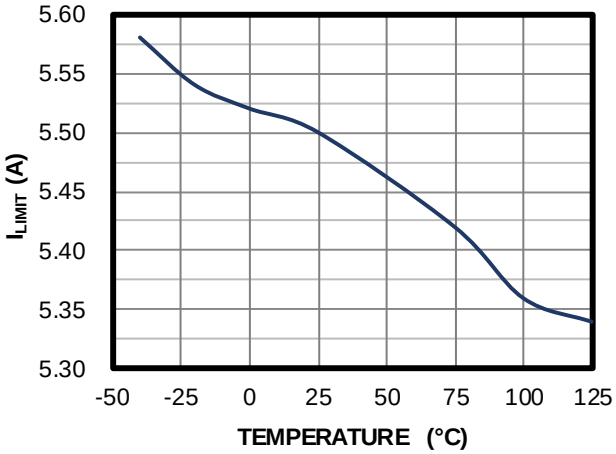
Quiescent Current vs. Temperature



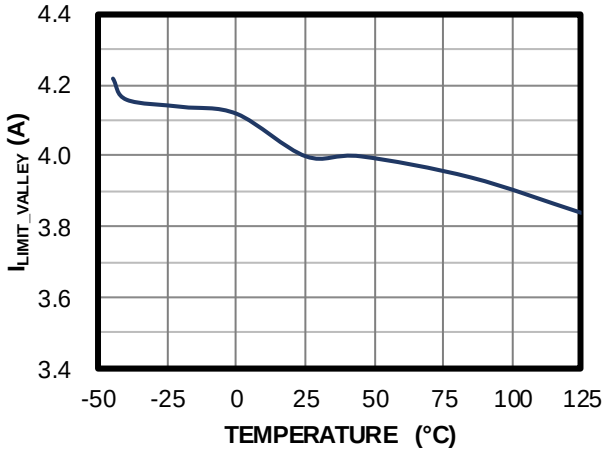
Feedback Voltage vs. Temperature



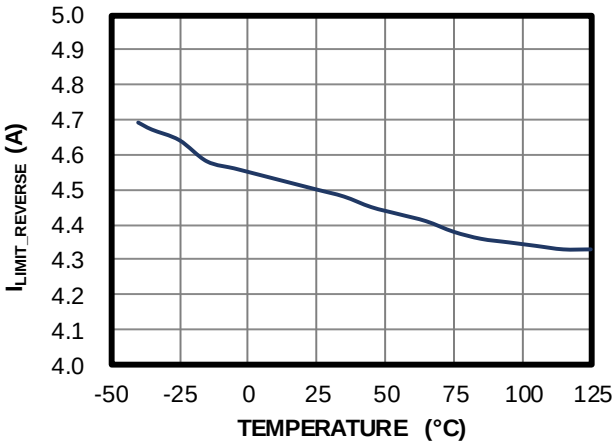
Current Limit vs. Temperature



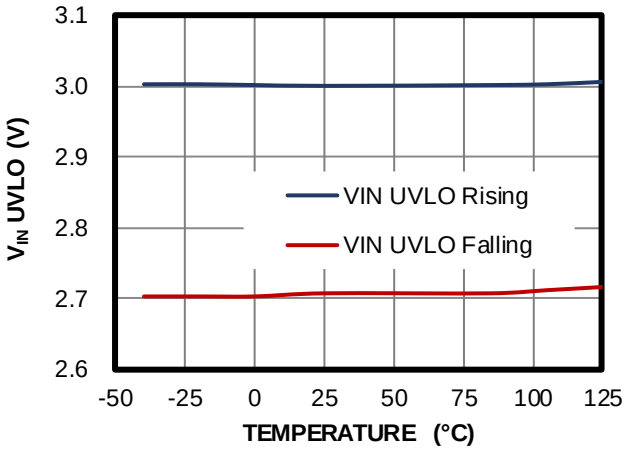
Valley Current Limit vs. Temperature



Reverse Current Limit vs. Temperature



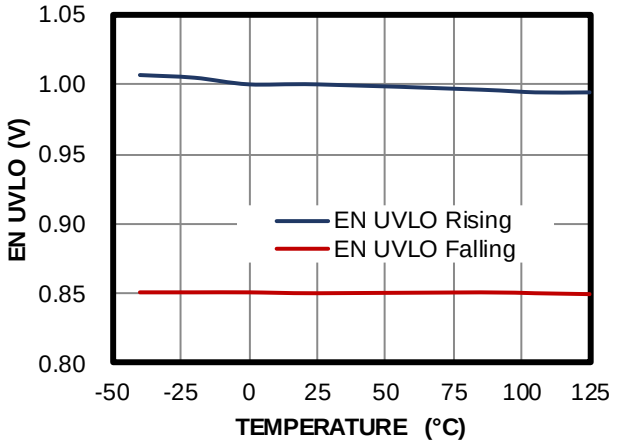
V_{IN} UVLO Threshold vs. Temperature



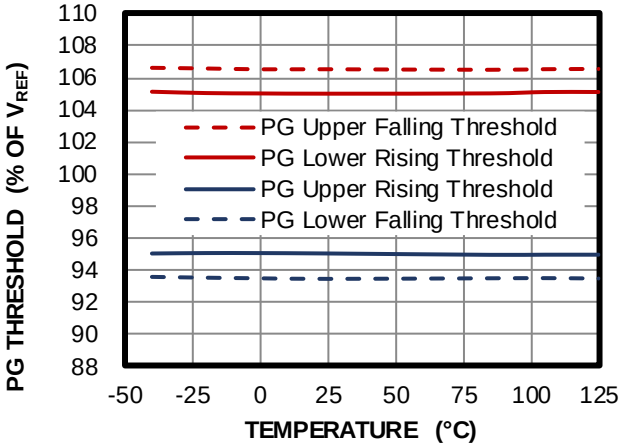
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

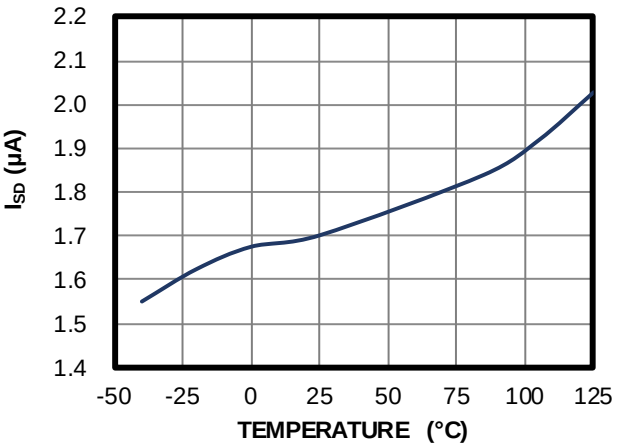
EN UVLO Threshold vs. Temperature



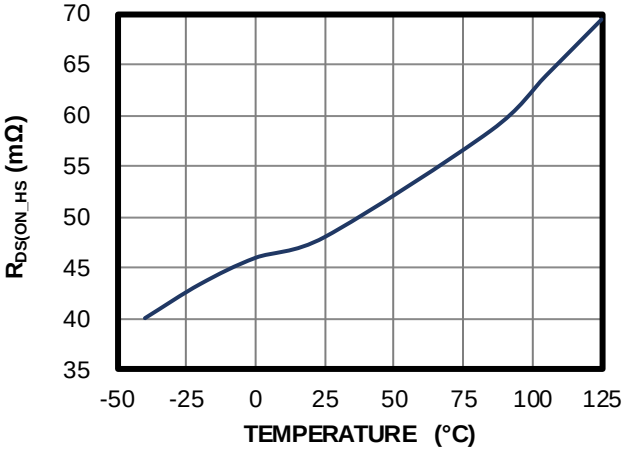
PG Rising/Falling Threshold vs. Temperature



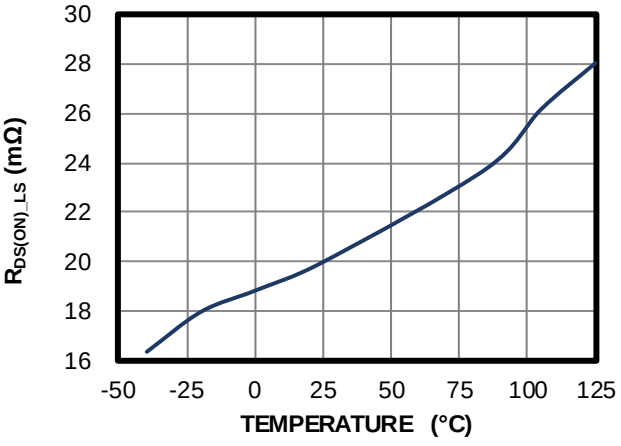
V_{IN} Shutdown Current vs. Temperature



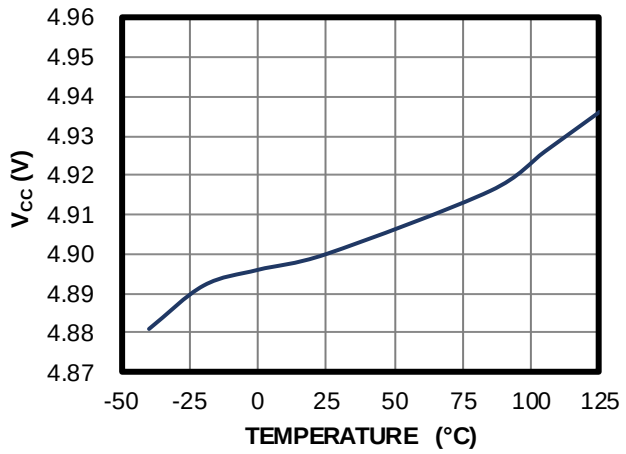
$R_{DS(ON)\_HS}$ vs. Temperature



$R_{DS(ON)\_LS}$ vs. Temperature



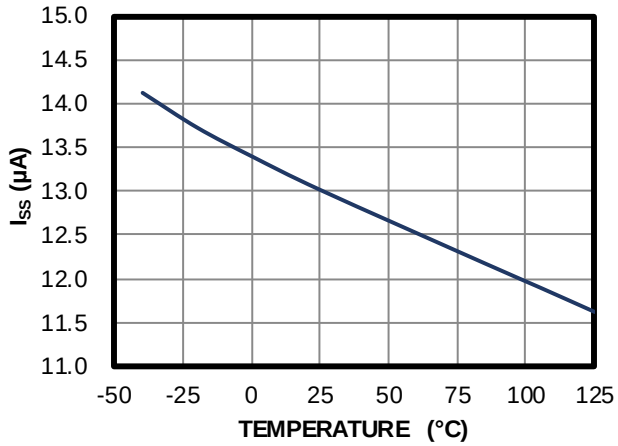
V_{CC} vs. Temperature



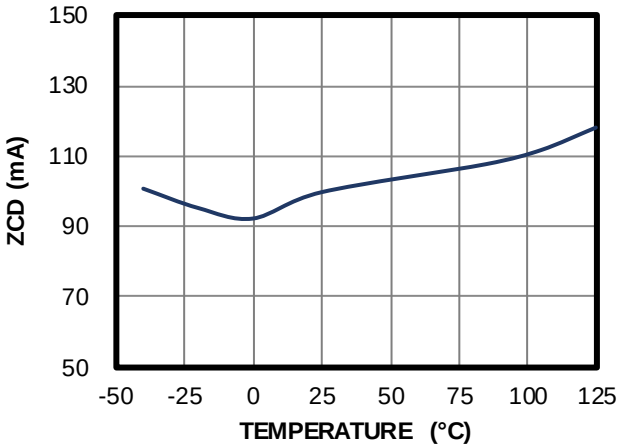
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Soft-Start Current vs. Temperature

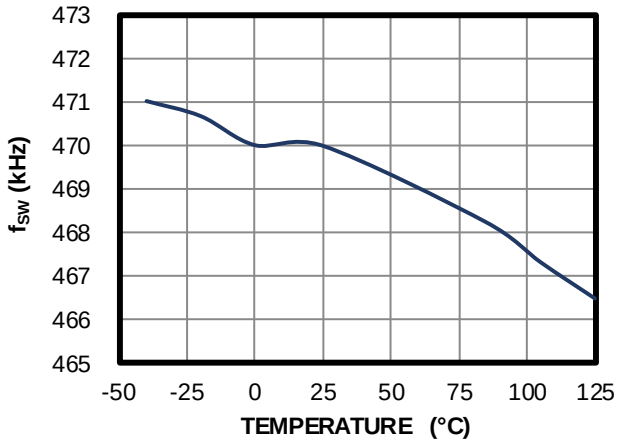


Zero-Current Detection vs. Temperature



f_{SW} vs. Temperature

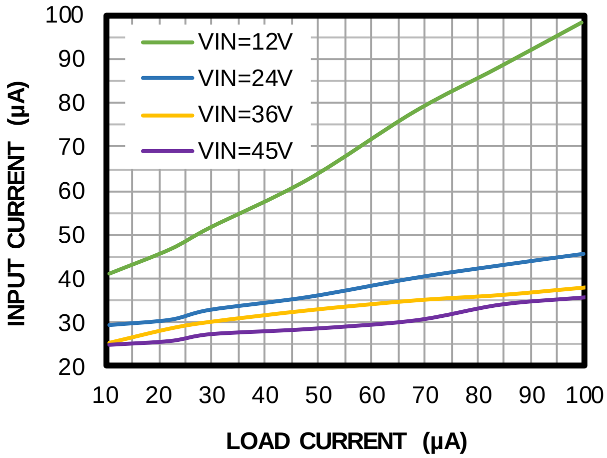
R_{FREQ} = 62kΩ



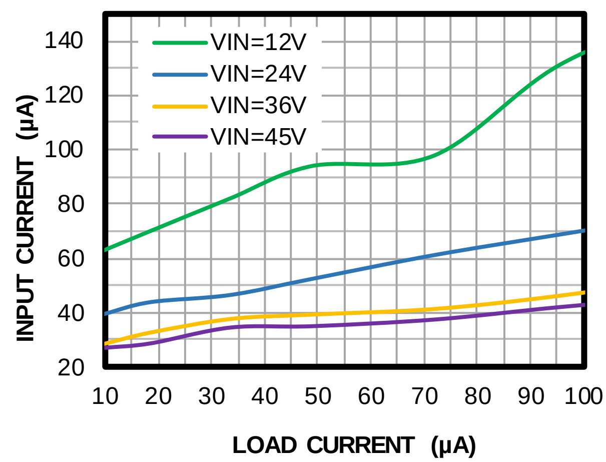
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 5.6µH [7], f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

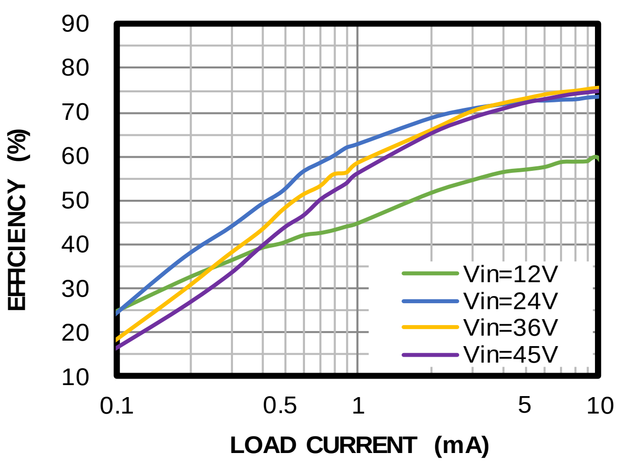
Input Current vs. Load Current
AAM mode, V_{OUT} = 3.3V



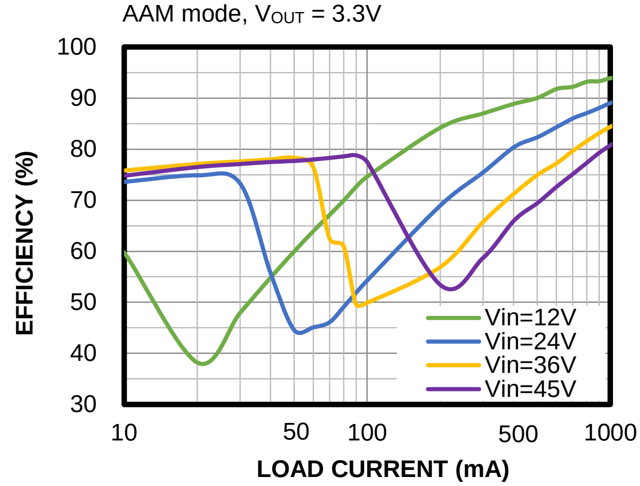
Input Current vs. Load Current
AAM mode, V_{OUT} = 5V



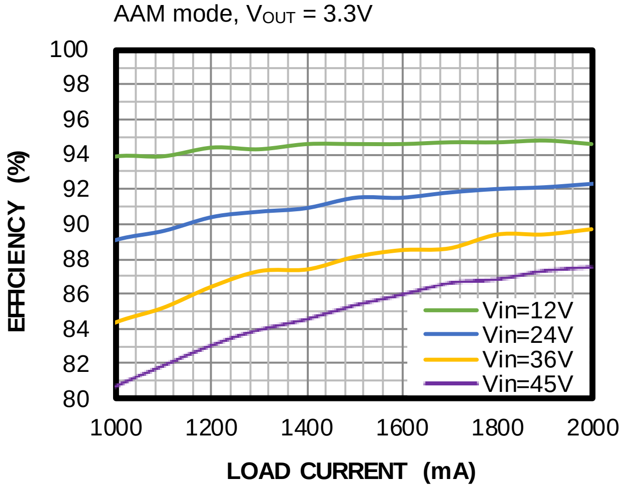
Efficiency vs. Load Current
AAM mode, V_{OUT} = 3.3V



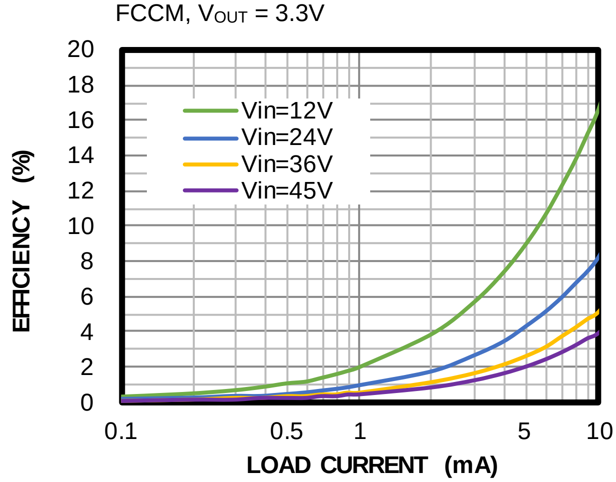
Efficiency vs. Load Current
AAM mode, V_{OUT} = 3.3V



Efficiency vs. Load Current
AAM mode, V_{OUT} = 3.3V



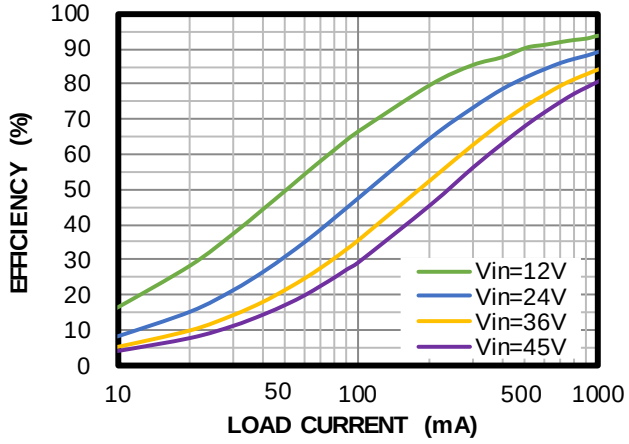
Efficiency vs. Load Current
FCCM, V_{OUT} = 3.3V



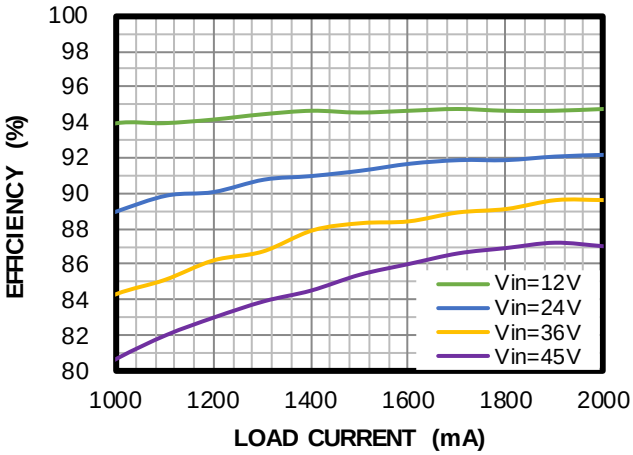
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 5.6µH [7], f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

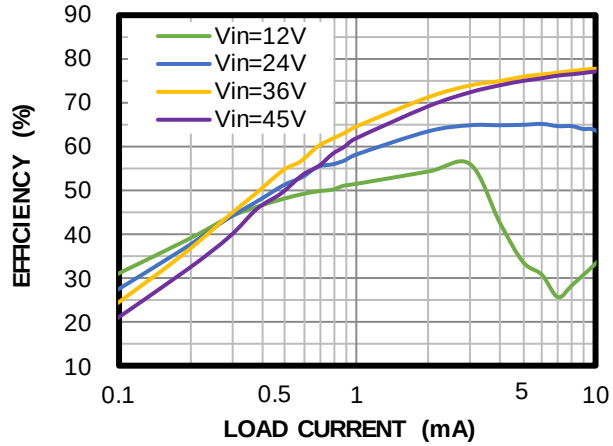
Efficiency vs. Load Current
FCCM, V_{OUT} = 3.3V



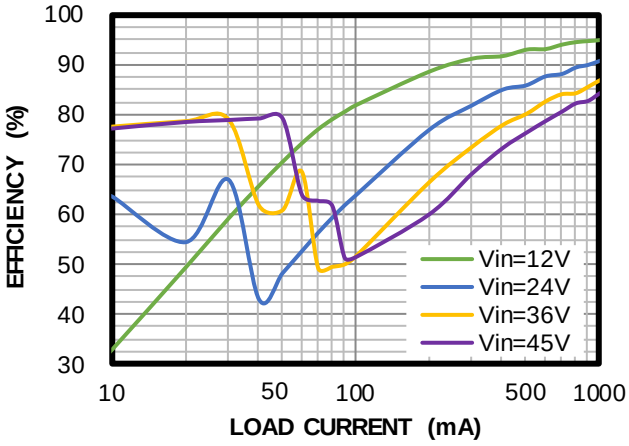
Efficiency vs. Load Current
FCCM, V_{OUT} = 3.3V



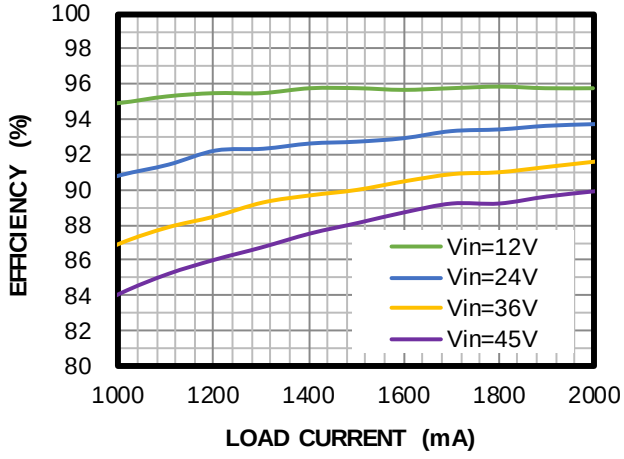
Efficiency vs. Load Current
AAM mode, V_{OUT} = 5V



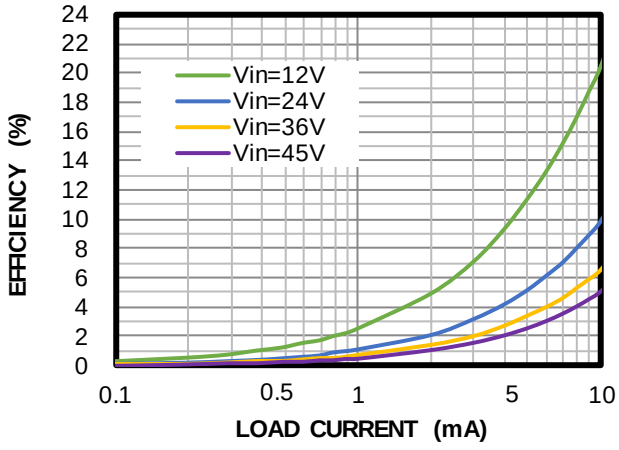
Efficiency vs. Load Current
AAM mode, V_{OUT} = 5V



Efficiency vs. Load Current
AAM mode, V_{OUT} = 5V



Efficiency vs. Load Current
FCCM, V_{OUT} = 5V

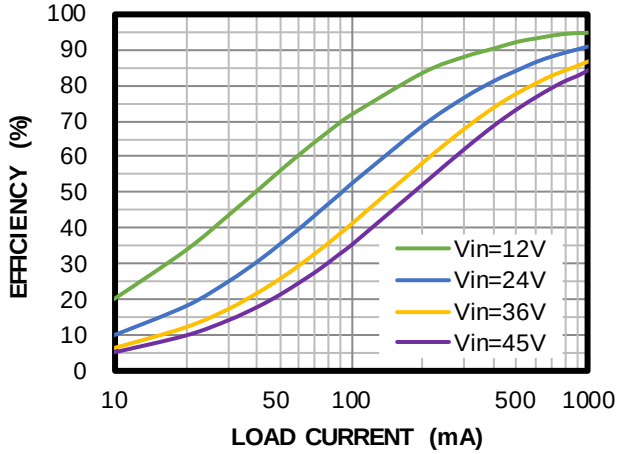


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 5.6µH [7], f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

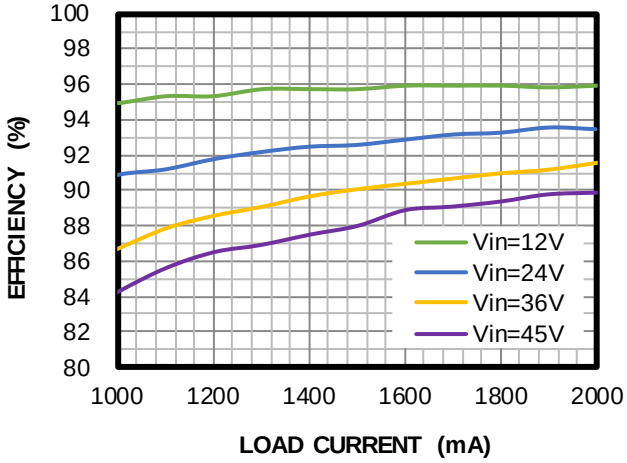
Efficiency vs. Load Current

FCCM, V_{OUT} = 5V



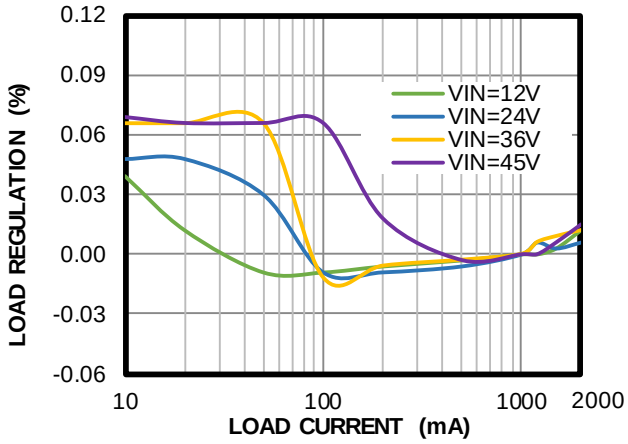
Efficiency vs. Load Current

FCCM, V_{OUT} = 5V



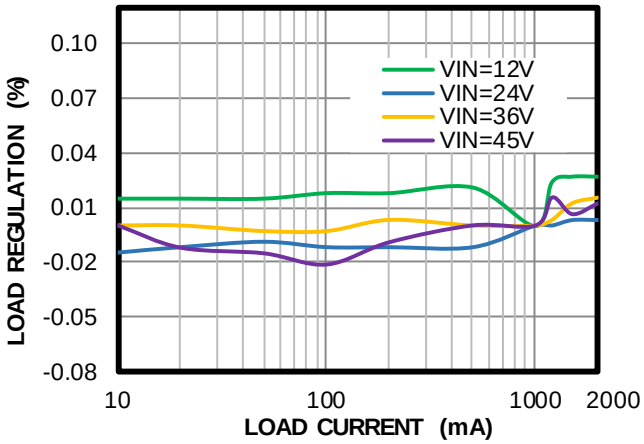
Load Regulation

AAM mode, V_{OUT} = 3.3V



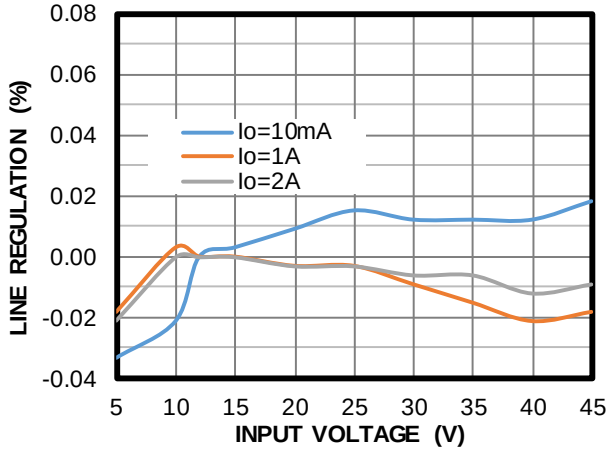
Load Regulation

FCCM, V_{OUT} = 3.3V



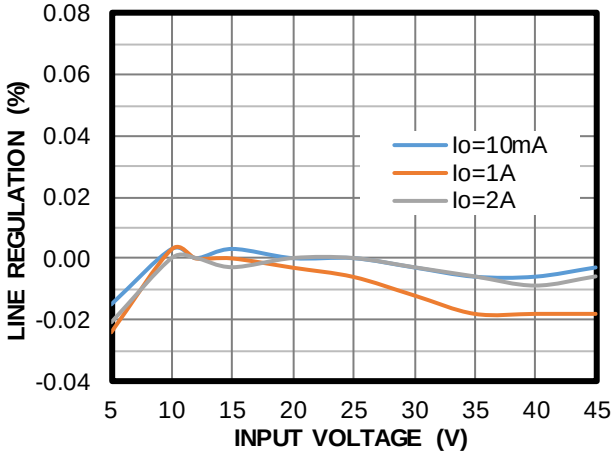
Line Regulation

AAM mode, V_{OUT} = 3.3V



Line Regulation

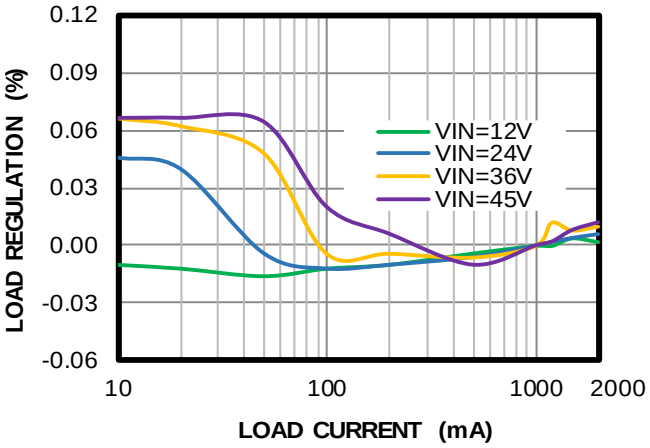
FCCM, V_{OUT} = 3.3V



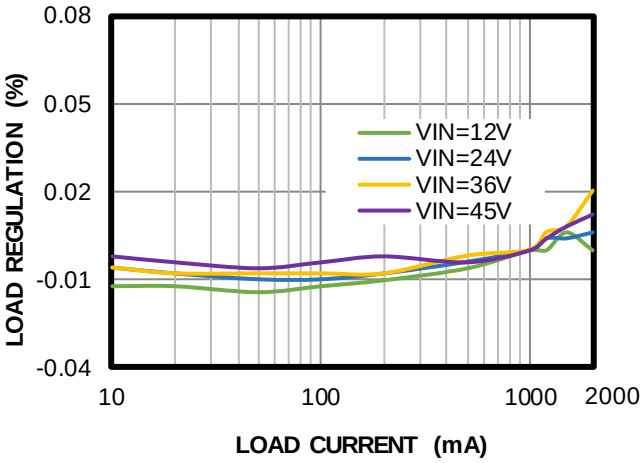
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 5.6µH [7], f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

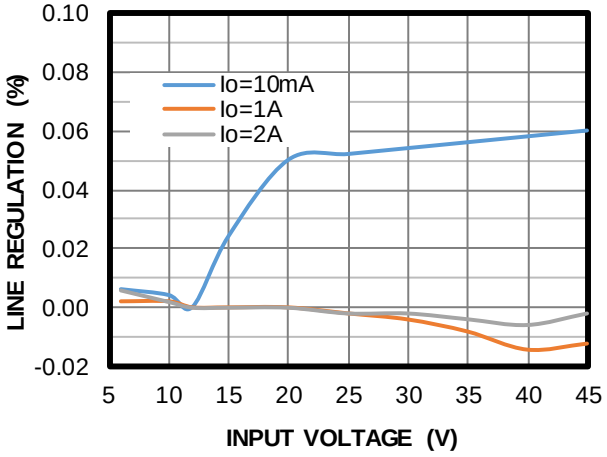
Load Regulation
AAM mode, V_{OUT} = 5V



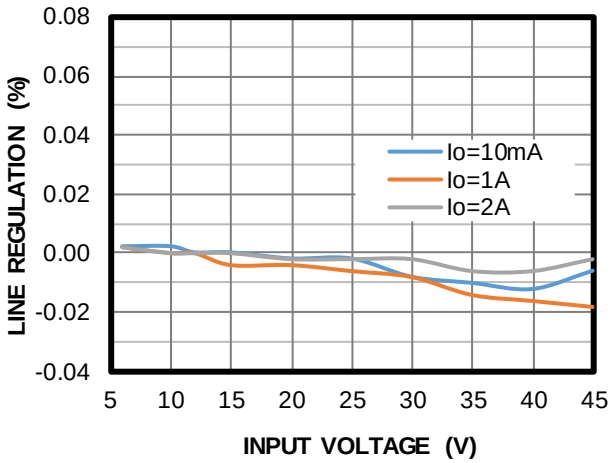
Load Regulation
FCCM, V_{OUT} = 5V



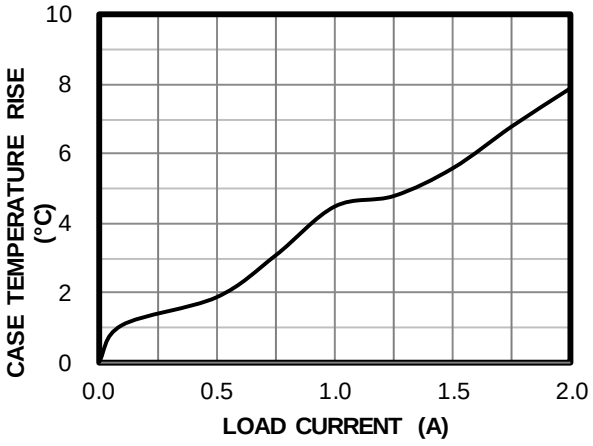
Line Regulation
AAM mode, V_{OUT} = 5V



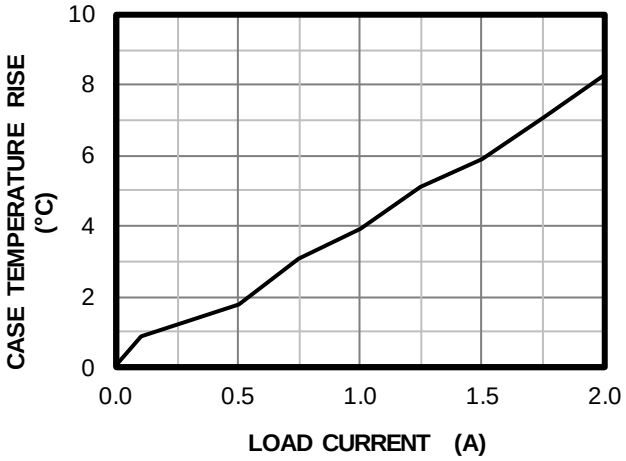
Line Regulation
FCCM, V_{OUT} = 5V



Case Temperature Rise
V_{OUT} = 3.3V



Case Temperature Rise
V_{OUT} = 5V

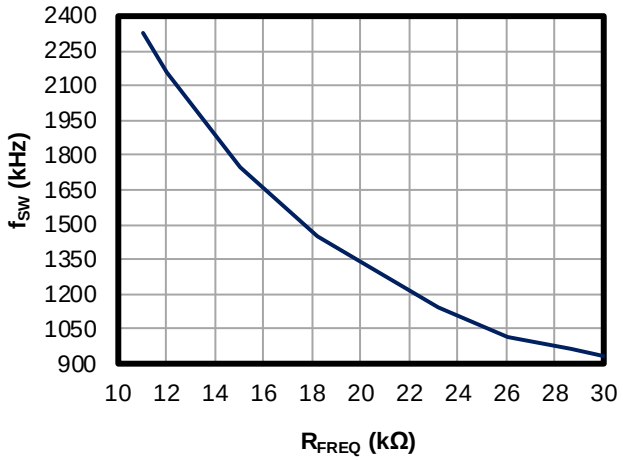


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 5.6µH (7), f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

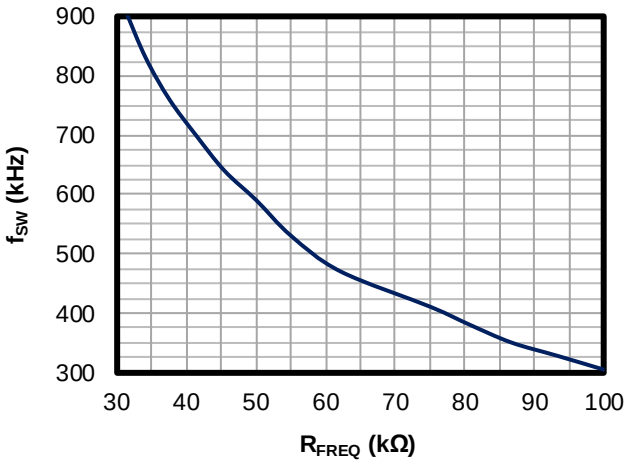
f_{SW} vs. R_{FREQ}

R_{FREQ} = 10kΩ to 30kΩ

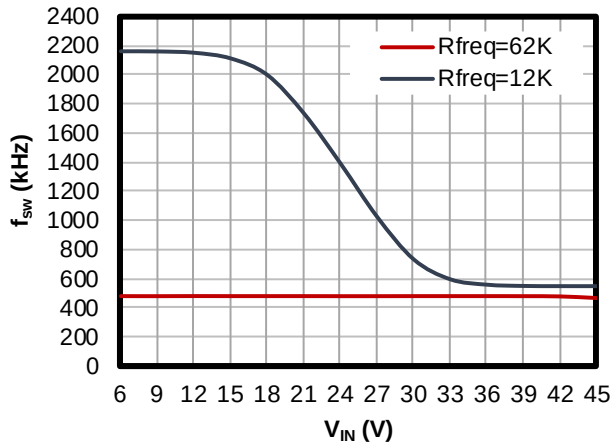


f_{SW} vs. R_{FREQ}

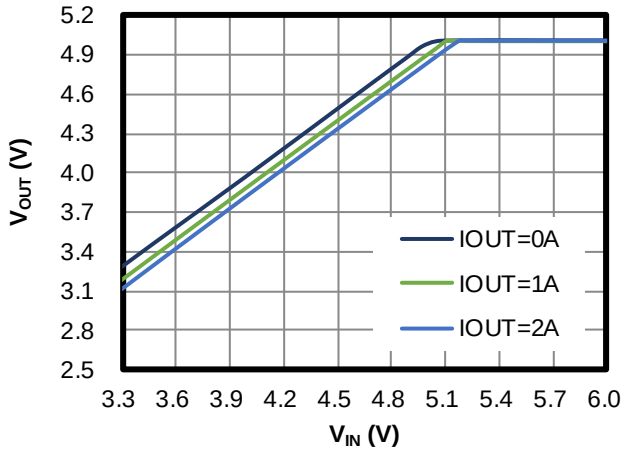
R_{FREQ} = 30kΩ to 100kΩ



f_{SW} vs. V_{IN}



Low-Dropout Mode

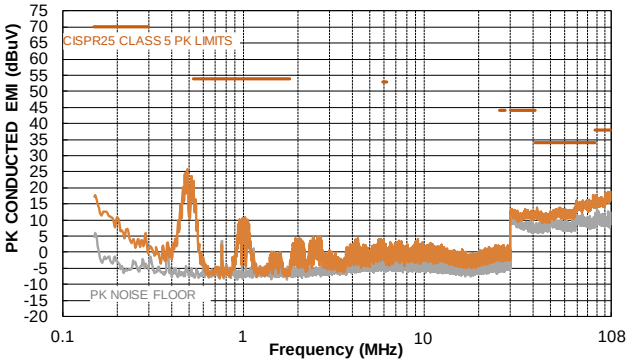


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 2A, L = 5.6µH [7], f_{SW} = 470kHz, T_A = 25°C, unless otherwise noted. [8]

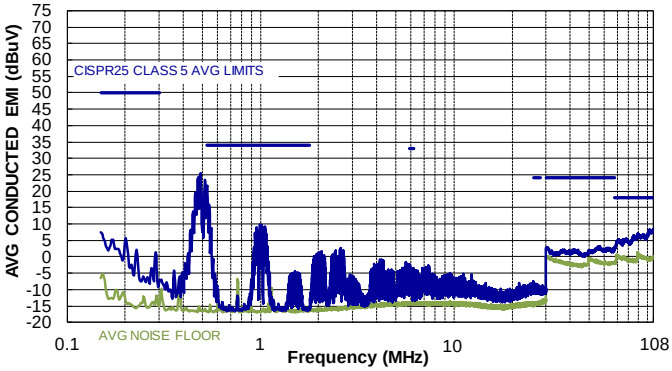
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



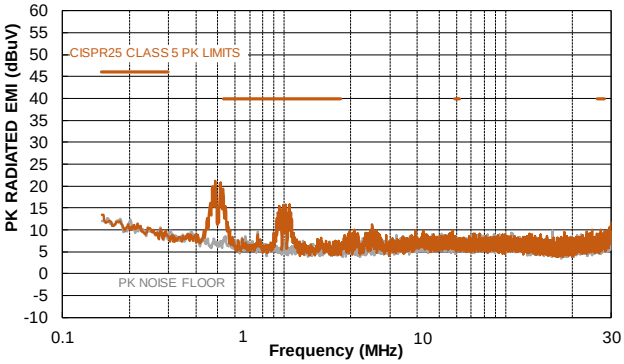
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



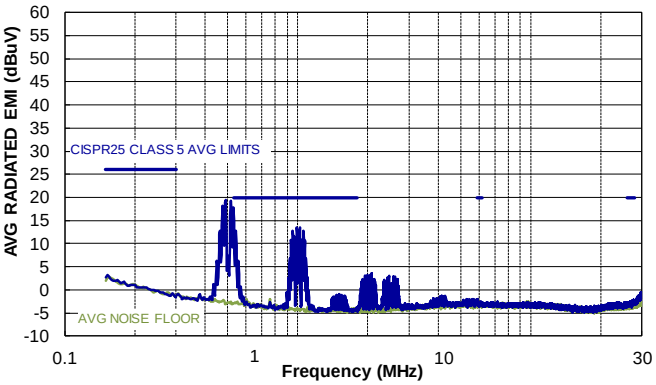
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



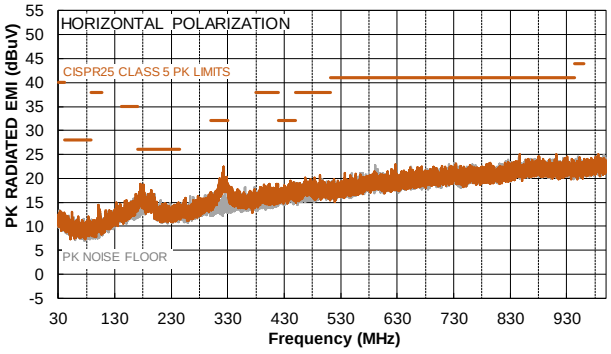
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



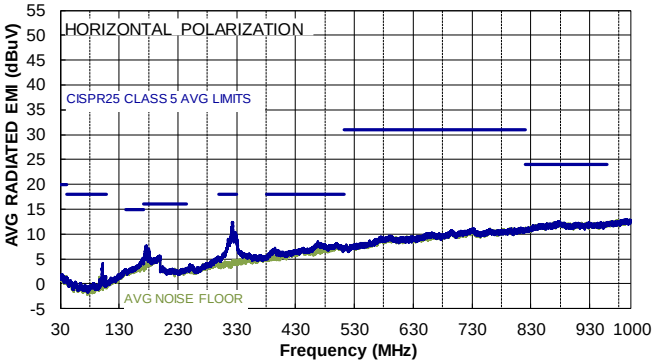
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz

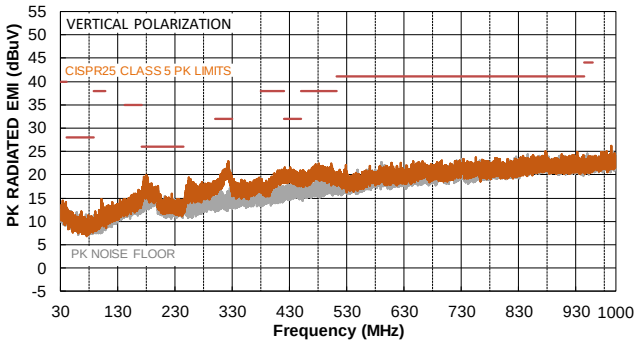


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 2A, L = 5.6µH (7), f_{SW} = 470kHz, T_A = 25°C, unless otherwise noted. (8)

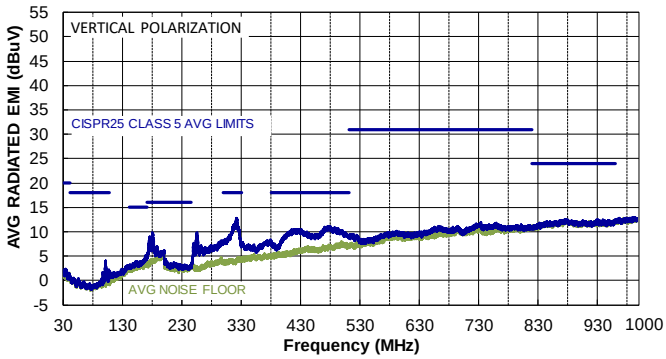
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



Notes:

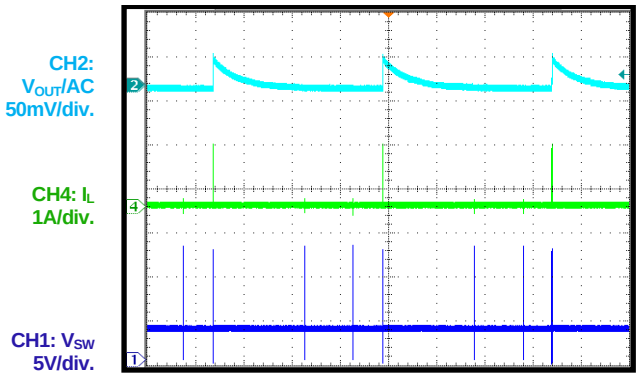
7) Inductor part number: XAL6060-562MEC. DCR = 14.5mΩ.

8) The EMC test results are based on the application circuit with EMI filters (see Figure 11 on page 34).

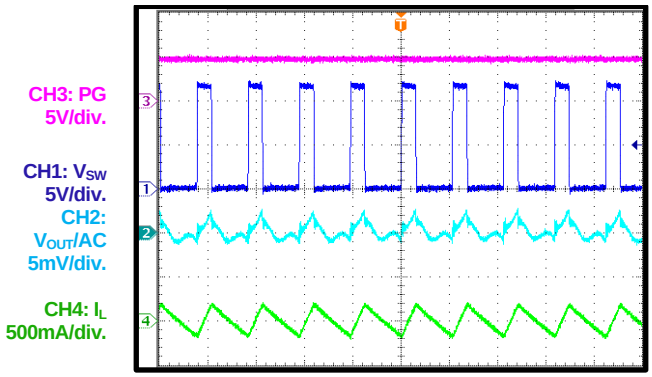
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 5.6µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

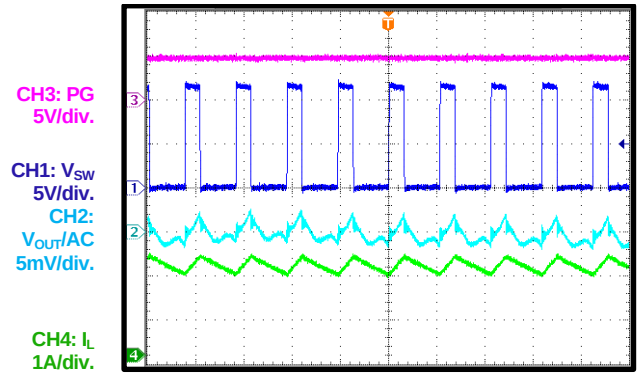
Steady State
I_{OUT} = 0A, AAM mode



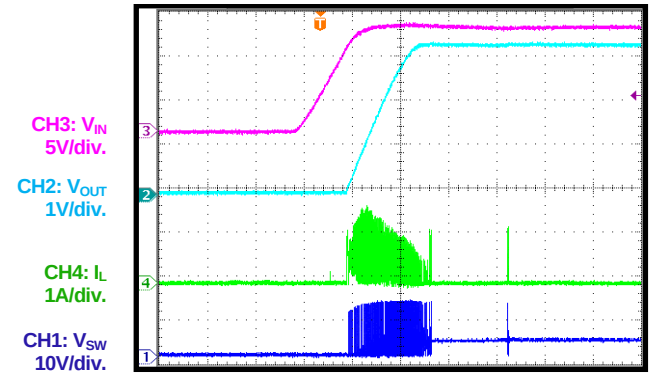
Steady State
I_{OUT} = 0A, FCCM



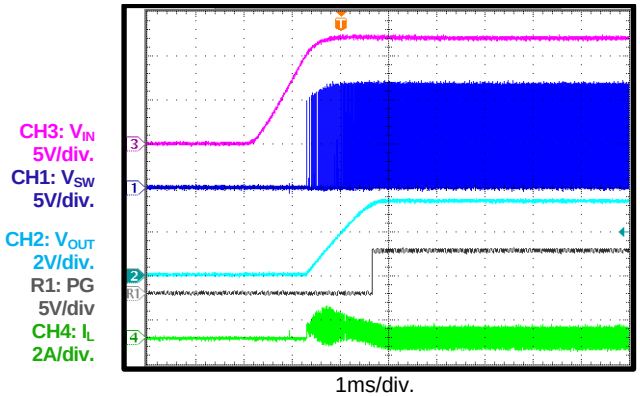
Steady State
I_{OUT} = 2A



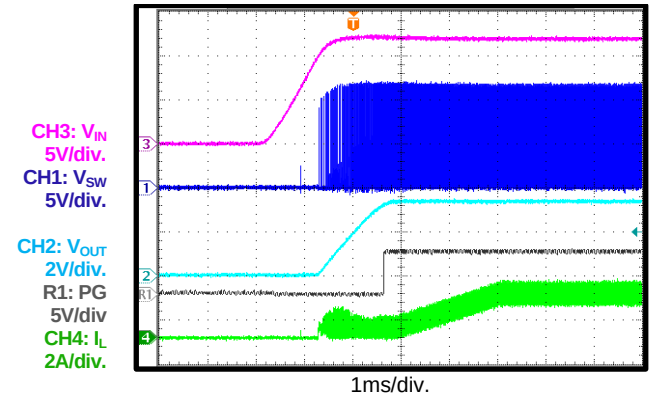
Start-Up through VIN
I_{OUT} = 0A, AAM mode



Start-Up through VIN
I_{OUT} = 0A, FCCM



Start-Up through VIN
I_{OUT} = 2A

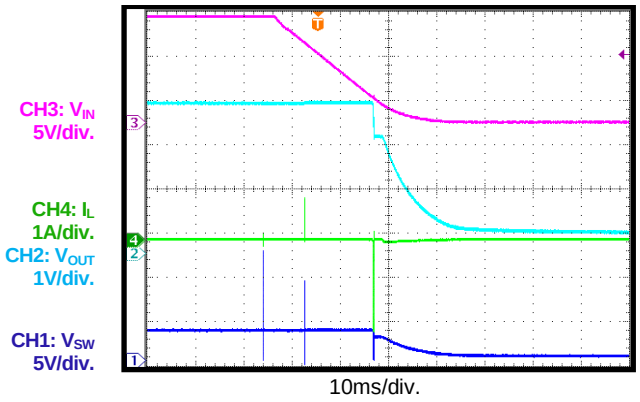


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 5.6µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

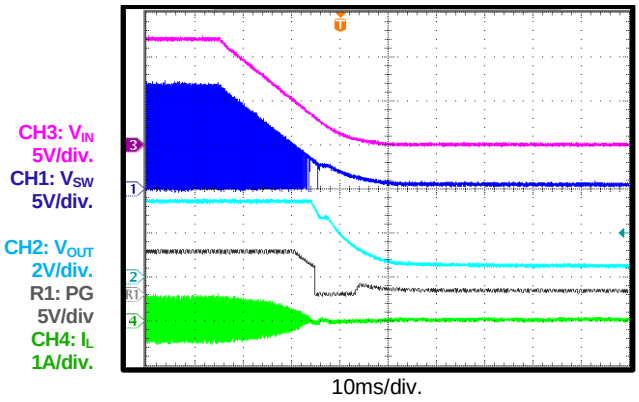
Shutdown through VIN

I_{OUT} = 0A, AAM mode



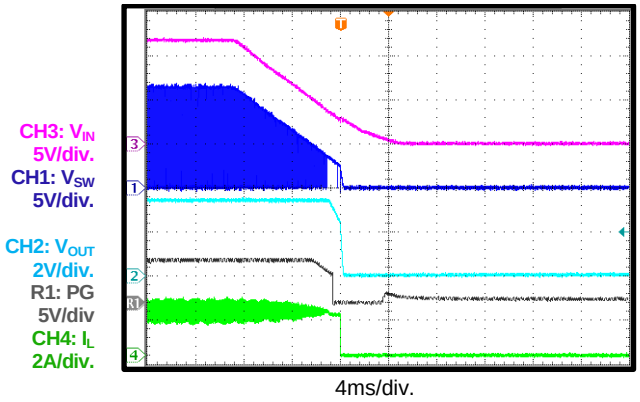
Shutdown through VIN

I_{OUT} = 0A, FCCM



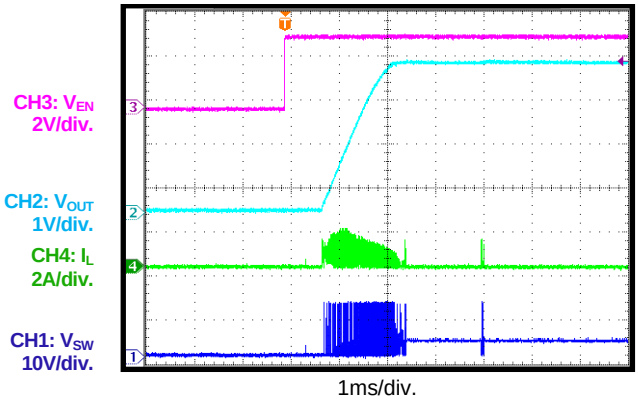
Shutdown through VIN

I_{OUT} = 2A



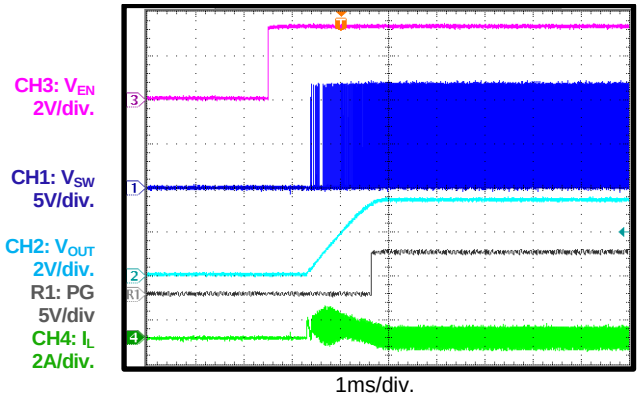
Start-Up through EN

I_{OUT} = 0A, AAM mode



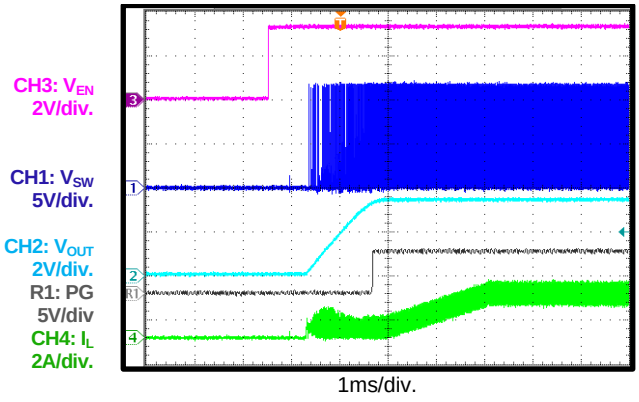
Start-Up through EN

I_{OUT} = 0A, FCCM



Start-Up through EN

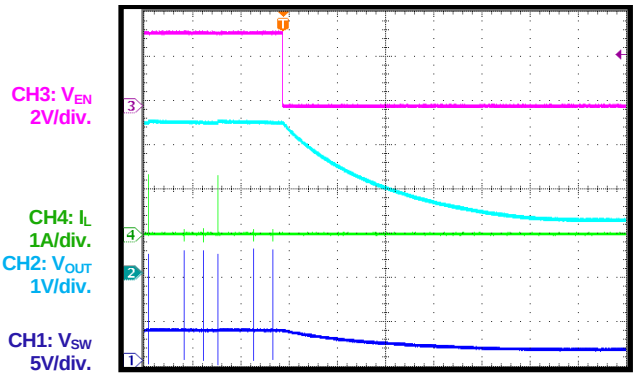
I_{OUT} = 2A



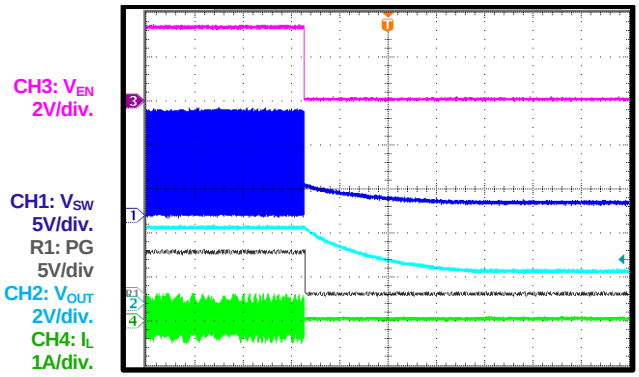
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 5.6µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

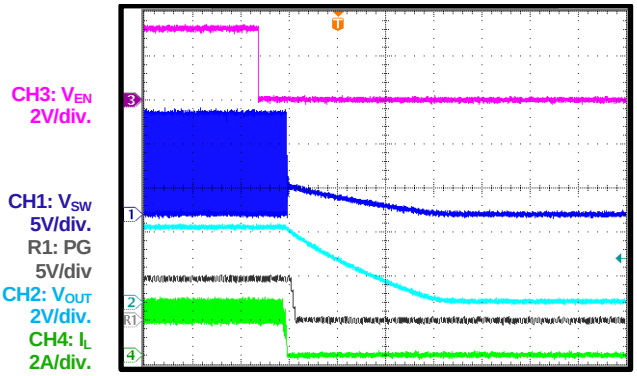
Shutdown through EN
I_{OUT} = 0A, AAM mode



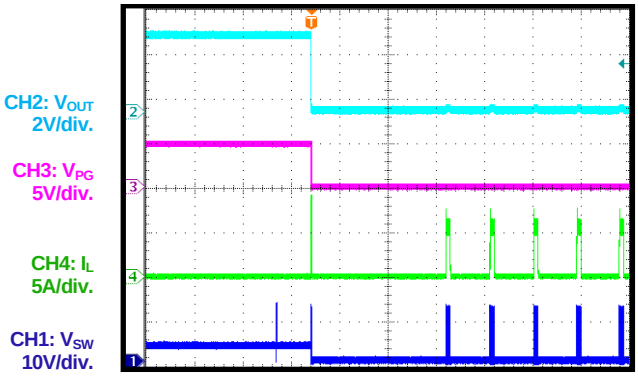
Shutdown through EN
I_{OUT} = 0A, FCCM



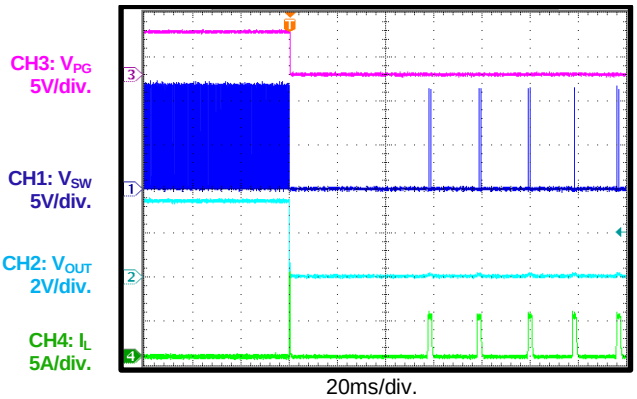
Shutdown through EN
I_{OUT} = 2A



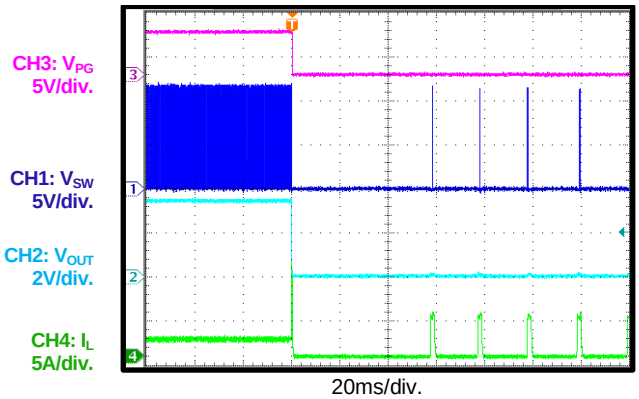
SCP Entry
I_{OUT} = 0A, AAM mode



SCP Entry
I_{OUT} = 0A, FCCM



SCP Entry
I_{OUT} = 2A

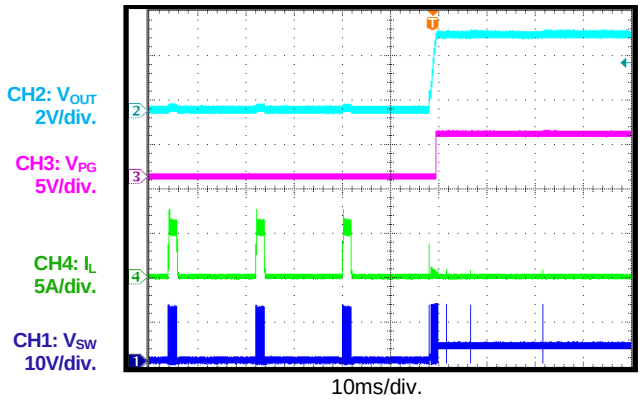


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 5.6µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

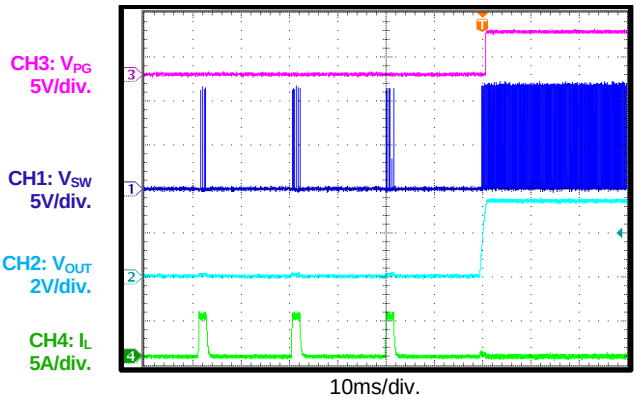
SCP Recovery

I_{OUT} = 0A, AAM mode



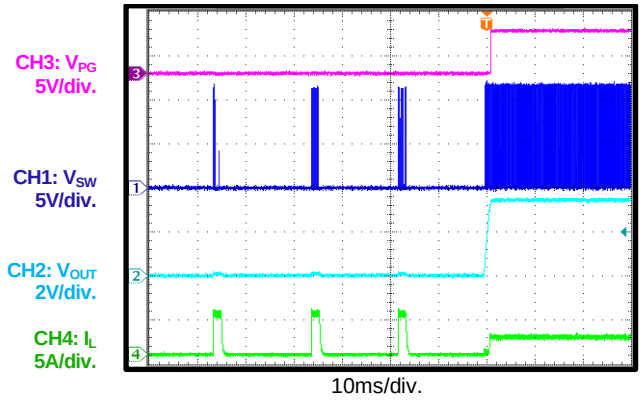
SCP Recovery

I_{OUT} = 0A, FCCM

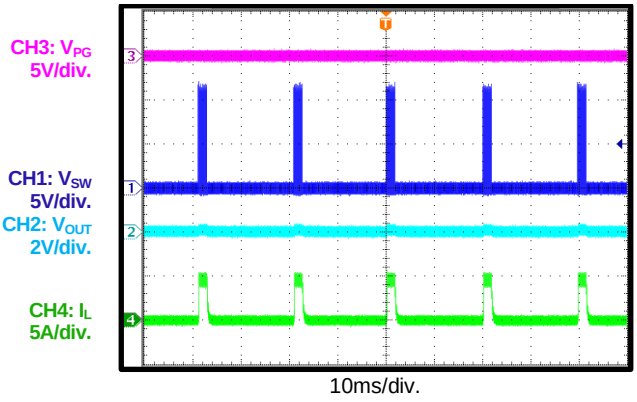


SCP Recovery

I_{OUT} = 2A

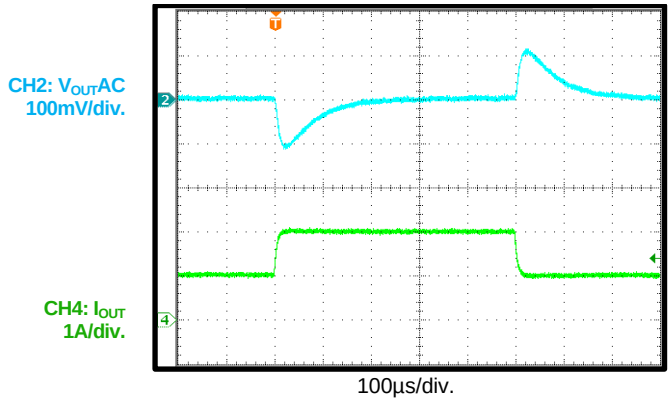


SCP Steady State



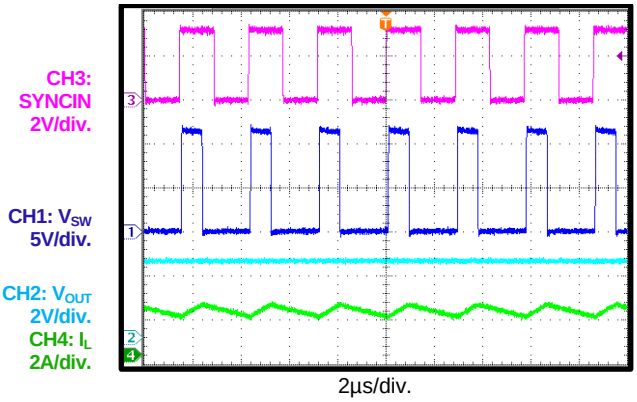
Load Transient

I_{OUT} = 1A to 2A, 1.6A/µs



SYNC Operation

I_{OUT} = 2A, f_{SYNC} = 350kHz

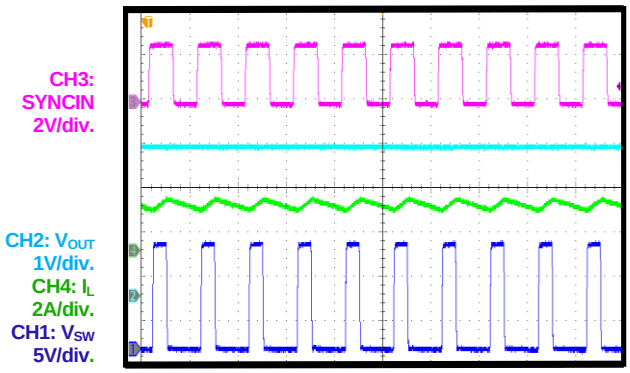


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 5.6µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

SYNC Operation

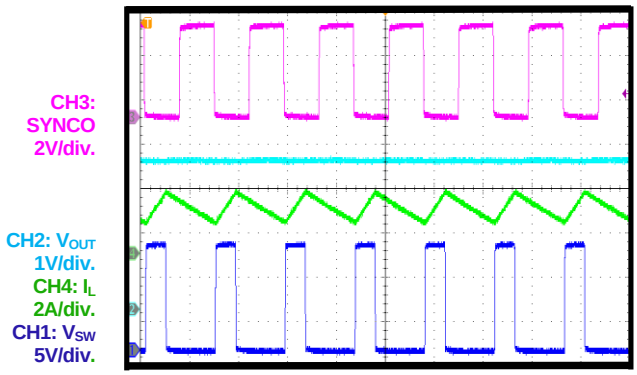
I_{OUT} = 2A, f_{SYNC} = 1000kHz



1µs/div.

SYNCO Operation

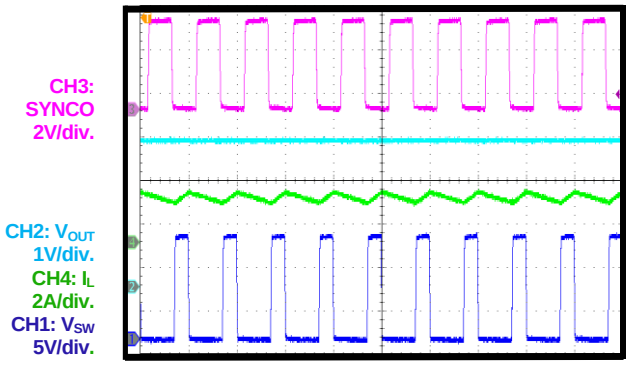
I_{OUT} = 2A, f_{SYNC} = 350kHz



2µs/div.

SYNCO Operation

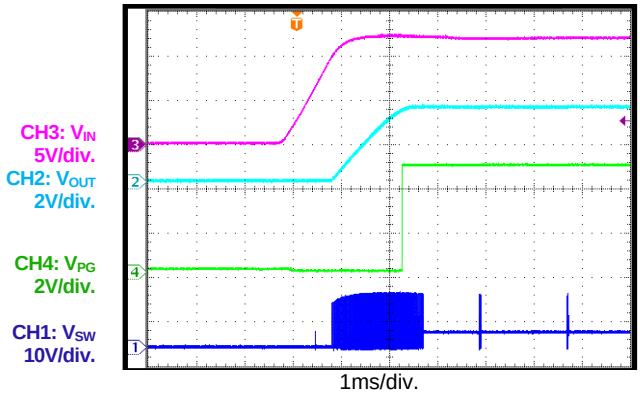
I_{OUT} = 2A, f_{SYNC} = 1000kHz



1µs/div.

PG in Start-Up through VIN

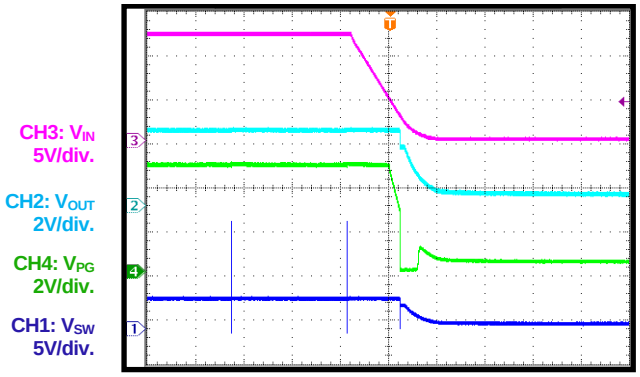
I_{OUT} = 0A, AAM mode



1ms/div.

PG in Shutdown through VIN

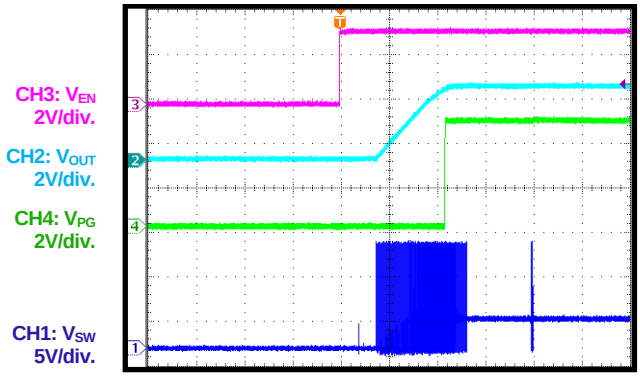
I_{OUT} = 0A, AAM mode



20ms/div.

PG in Start-Up through EN

I_{OUT} = 0A, AAM mode



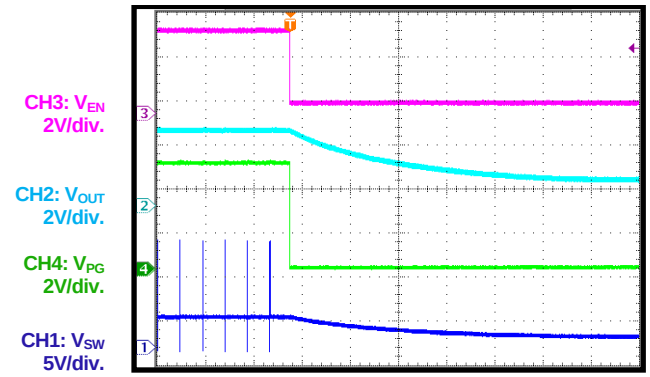
1ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 5.6µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

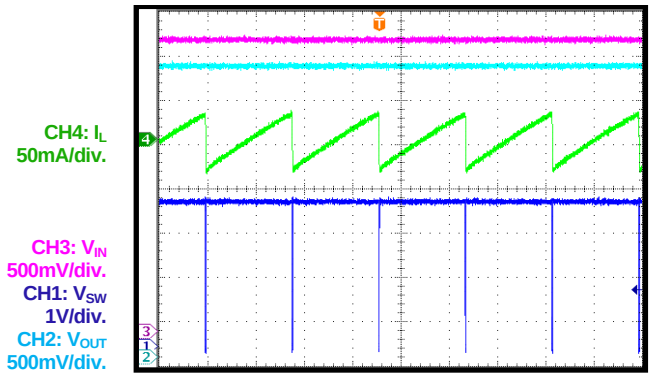
PG in Shutdown through EN

I_{OUT} = 0A, AAM mode



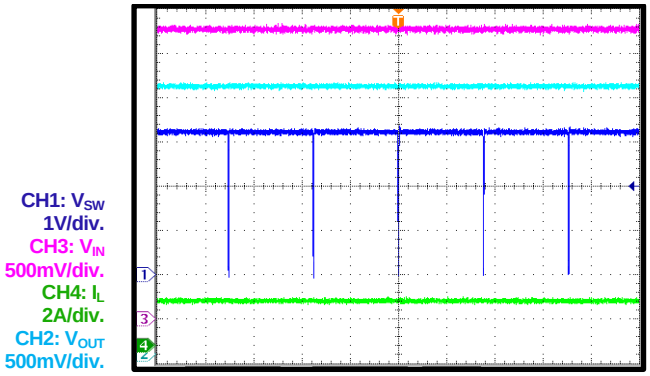
Low-Dropout Mode

V_{IN} = 3.3V, V_{OUT} set to 3.3V, I_{OUT} = 0A



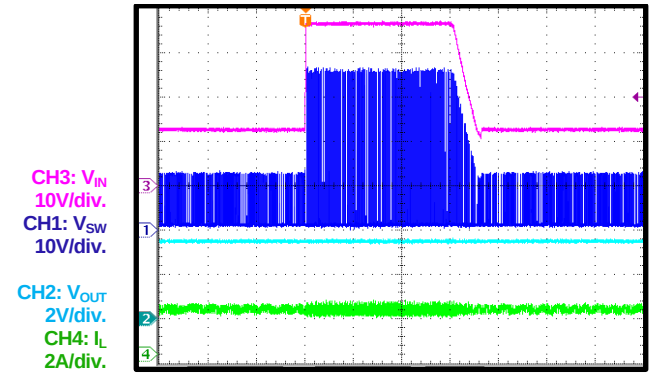
Low-Dropout Mode

V_{IN} = 3.3V, V_{OUT} set to 3.3V, I_{OUT} = 2A



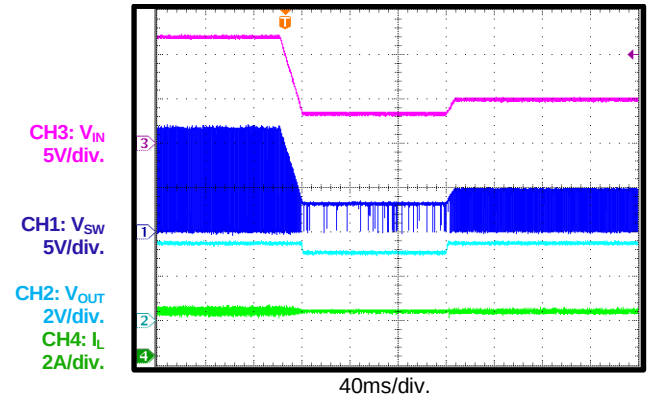
Load Dump

V_{IN} = 12V to 36V, I_{OUT} = 2A



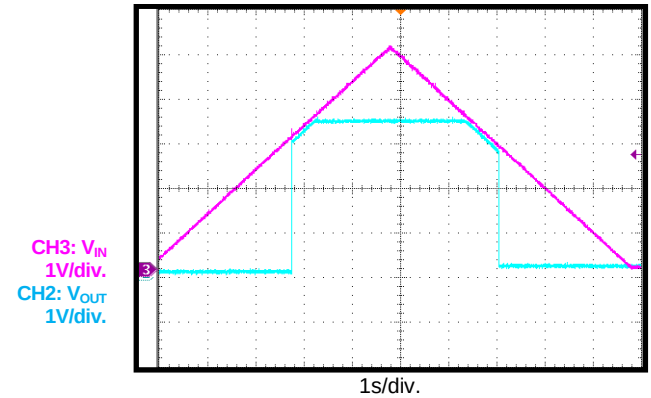
Cold Crank

V_{IN} = 12V to 3.3V to 5V, I_{OUT} = 2A



V_{IN} Ramping Up and Down

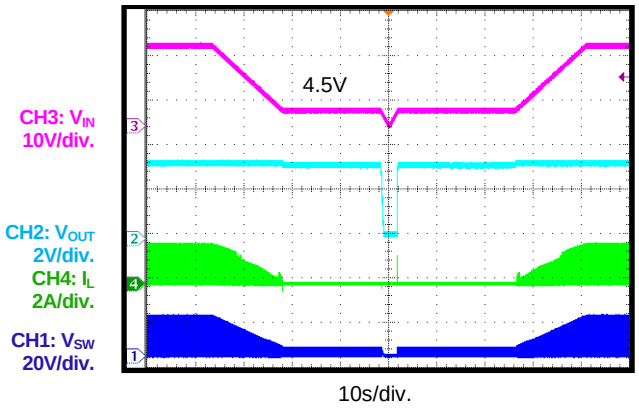
I_{OUT} = 0.1A



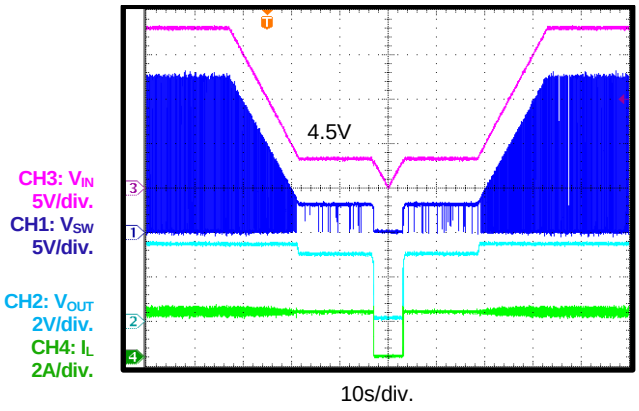
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 5.6µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

V_{IN} Ramping Down and Up
I_{OUT} = 1mA



V_{IN} Ramping Down and Up
I_{OUT} = 2A



FUNCTIONAL BLOCK DIAGRAM

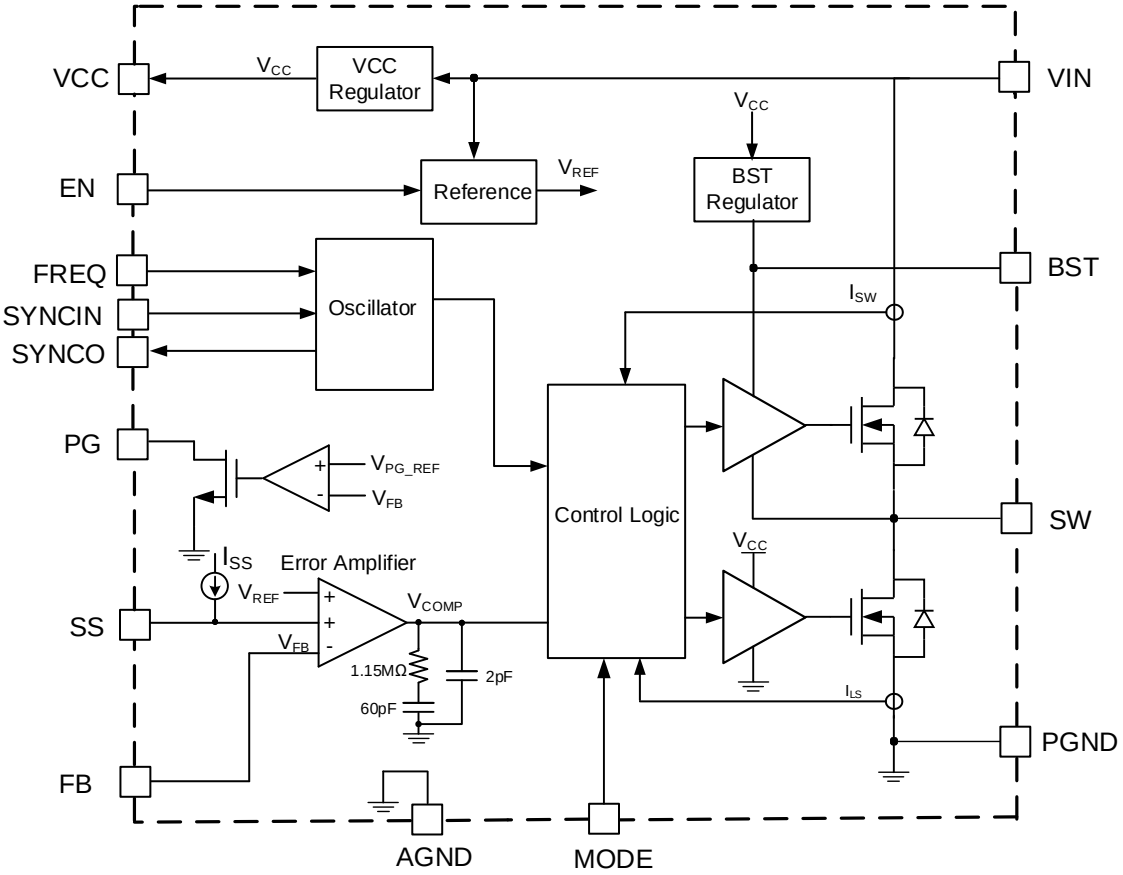


Figure 1: Functional Block Diagram

TIMING SEQUENCE

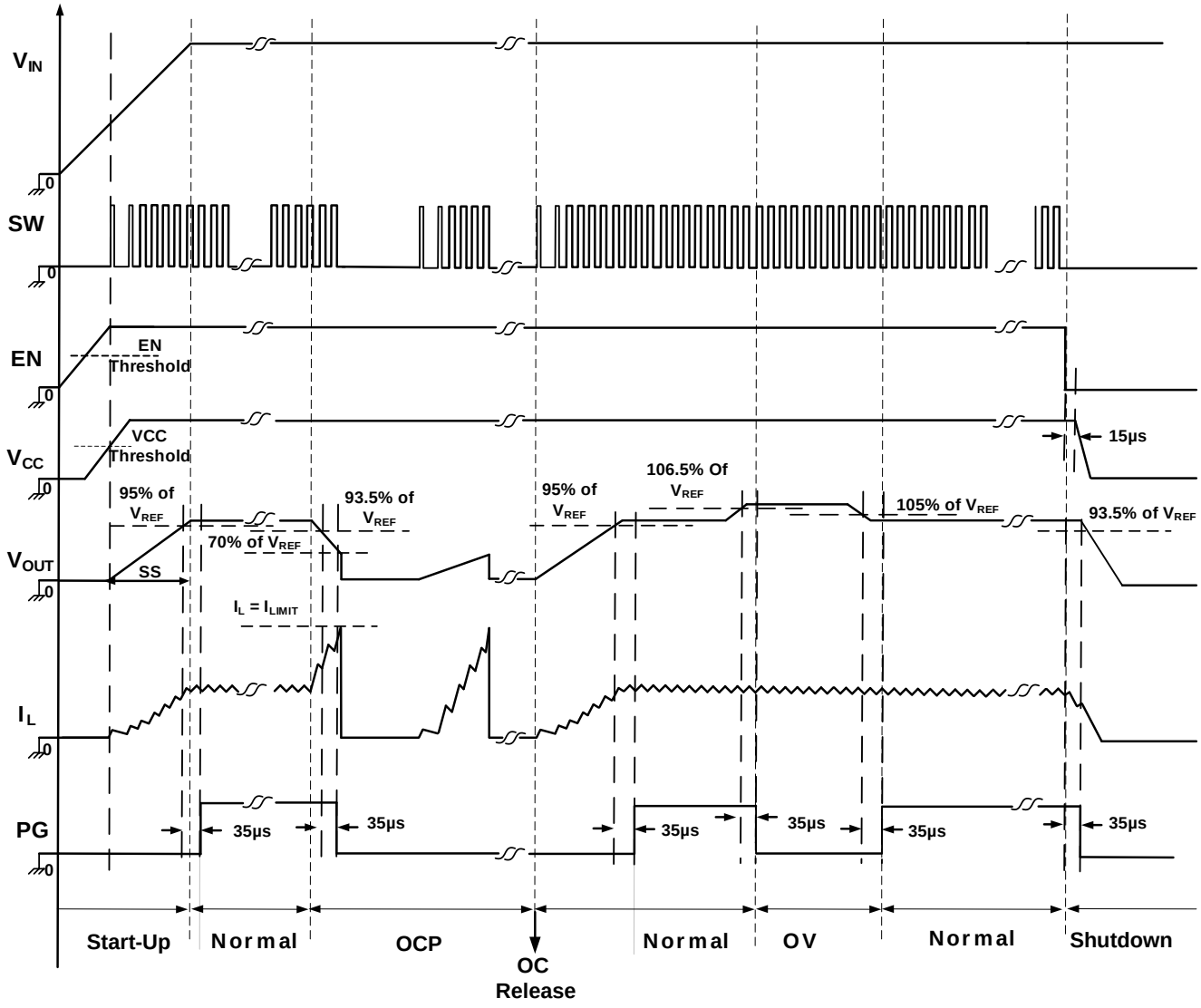


Figure 2: Timing Sequence

OPERATION

The MPQ4312 is a synchronous, step-down switching converter with integrated internal high-side and low-side power MOSFETs (HS-FET and LS-FET, respectively). The device provides 2A of highly efficient output current (I_{OUT}) with current mode control.

The MPQ4312 features a wide input voltage (V_{IN}) range, configurable switching frequency (f_{SW}), external soft start (SS), and a precise current limit. The device's low operational quiescent current (I_Q) makes it well-suited for battery-powered applications.

PWM Control

At moderate to high output currents, the MPQ4312 operates with fixed-frequency, peak current control to regulate the output voltage (V_{OUT}). A PWM cycle is initiated by the internal clock. At the rising edge of the clock, the HS-FET turns on. The HS-FET remains on for at least 100ns, until its current reaches the value set by the internal COMP voltage (V_{COMP}).

When the HS-FET is off, the LS-FET immediately turns on, and remains on until the next cycle starts. The LS-FET remains on for at least 80ns before the next cycle starts.

If the current in the HS-FET does not reach the value set by COMP within one PWM period, then the HS-FET remains on, which saves a turn-off operation. The HS-FET is forced off after about 10µs, even if it does not reach the value set by COMP.

Light-Load Operation

Under light-load conditions, the MPQ4312 can work in two different operation modes based on the MODE pin.

The MPQ4312 works in forced continuous conduction mode (FCCM) when the MODE pin is pulled above 1.8V. In FCCM, the device works with a fixed frequency from no-load to full-load conditions. The advantage of FCCM is its controllable frequency and lower output ripple under light loads.

The chip works in advanced asynchronous modulation (AAM) mode when the MODE pin is pulled below 0.4V. AAM mode optimizes efficiency under light-load and no-load conditions.

When AAM mode is enabled, the MPQ4312 enters asynchronous operation while the inductor current (I_L) approaches 0A under light loads (see Figure 3). If the load is further decreased or there is no load, V_{COMP} drops to the set value, and the MPQ4312 enters AAM mode.

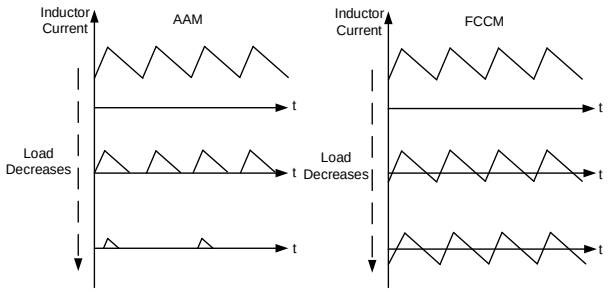


Figure 3: AAM and FCCM

In AAM mode, the internal clock resets when V_{COMP} crosses the set value. The crossover time is used as the benchmark for the next clock. When the load increases and V_{COMP} exceeds the set value, the device operates in discontinuous conduction mode (DCM) or CCM, both of which have a constant f_{SW}.

Error Amplifier (EA)

The error amplifier (EA) compares the FB pin voltage (V_{FB}) to the internal reference voltage (V_{REF}, typically 0.815V), and outputs a current proportional to the difference between the two voltages. I_{OUT} charges the compensation network to form V_{COMP}, which controls the MOSFET current.

During normal operation, the minimum V_{COMP} is clamped to 0.9V, and its maximum is clamped to 2V. COMP is internally pulled down to GND when the device shuts down.

Internal Regulator VCC

The internal 4.9V regulator (VCC) powers most of the internal circuitry. This regulator uses VIN as the input and operates in the full V_{IN} range. When V_{IN} exceeds 4.9V, VCC is in full regulation. When V_{IN} is below 4.9V, the VCC output degrades.

Bootstrap (BST) Charging

The bootstrap (BST) capacitor (C_{BST}) is charged and regulated to about 5V by the dedicated

internal BST regulator. When the voltage between the BST and SW nodes drops below its regulated value, a P-channel MOSFET pass transistor connected from VCC to BST turns on to charge C_{BST}. The external circuit should provide enough voltage headroom to facilitate charging. When the HS-FET is on, BST exceeds VCC, which means that C_{BST} cannot be charged.

Under higher duty cycles, there is less time for C_{BST} to charge, so it may not be charged sufficiently. If the external circuit has an insufficient voltage (or not enough time) to charge C_{BST}, use additional external circuitry to ensure that the BST voltage (V_{BST}) remains in the normal operation range.

Low-Dropout Mode and BST Refresh

To improve dropout, the MPQ4312 is designed to operate at close to 100% duty cycle when the difference between the voltages on the BST and SW pins exceeds 2.5V. When the voltage from BST to SW drops below 2.5V, the HS-FET turns off using an under-voltage lockout (UVLO) circuit. This allows the LS-FET to conduct and refresh the charge on C_{BST}. In DCM or pulse-skip mode (PSM), the LS-FET is forced on to refresh V_{BST}.

Since the supply current sourced from C_{BST} is low, the HS-FET can remain on for more switching cycles than are required to refresh the capacitor. As a result, the effective duty cycle of the switching regulator is high.

The regulator's effective duty cycle during dropout is mainly influenced by the voltage drops across the power MOSFET, the inductor resistance, the low-side diode, and the PCB resistance.

Enable Control

EN is a digital control pin that turns the MPQ4312 on and off.

Enabled by an External Logic (High/Low) Signal

When EN is pulled below its falling threshold voltage (about 0.85V), the chip operates in the lowest shutdown current mode. Pull EN above its rising threshold voltage (about 1V) to enable the part.

Configurable V_{IN} Under-Voltage Lockout (UVLO)

When V_{IN} is sufficiently high, the chip can be enabled and disabled via the EN pin. With an internal current source, the circuit can generate a configurable V_{IN} UVLO threshold and hysteresis. Use resistor dividers to set the EN voltage (see Figure 4).

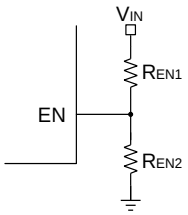


Figure 4: Enable Divider Circuit

Configurable Frequency and Foldback

The MPQ4312's oscillating frequency can be configured via an external resistor (R_{FREQ}) connected from the FREQ pin to ground, or by a logic level SYNC signal.

To set f_{SW}, select R_{FREQ} using the f_{SW} vs. R_{FREQ} curve on page 15. When f_{SW} is set high, it may fold back at high input voltages to avoid triggering a minimum on time and forcing the output out of regulation.

In car-battery applications, f_{SW} is between 350kHz and 1000kHz. Table 1 lists the recommended R_{FREQ} values for common frequencies. Higher frequencies can be used in applications that do not have a critical f_{SW} limit, as well as applications with a low and stable V_{IN}.

Table 1: R_{FREQ} vs. f_{SW}

R_{FREQ} (kΩ)	f_{SW} (kHz)
86.6	350
80.6	380
75	410
62	470
59	500
54.9	530
49.9	590
45.3	640
41.2	700
37.4	760
34	830
30.9	910
28.7	960
26.1	1000

Frequency Spread Spectrum

The MPQ4312 uses a 12kHz modulation frequency with a fixed 128-step triangular profile to spread the internal oscillator frequency across a 20% (±10%) window (see Figure 5). The steps are fixed and independent of the set oscillator frequency, which optimizes frequency spread spectrum (FSS) performance.

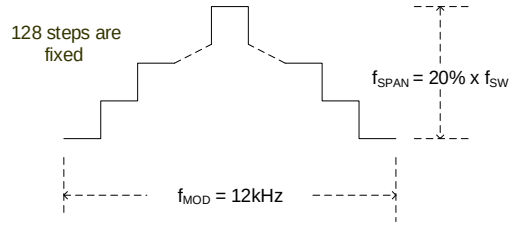


Figure 5: Frequency Spread Spectrum Scheme

Side bands are created by modulating f_{SW} with a triangle modulation waveform. This reduces the emission power of the fundamental f_{SW}, as well as its harmonics, which then reduces peak electromagnetic interference (EMI) noise.

Soft Start (SS)

Soft start (SS) is implemented to prevent the converter's V_{OUT} from overshooting during start-up.

When SS begins, an internal current source begins charging the external soft-start capacitor (C_{SS}). When the soft-start voltage (V_{SS}) is below the internal V_{REF}, V_{SS} overrides V_{REF} and the EA uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the EA uses V_{REF} as the reference.

C_{SS} can be calculated with Equation (1):

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} = 13.5 \times t_{SS}(ms) \quad (1)$$

The SS pins can be used for tracking and sequencing.

Pre-Biased Start-Up

If V_{FB} exceeds V_{SS} - 150mV during start-up, this means that the output has a pre-biased voltage. In the scenario, the HS-FET and LS-FET do not turn on until V_{SS} exceeds V_{FB}.

Thermal Shutdown

Thermal shutdown is implemented to protect the chip from thermal runaway. If the silicon die temperature exceeds its upper threshold (typically 170°C), the device shuts down the power MOSFETs. When the temperature falls below the lower threshold (150°C), the chip starts up again and resumes normal operation.

Current Comparator and Current Limit

The power MOSFET current is accurately sensed via a current-sense MOSFET. This current is then fed to the high-speed current comparator for current mode control. The current comparator uses this sensed current as one of its inputs.

When the HS-FET turns on, the comparator is blanked until the end of the turn-on transition to mitigate noise. The comparator compares the MOSFET current to the value set by V_{COMP}. When the sensed current exceeds the value set by COMP, the comparator outputs low to turn off the HS-FET. The MOSFET's maximum current is internally limited cycle by cycle.

Hiccup Protection

If the output is shorted to ground, V_{OUT} may drop below 70% of its nominal output. If this occurs, the MPQ4312 shuts down momentarily and begins discharging C_{SS}. The device restarts with a full soft start once C_{SS} is fully discharged. This process is repeated until the fault condition is removed.

Start-Up and Shutdown

If both V_{IN} and EN exceed their respective thresholds, the chip starts. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

While the internal supply rail is up, an internal timer holds the power MOSFET off for about 50µs to blank the start-up glitches. When the soft-start block is enabled, the SS output remains low to ensure that the remaining circuitries are ready before slowly ramping up.

Three events can shut down the chip: EN going low, V_{IN} going low, and thermal shutdown. When shutdown is initiated, the signaling path is first blocked to avoid any fault triggering. Next, V_{COMP} and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

Power Good (PG) Output

The MPQ4312 includes an open-drain power good (PG) output. If this function is used, a pull-up resistor to power source is required. If V_{OUT} is within 95% to 105% of the nominal voltage, then the PG pin goes high. If V_{OUT} is above 106.5% or below 93.5% of the nominal voltage, then PG goes low

SYNCIN and SYNCO

f_{SW} can be synchronized to the rising edge of the clock signal applied at SYNCIN. The recommended SYNCIN frequency range is 350kHz to 1000kHz. Ensure that SYNCIN's off time is shorter than the internal oscillator period. Otherwise, the internal clock may turn on the HS-FET before the rising edge of SYNCIN.

There is no limit for the SYNCIN pulse width, but there is always parasitic capacitance on the pad. If the pulse width is too short, a clear rising and falling edge may not be seen due to the parasitic capacitance. It is recommended to make the pulse longer than 100ns.

When using SYNCIN in AAM mode, drive SYNCIN below its specified threshold (about 0.4V), or float the SYNCIN pin before starting up the MPQ4312. Then add the external SYNCIN clock. If using this function, connect a resistor (10kΩ to 51kΩ) from SYNCIN to GND and do not float SYNCIN.

The SYNCO pin provides a default 180° phase-shifted clock for the internal oscillator. If there is no external SYNCIN clock, SYNCO can provide a clock that is phase-shifted 180° compared to the internal clock.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider connected to FB sets V_{OUT} (see Figure 6).

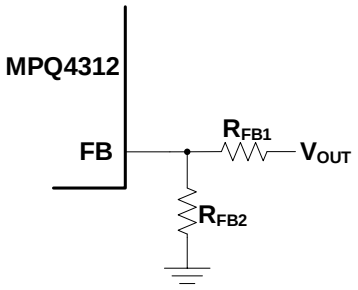


Figure 6: Feedback Network

Calculate R_{FB2} with Equation (2):

$$R_{FB2} = \frac{R_{FB1}}{\frac{V_{OUT}}{0.815V} - 1} \quad (2)$$

Table 2 lists the recommended feedback resistor values for common output voltages.

Table 2: Resistor Selection for Output Voltages

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)
3.3	100 (1%)	32.4 (1%)
5	100 (1%)	19.6 (1%)

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their low ESR and small temperature coefficients.

For most applications, a 4.7µF to 10µF capacitor is sufficient. It is strongly recommended to use another, lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and GND as possible.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating.

The RMS current in the input capacitor (I_{CIN}) can be estimated with Equation (3):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (3)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (4):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, place a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the device as possible.

When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent an excessive voltage ripple at the input. The input voltage ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep the output voltage ripple low. The output voltage ripple (ΔV_{OUT}) can be calculated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (6)$$

Where L is the inductance, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple.

For simplification, the output voltage ripple (ΔV_{OUT}) can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output voltage ripple (ΔV_{OUT}) can be calculated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (8)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ4312 can be optimized for a wide range of capacitance and ESR values.

Selecting the Inductor

A 1µH to 10µH inductor with a DC current rating at least 25% greater than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage; however, it also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance is to allow the inductor ripple current to be approximately 30% of the maximum load current. The inductance (L) can then be calculated with Equation (9):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current (I_{LP}) can be calculated with Equation (10):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

V_{IN} Under-Voltage Lockout (UVLO) Setting

The MPQ4312 has an internal, fixed under-voltage lockout (UVLO) threshold. The rising threshold is 3V, and the falling threshold is about 2.7V. For the applications that require a higher UVLO point, an external resistor divider between VIN and EN can be used to achieve a higher equivalent UVLO threshold (see Figure 7).

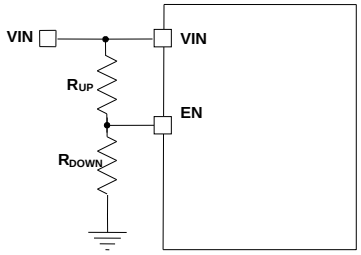


Figure 7: Adjustable UVLO Using EN Divider

The UVLO rising and falling thresholds can be calculated with Equation (11) and Equation (12), respectively:

$$V_{IN\_UVLO\_RISING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN\_RISING} \quad (11)$$

$$V_{IN\_UVLO\_FALLING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN\_FALLING} \quad (12)$$

Where V_{EN_RISING} is 1V, and $V_{EN\_FALLING}$ is 0.85V.

Selecting the External BST Diode and Resistor

An external BST diode can enhance the regulator's efficiency when the duty cycle is high. A power supply between 2.5V and 5V can be used to power the external bootstrap diode. It is recommended to make V_{CC} or V_{OUT} the power supply in the circuit (see Figure 8).

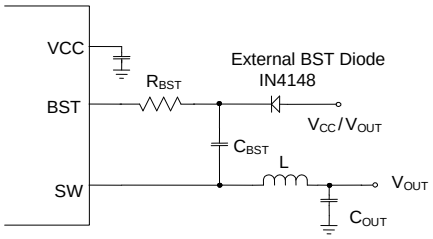


Figure 8: Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the recommended C_{BST} value is between 0.1µF and 1µF. Connect a resistor (R_{BST}) in series with C_{BST} to reduce the SW rising rate and voltage spikes. This improves EMI performance and reduces voltage stress at higher input voltages. A higher resistance reduces SW spikes but compromises efficiency, so an appropriate tradeoff for the application must be made. It is recommended for R_{BST} to be ≤20Ω.

Selecting the VCC Capacitor

The VCC capacitor should be 10 times greater than the boost capacitor. A VCC capacitor above 68µF (nominal) is not recommended.

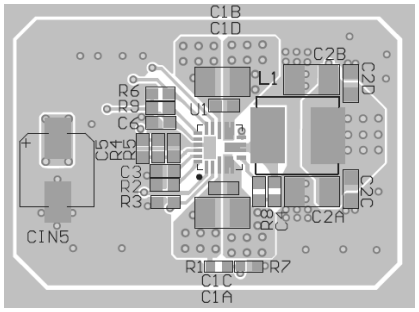
PCB Layout Guidelines [9]

Efficient PCB layout, is critical for stable operation. A 4-layer layout is strongly recommended to achieve better thermal performance. For the best results, refer to Figure 9 and follow the guidelines below:

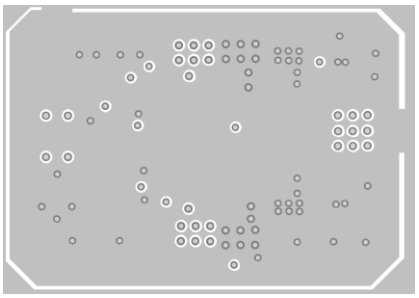
1. Place symmetric input capacitors as close to the VIN and GND pins as possible.
2. Connect a large ground plane directly to PGND.
3. Add vias near PGND if the bottom layer is a ground plane.
4. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
5. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high-frequency noise.
6. Keep the connection of the input capacitor and VIN as short and wide as possible.
7. Place the VCC capacitor as close to the VCC and GND pins as possible.
8. Route SW and BST away from sensitive analog areas, such as FB.
9. Place the feedback resistors close to the chip to ensure that the trace that connects to FB is as short as possible.
10. Use multiple vias to connect the power planes to the internal layers.

Note:

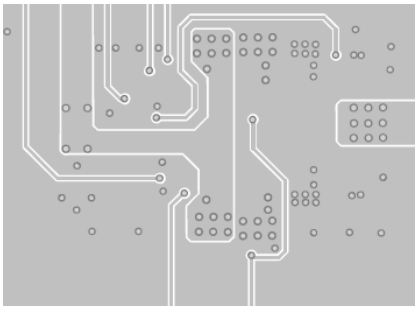
9) The recommended PCB layout is based on Figure 10 on page 34.



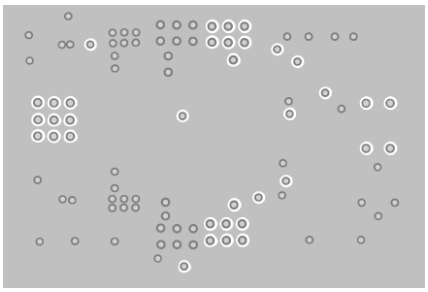
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 9: Recommended PCB Layout

TYPICAL APPLICATION

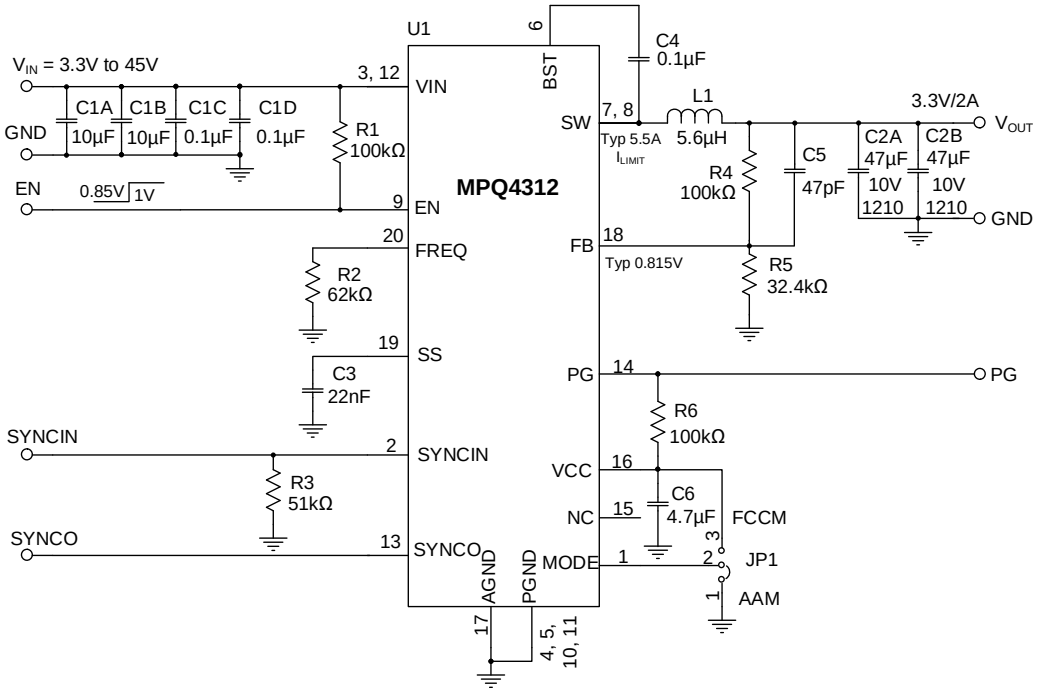


Figure 10: V_{OUT} = 3.3V, f_{SW} = 470kHz

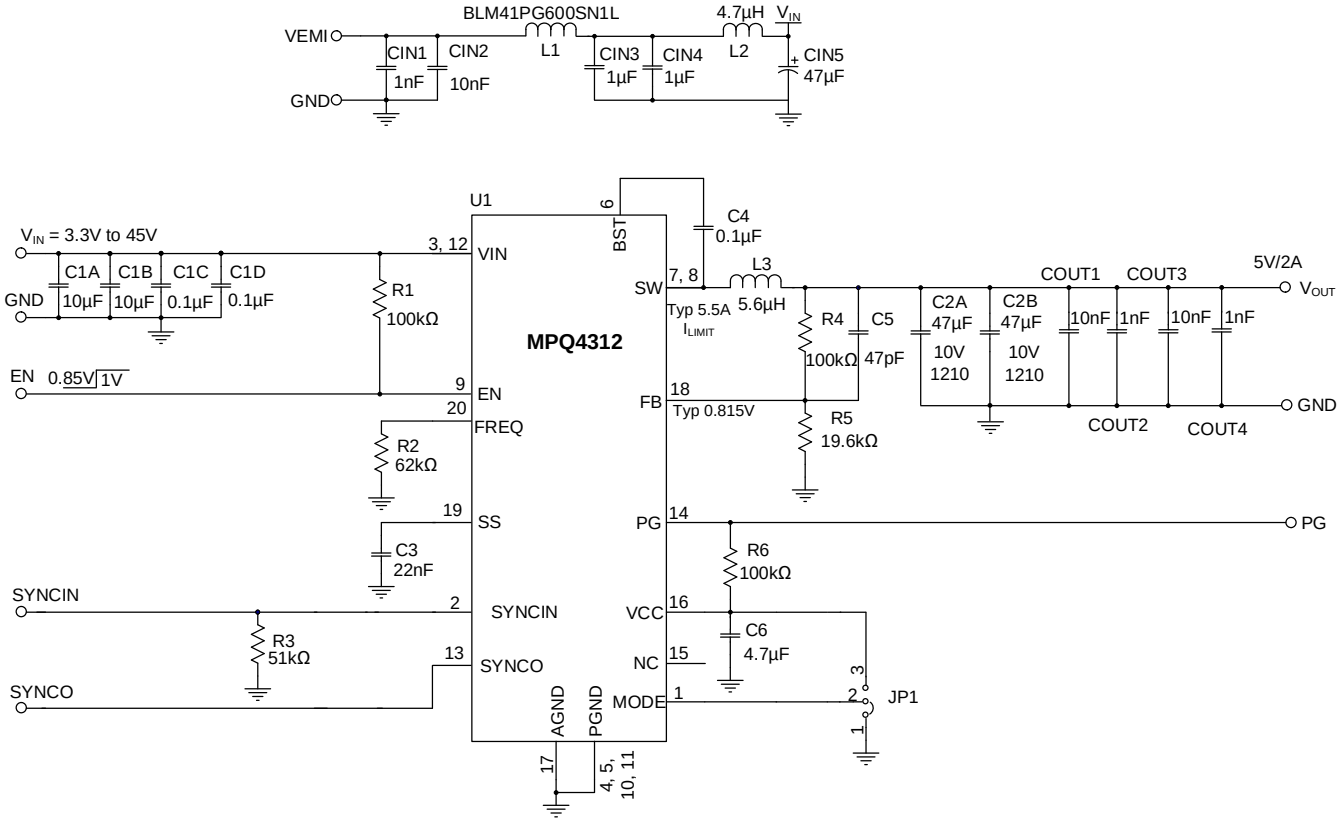
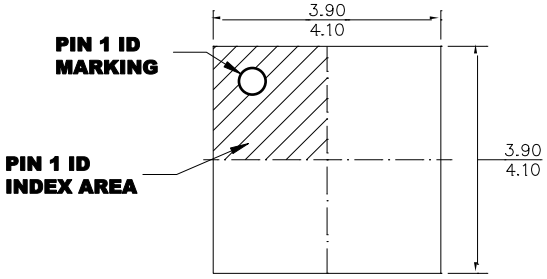


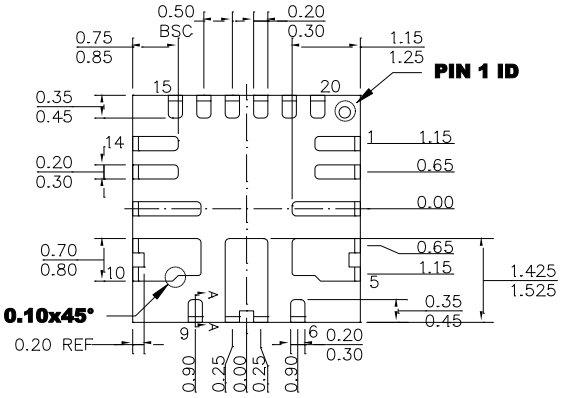
Figure 11: V_{OUT} = 5V, f_{SW} = 470kHz with EMI Filters

PACKAGE INFORMATION

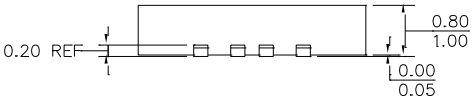
QFN-20 (4mmx4mm)
Wettable Flank



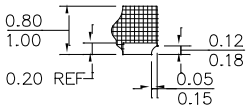
TOP VIEW



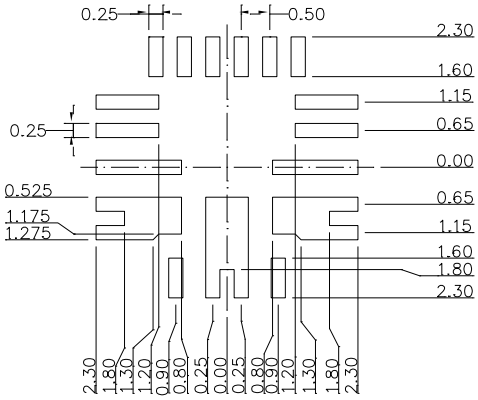
BOTTOM VIEW



SIDE VIEW



SECTION A-A

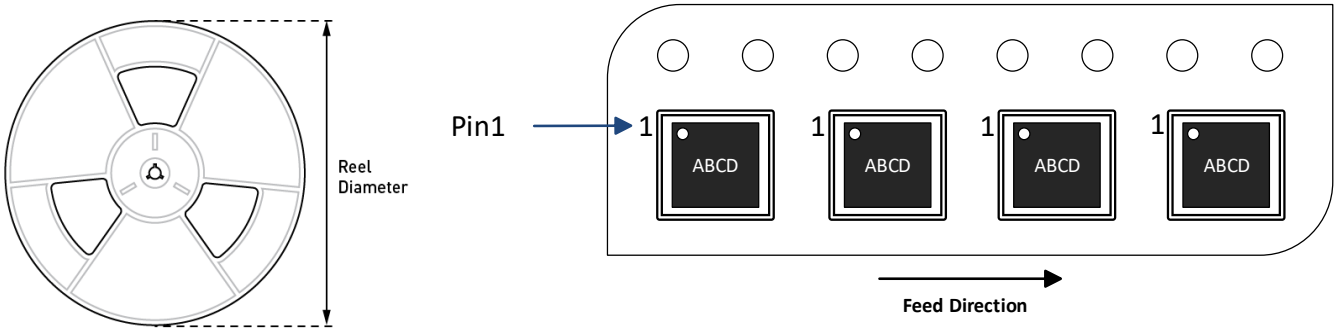


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube (10)	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4312GRE -AEC1-Z	QFN-20 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

Note:

10) N/A indicates “not available” in tubes. For 500 pieces tape & reel prototype quantities, contact MPS. (Order code for 500 pieces partial reel is “-P”. The tape & reel dimensions are the same as for full reel.)

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	10/13/2021	Initial Release	-