MPQ4340/4340J

36V, 4A, Ultra-Low Quiescent Current, Synchronous Step-Down Converter with Multi-Phase Capability, AEC-Q100 Qualified

DESCRIPTION

The MPQ4340/4340J is a configurable-frequency (350kHz to 2.5MHz), synchronous step-down switching converter with integrated internal high-side and low side power MOSFETs (HS-FET and LS-FET, respectively). It provides up to 4A of highly efficient output current (I_{OUT}) with fixed-frequency zero-delay PWM (ZDP) control for near optimal transient response.

The wide 3.3V to 36V input voltage (V_{IN}) range with 42V load dump support accommodates a variety of step-down applications in automotive input environments. A 1µA shutdown current (I_{SD}) allows the device to be used in battery-powered applications.

High power conversion efficiency across a wide load range is achieved by scaling down the switching frequency (f_{SW}) under light-load conditions to reduce switching and gate driver losses. An open-drain power good (PG) signal indicates whether the output voltage (V_{OUT}) is within 94% to 106% of its nominal voltage range. Thermal shutdown provides reliable, fault-tolerant operation. High duty cycle and low-dropout (LDO) mode are provided for automotive cold-crank conditions.

The MPQ4340 is available in a QFN-17 (3mmx4mm) package. The MPQ4340J is available in a QFN-19 (3mmx4mm) package. Both versions are AEC-Q100 qualified.

FEATURES

- **Designed for Automotive Applications**
  - Survives 42V Load Dump
  - Supports Up to 3.1V Cold Crank
  - Low-Dropout (LDO) Mode
  - Up to 4A of Continuous Output Current (I_{OUT})
  - Continuous Operation Up to 36V
  - Zero-Delay PWM Control (ZDP)
  - Multi-Phase Capability
  - 20ns Minimum On Time
  - -40°C to +150°C Junction Temperature Operation Range
  - Available in AEC-Q100 Grade 1

FEATURES *(continued)*

- **Increases Battery Life**
  - 1µA Low Shutdown Current (I_{SD})
  - 3µA Sleep Mode Quiescent Current (I_Q)
  - Advanced Asynchronous Modulation (AAM) Mode Increases Efficiency under Light Loads
- **High Performance for Improved Thermals**
  - Internal 60mΩ High-Side MOSFET and 35mΩ Low-Side MOSFET (HS-FET and LS-FET, Respectively)
- **Optimized for EMC/EMI**
  - 350kHz to 2.5MHz Configurable Switching Frequency (f_{SW})
  - Symmetric Vin Pinout
  - Frequency Spread Spectrum (FSS) Modulation
  - CISPR25 Class 5 Compliant
  - MeshConnect™ Flip-Chip Package
- **Additional Features**
  - Fixed Output Options (1): 1V, 1.1V, 1.8V, 2.5V, 3V, 3.3V, 3.8V, 5V
  - Synchronizable to External Clock
  - Synchronized Clock Output
  - Power Good (PG) Output
  - External Soft Start (SS)
  - Hiccup Over-Current Protection (OCP)
  - Available in a QFN-17 (3mmx4mm) Package for MPQ4340 and QFN-19 (3mmx4mm) Package for MPQ4340J Both with Wettable Flanks

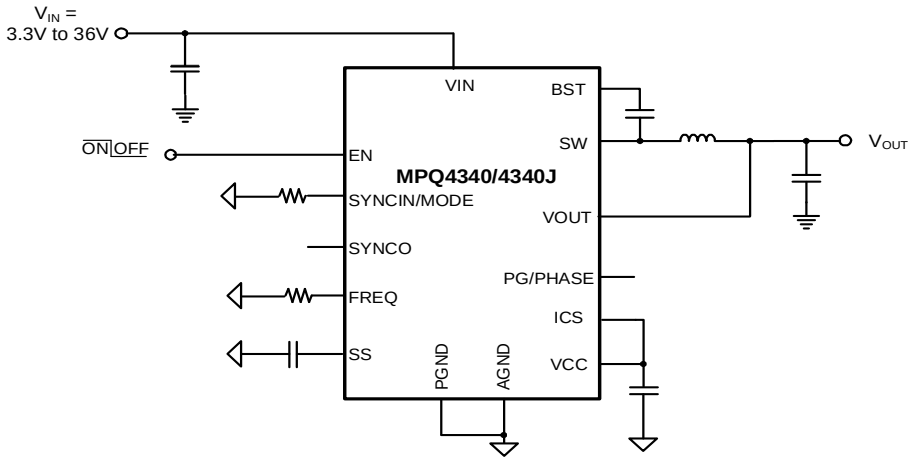
APPLICATIONS

- Automotive Clusters
- Automotive Infotainment
- Advanced Driver Assistance Systems (ADAS)
- Industrial Power Systems

Note:

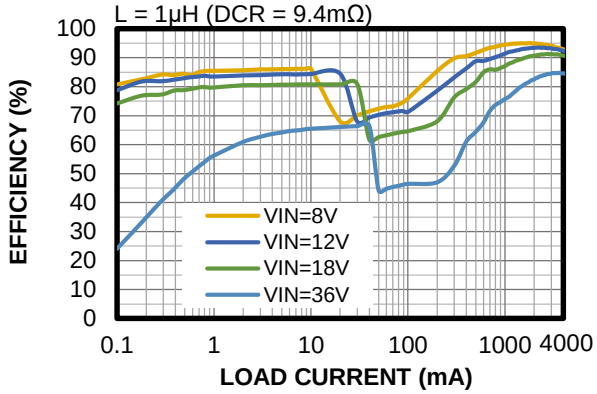
1) See the Ordering Information section on page 3 for details regarding the availability of fixed-output versions. Additional output voltages may be available. Contact MPS for details.

TYPICAL APPLICATION



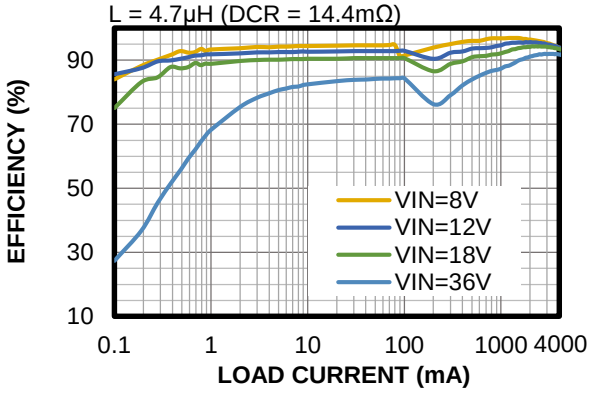
Efficiency vs. Load Current

AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz,
R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ,
L = 1µH (DCR = 9.4mΩ)



Efficiency vs. Load Current

AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz,
R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ,
L = 4.7µH (DCR = 14.4mΩ)



ORDERING INFORMATION

Part Number [2] *	Output Voltage	Package	Top Marking	MSL Rating**
MPQ4340GLE-33-AEC1***	Fixed 3.3V	QFN-17 (3mmx4mm)	*See Below*	1
MPQ4340GLE-5-AEC1***	Fixed 5V	QFN-17 (3mmx4mm)	*See Below*	1
MPQ4340JGLE-33-AEC1***	Fixed 3.3V	QFN-19 (3mmx4mm)	*See Below*	1
MPQ4340JGLE-5-AEC1***	Fixed 5V	QFN-19 (3mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ4340GLE-33-AEC1-Z).

**Moisture Sensitivity Level Rating

***Wettable Flank

Note:

2) Contact MPS for details regarding other fixed-output versions.

TOP MARKING (MPQ4340GLE-33-AEC1 and MPQ4340GLE-5-AEC1)

MPYW
4340
LLL
E

MP: MPS prefix
Y: Year code
W: Week code
4340: Part number
LLL: Lot number
E: Wettable flank

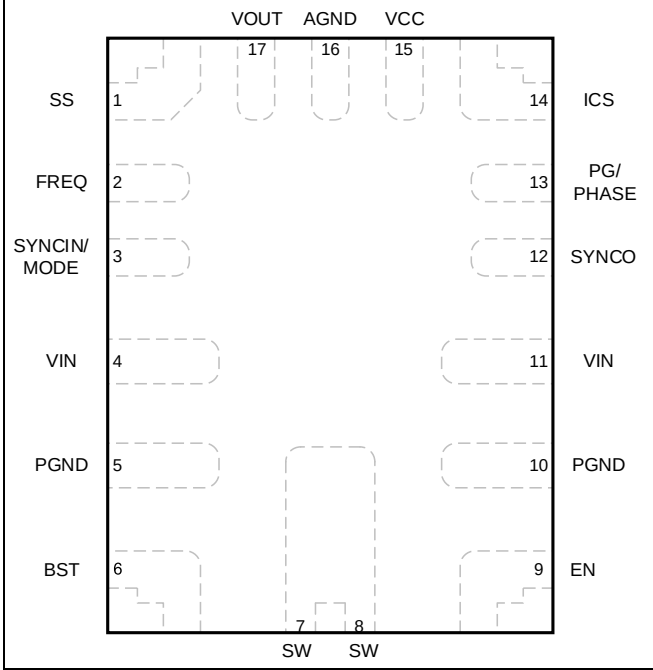
TOP MARKING (MPQ4340JGLE-33-AEC1 and MPQ4340JGLE-5-AEC1)

MPYW
4340
JLLL
E

MP: MPS prefix
Y: Year code
W: Week code
4340J: Part number
LLL: Lot number
E: Wettable flank

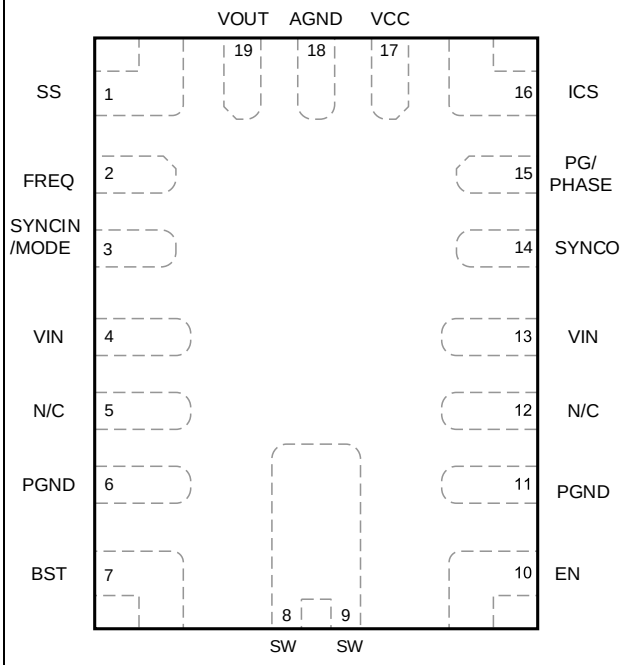
PACKAGE REFERENCE

TOP VIEW



QFN-17 (3mmx4mm)

TOP VIEW



QFN-19 (3mmx4mm)

PIN FUNCTIONS

Pin# QFN-19	Pin # QFN-17	Name	Description
1	1	SS	**Soft-start input.** Place a capacitor from the SS pin to ground to set the soft-start time. The MPQ4340/4340J sources 10μA from SS to the soft-start capacitor (C_{SS}) at start-up. As the SS voltage (V_{SS}) rises, the feedback reference voltage (V_{REF}) increases to limit inrush current during start-up.
2	2	FREQ	**Switching frequency configuration.** Connect a resistor from the FREQ pin to AGND to set the switching frequency (f_{SW}).
3	3	SYNCIN/ MODE	**SYNC input and MODE selection.** Apply a clock signal to the SYNCIN/MODE pin to synchronize the internal f_{SW} to the external clock. Use an external clock or pull this pin high to enter forced continuous conduction mode (FCCM). Pull this pin low to enable advanced asynchronous modulation (AAM) mode and pulse skipping under light loads. Do not float this pin.
4,13	4, 11	VIN	**Input supply.** The VIN pin supplies power to all the internal control circuitry, as well as the power switch connected to SW. Place a decoupling capacitor from VIN to ground, as close as possible to VIN, to minimize switching spikes.
5, 12	-	NC	**No connection.** Float the NC pin.
6, 11	5, 10	PGND	**Power ground.**
7	6	BST	**Bootstrap.** The BST pin is the positive power supply for the high-side MOSFET (HS-FET) connected to SW. Connect a bypass capacitor between the BST and SW pins. See the Floating Driver and Bootstrap Charging (BST, Pin 6) section on page 45 to calculate the size of this capacitor.
8, 9	7, 8	SW	**Switch node.** The SW pin is the internal power switch's output.
10	9	EN	**Enable.** Pull EN above the specified threshold (1V) to enable the chip. Pull the EN pin below the specified threshold (0.85V) to shut down the chip. Do not float this pin.
14	12	SYNCO	**SYNC output and mode selection for slave device.** When SYNCO is in a high-impedance (Hi-Z) state, the MPQ4340/4340J operates as a master device and the SYNCO pin outputs a clock signal in phase with the internal oscillator signal. In this mode, the pin can be floated. To set the MPQ4340/4340J to operates as a slave device, tie this pin to a low-impedance ground, voltage source, or clock (connected resistor < 25kΩ). In this mode, SYNCO acts as a mode input pin and cannot be floated.
15	13	PG/PHASE	**Power good output or phase shift.** The PG pin's output is an open drain. If the device is in master mode and PG is used, it should be connected to a power source via a pull-up resistor. If the output voltage (V_{OUT}) is within 94% to 106% of the nominal voltage, PG goes high. If V_{OUT} is above 107% or below 93% of the nominal voltage, PG goes low. If the device is in slave mode, connect a resistor to AGND to set the phase.
16	14	ICS	**Current sharing.** For multi-phase applications, connect the ICS pins of the devices in parallel to improve current sharing between different phases. Connect this pin to VCC for single-phase operation. Do not float this pin.
17	15	VCC	**Bias supply.** The VCC pin supplies 5V of power to the internal control circuit and gate drivers. Place a decoupling capacitor from VCC to ground, as close as possible to this pin. See the Setting the VCC Capacitor (VCC, Pin 15) section on page 47 to calculate the size of this capacitor.
18	16	AGND	**Analog ground.**
19	17	VOUT	**V_{OUT} regulation point.** Connect the VOUT pin directly to V_{OUT}.

ABSOLUTE MAXIMUM RATINGS (3)

VIN, EN……-0.3V to +42V
SW…… -0.3V to $V_{IN(MAX)}$ + 0.3V
BST…… V_{SW} + 5.5V
All other pins……-0.3V to +6V
Continuous power dissipation (T_A = 25°C)
QFN-17 (3mmx4mm) (4) (8) ……4.28W
QFN-19 (3mmx4mm) (4) (8) ……4.13W
Junction temperature……150°C
Lead temperature……260°C
Storage temperature…….. -65°C to +150°C

ESD Ratings

Human body model (HBM) .....Class 2 (5)
Charged-device model (CDM) ……Class C2b (6)

Recommended Operating Conditions

Supply voltage (V_{IN}) …… .....3.3V to 36V
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-17 (3mmx4mm)
JESD51-7.....44.7.....5.2.....°C/W (7)
EVQ4340-L-00A.....29.2.....6.1.....°C/W (8)

Ψ_{JT}
JESD51-7.....1.2.....°C/W (7)
EVQ4340-L-00A.....6.1.....°C/W (8)

QFN-19 (3mmx4mm) θ_{JA} θ_{JC}
JESD51-7.....43.6....5.4.....°C/W (7)
EVQ4340J-L-00A .....30.3.....°C/W (8)

Ψ_{JT}
JESD51-7.....0.9.....°C/W (7)
EVQ4340J-L-00A.....5.17.....°C/W (8)

Notes:

3) Exceeding these ratings may damage the device.
4) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
5) Per AECQ100-002.
6) Per AECQ100-011.
7) Measured on a JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application, the value of θ_{Jc} shows the thermal resistance from junction-to-case bottom. Ψ_{JT} is the characterization parameter from junction-to-case top.
8) Measured on an MPS standard EVB: 8.3cmx8.3cm, 2oz. copper thickness, 4-layer PCB. Ψ_{JT} is the characterization parameter from junction-to-case top.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J= -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply						
V_{IN} minimum operating voltage	V_{IN_MIN}				3.3	V
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$		2.8	3	3.2	V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$		2.6	2.8	3	V
V_{IN} UVLO hysteresis	$V_{IN\_UVLO\_HYS}$			200		mV
VIN quiescent current (9)	I_Q	V_{OUT} = 1.05 x V_{SET}, no load, (sleep mode), T_J = -40°C to +85°C	1.9	3	3.6	µA
		V_{OUT} = 1.05 x V_{SET}, no load, (sleep mode), T_J = -40°C to +125°C	1.5		15	µA
VIN quiescent current (switching) (9)	I_{Q_SLEEP}	SYNCIN/MODE = GND (AAM mode), switching, no load, T_J = -40°C to +85°C	2.4	3.5	4.5	µA
		SYNCIN/MODE = GND (AAM mode), switching, no load, T_J = -40°C to +125°C	2		16	µA
VIN active current (no switching)	I_{Q_ACTIVE}	SYNCIN/MODE = VCC (CCM), no switching		1200		µA
VIN shutdown current	I_{SD}	EN = 0V, T_J = 25°C		1	3	µA
		EN = 0V			11	µA
VIN over-voltage protection (OVP) threshold	$V_{IN\_OVP\_RISING}$		36	38	40	V
VIN OVP hysteresis	$V_{IN\_OVP\_HYS}$			10		V
Enable (EN)						
EN rising threshold	V_{EN_RISING}		0.8	1.0	1.2	V
EN falling threshold	$V_{EN\_FALLING}$		0.65	0.85	1.05	V
EN hysteresis voltage	V_{EN_HYS}			150		mV
Soft Start (SS) and VCC						
VCC voltage	V_{CC}	I_{VCC} = 0	4.7	5.0	5.3	V
VCC regulation		I_{VCC} = 0mA and 30mA			1	%
VCC current limit	I_{LIMIT_VCC}	V_{CC} = 4V	50	100		mA
		V_{CC} = 0V		70		mA
Soft-start current	I_{SS}	V_{SS} = 0V		10		µA
BST						
BST - SW refresh rising threshold	V_{BST-SW_RISING}			2.5	2.9	V
BST - SW refresh falling threshold	$V_{BST-SW\_FALLING}$			2.3	2.7	V
BST - SW refresh hysteresis	V_{BST-SW_HYS}			0.2		V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J= -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Switches and Frequency						
Switching frequency	f_{SW}	R_{FREQ} = 86.6kΩ	370	410	450	kHz
		R_{FREQ} = 33kΩ	950	1050	1150	kHz
		R_{FREQ} = 15kΩ	1980	2200	2420	kHz
Minimum on time	t_{ON_MIN}			20	35	ns
Minimum off time	t_{OFF_MIN}			120	140	ns
Switch leakage current	I_{SW_LKG}			0.01	5	µA
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	V_{BST} - V_{SW} = 5V		60	110	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	V_{CC} = 5V		35	60	mΩ
Output and Regulation						
Output voltage (V_{OUT}) accuracy of 3.3V fixed-output version	V_{OUT}	T_J = 25°C	3260	3300	3340	mV
		T_J = -40°C to +150°C	3230	3300	3370	mV
V_{OUT} accuracy of 5V fixed-output version	V_{OUT}	T_J = +25°C	4940	5000	5060	mV
		T_J = -40°C to +150°C	4900	5000	5100	mV
V_{OUT} current	I_{VOUT}	V_{OUT} = V_{OUT_REG}		300		nA
V_{OUT} discharge	$I_{DISCHARGE}$	EN = 0V, V_{OUT} = 0.3V, V_{IN} = 3.3V to 36V	1.8			mA
Power Good (PG)						
PG rising threshold	PG_{VTH_RISING}	V_{OUT} rising	91	94	97	%
		V_{OUT} falling	103	106	109	
PG falling threshold	$PG_{VTH\_FALLING}$	V_{OUT} falling	90	93	96	
		V_{OUT} rising	104	107	110	
PG trip threshold hysteresis	PG_{VTH_HYS}			1		%
PG output voltage low	V_{PG_LOW}	I_{SINK} = 1mA		0.1	0.3	V
PG rising deglitch	$t_{PG\_R\_DEGLITCH}$			50		µs
PG falling deglitch	$t_{PG\_F\_DEGLITCH}$			50		µs
Current Sharing						
Current-sharing gain	G_{CS}			100		mV/A
SYNCIN and SYNCO						
SYNCIN/MODE voltage rising threshold	V_{SYNC_RISING}		1.8			V
SYNCIN/MODE voltage falling threshold	$V_{SYNC\_FALLING}$				0.4	V
SYNCIN/MODE timeout	t_{MODE}	SYNCIN/MODE low to DCM		41		µs
SYNCIN clock range	f_{SYNC}	% of freerunning frequency	90		115	%
SYNCO high voltage	V_{SYNCO_HIGH}	I_{SYNCO} = -1mA	3.3	5		V
SYNCO low voltage	V_{SYNCO_LOW}	I_{SYNCO} = 1mA			0.4	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J= -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Protections						
High-side (HS) current limit	I_{LIMIT_HS}	Duty cycle = 30%	6.3	7.7	9.7	A
Low-side (LS) valley current limit (9)	I_{LIMIT_LS}		4.1	5.9	7.6	A
Zero-current detection (ZCD) threshold	I_{ZCD}	AAM mode	-0.05	0.1	+0.25	A
LS reverse current limit	$I_{LIMIT\_REVERSE}$	FCCM		4		A
Thermal shutdown (9)	T_{SD}		150	170		°C
Thermal shutdown hysteresis (9)	T_{SD_HYS}			20		°C

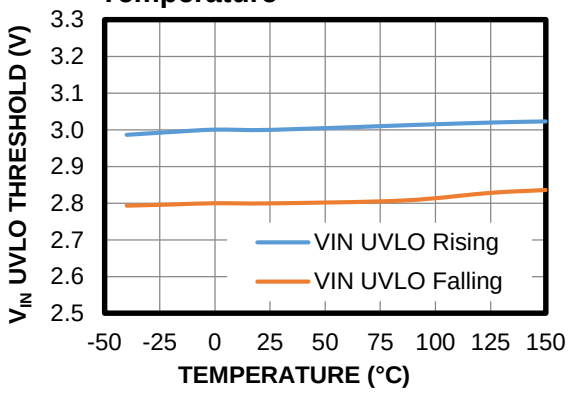
Note:

9) Guaranteed by design and characterization. Not tested in production.

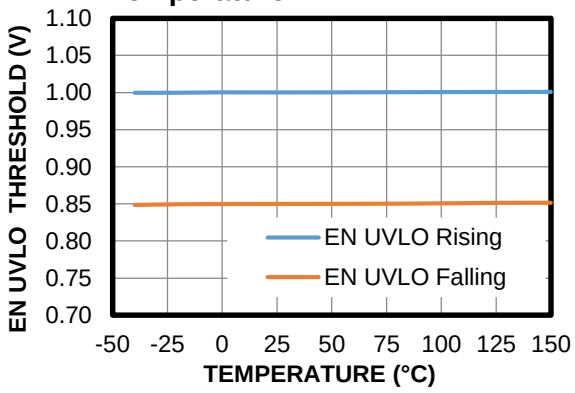
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, T_J = -40°C to +150°C, unless otherwise noted.

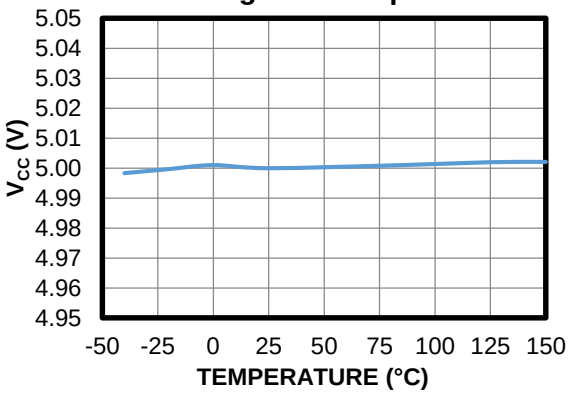
V_{IN} UVLO Threshold vs. Temperature



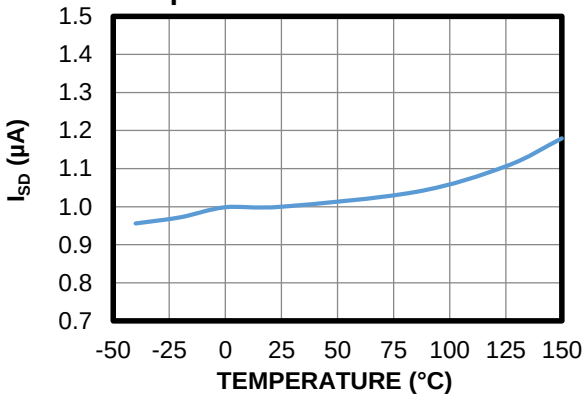
EN UVLO Threshold vs. Temperature



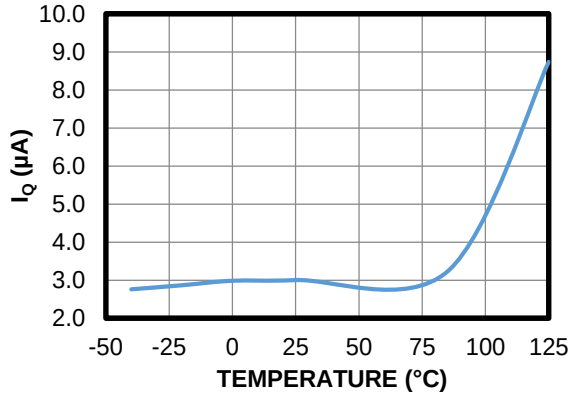
VCC Voltage vs. Temperature



V_{IN} Shutdown Current vs. Temperature

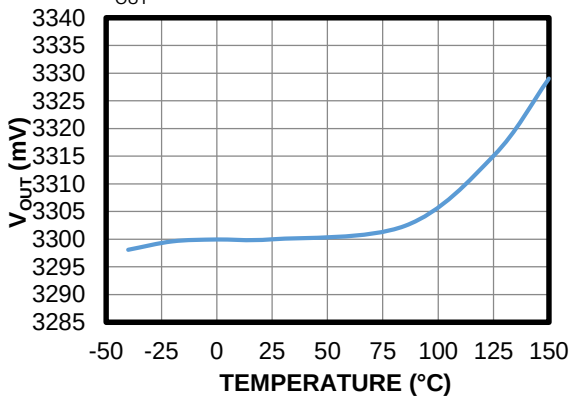


Quiescent Current vs. Temperature



V_{OUT} vs. Temperature

V_{OUT} = 3.3V

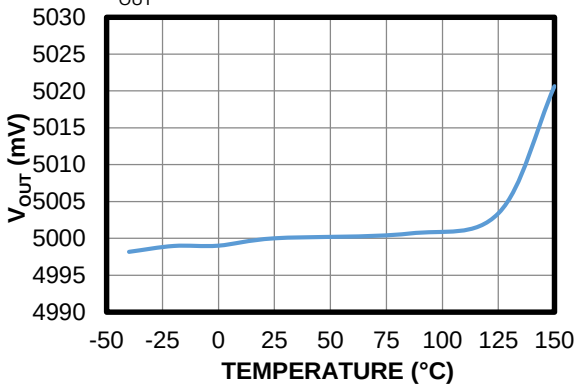


TYPICAL CHARACTERISTICS *(continued)*

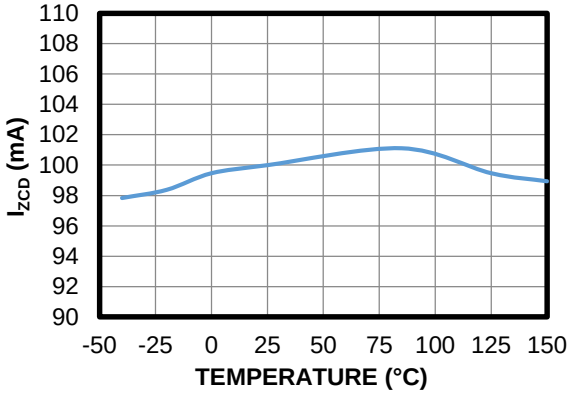
V_{IN} = 12V, V_{OUT} = 3.3V, T_J = -40°C to +150°C, unless otherwise noted.

V_{OUT} vs. Temperature

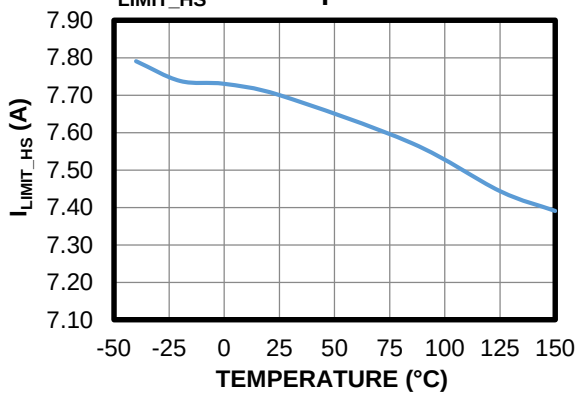
V_{OUT} = 5V



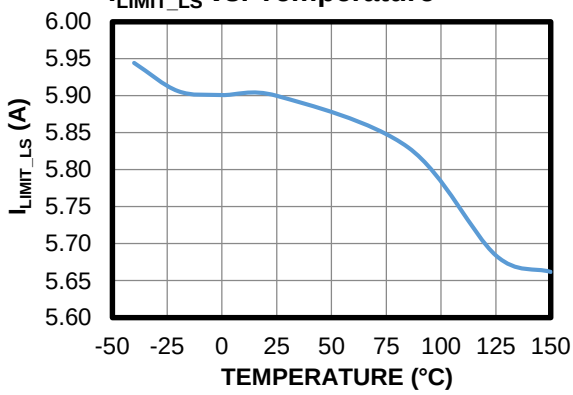
ZCD Threshold vs. Temperature



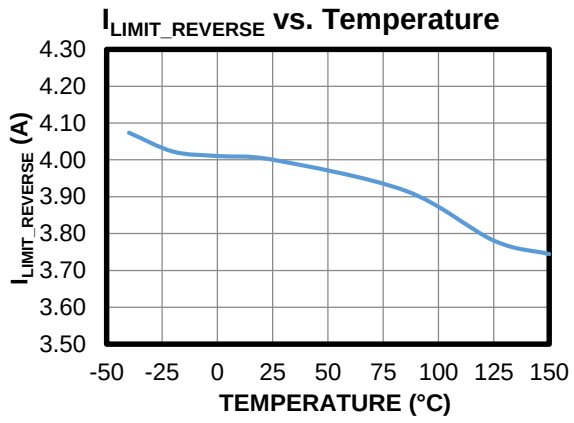
I_{LIMIT_HS} vs. Temperature



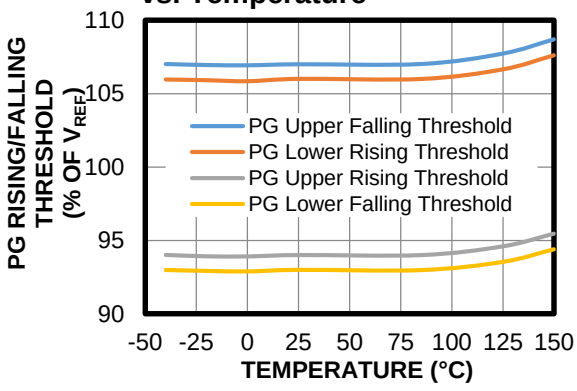
I_{LIMIT_LS} vs. Temperature



$I_{LIMIT\_REVERSE}$ vs. Temperature



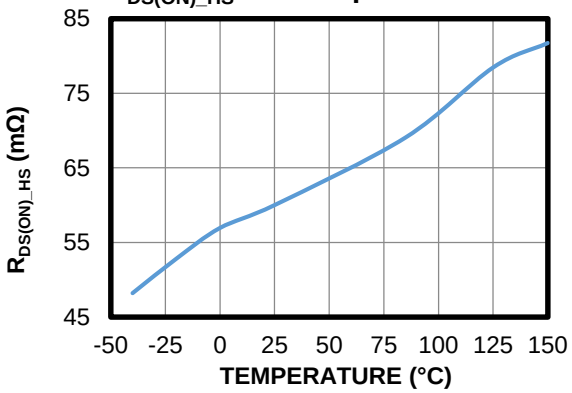
PG Rising/Falling Threshold vs. Temperature



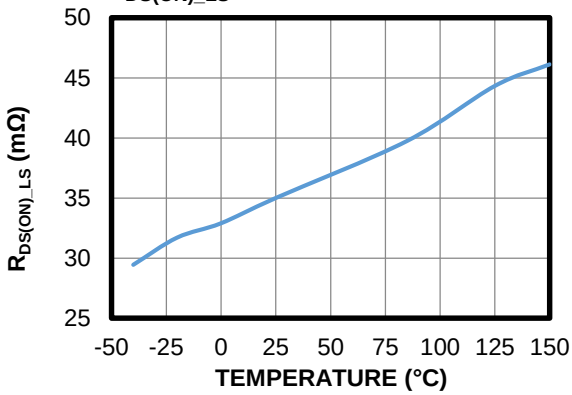
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, T_J = -40°C to +150°C, unless otherwise noted.

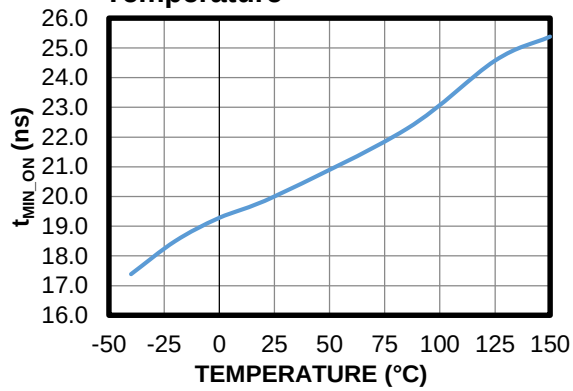
$R_{DS(ON)\_HS}$ vs. Temperature



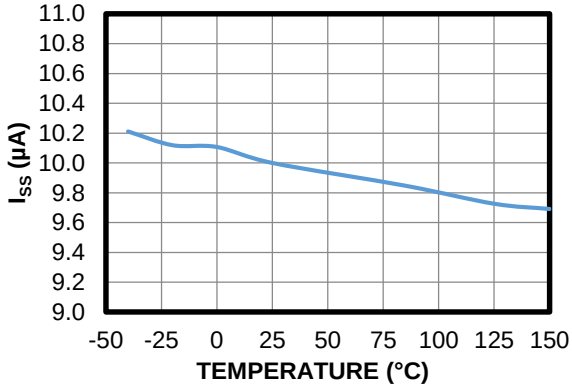
$R_{DS(ON)\_LS}$ vs. Temperature



Minimum On Time vs. Temperature

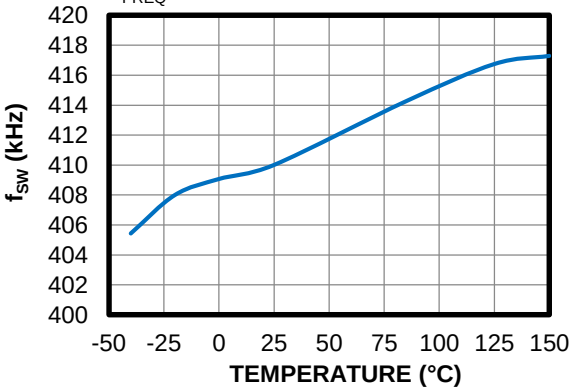


Soft-Start Current vs. Temperature



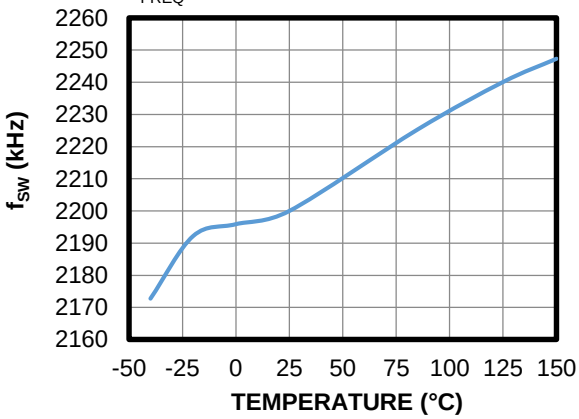
f_{SW} vs. Temperature

R_{FREQ} = 86.6kΩ



f_{SW} vs. Temperature

R_{FREQ} = 15kΩ

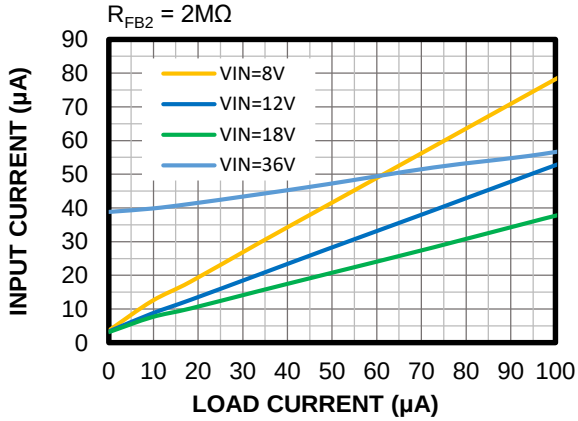


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH (DCR = 9.4mΩ), f_{SW} = 2.2MHz, 1-phase, T_A = 25°C, unless otherwise noted.

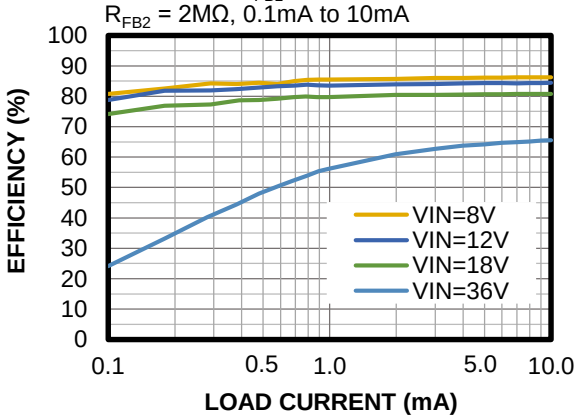
Input Current vs. Load Current

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



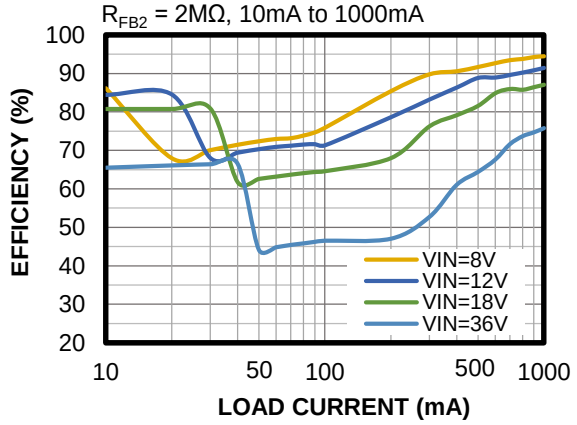
Efficiency vs. Load Current

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, 0.1mA to 10mA



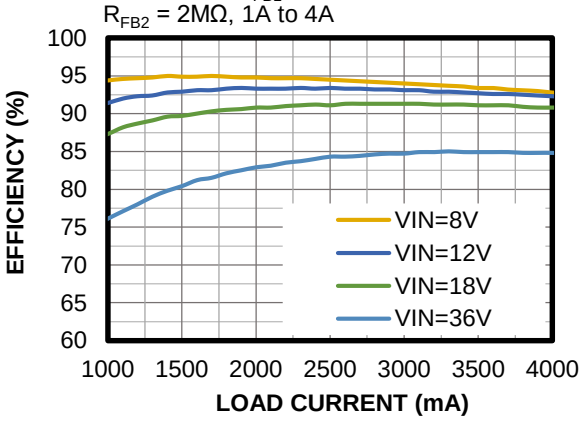
Efficiency vs. Load Current

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, 10mA to 1000mA



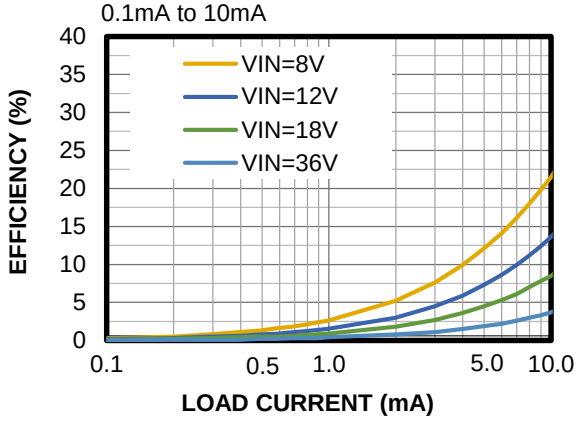
Efficiency vs. Load Current

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, 1A to 4A



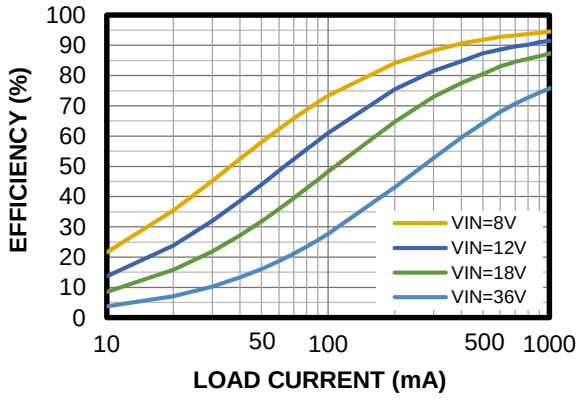
Efficiency vs. Load Current

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, 0.1mA to 10mA



Efficiency vs. Load Current

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, 10mA to 1000mA

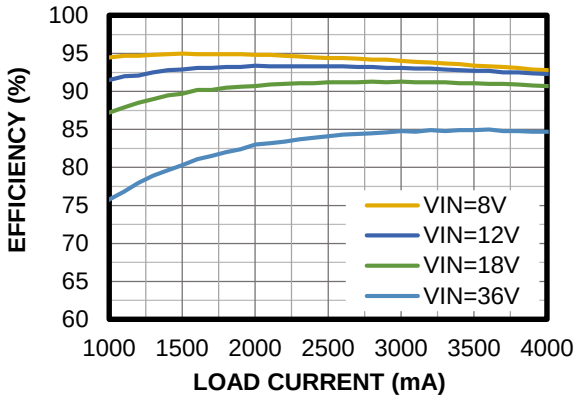


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH (DCR = 9.4mΩ), f_{SW} = 2.2MHz, 1-phase, T_A = 25°C, unless otherwise noted.

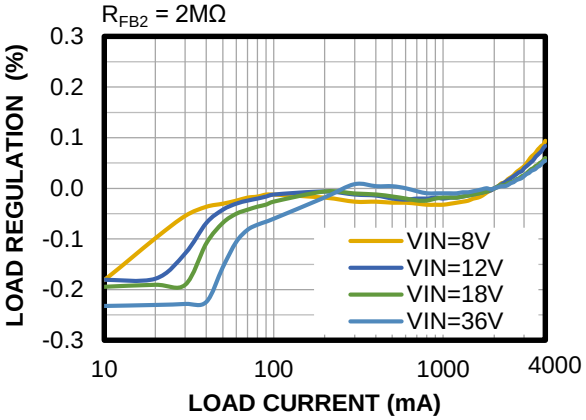
Efficiency vs. Load Current

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, 1A to 4A



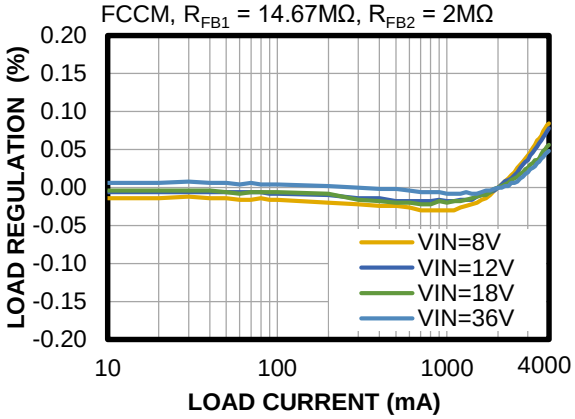
Load Regulation

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



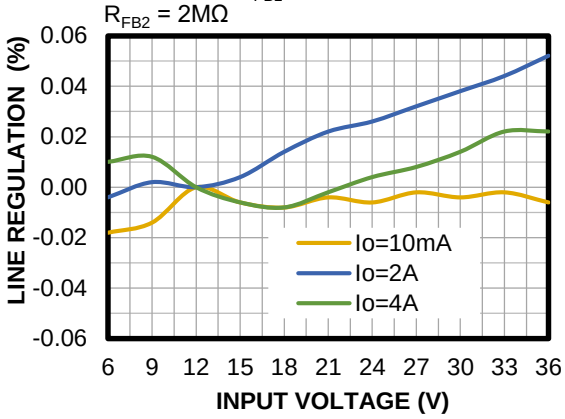
Load Regulation

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



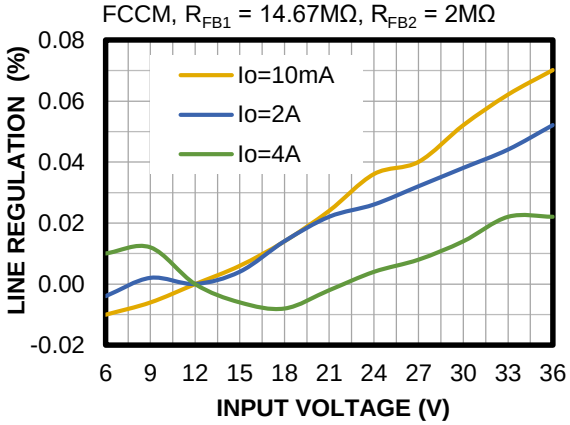
Line Regulation

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



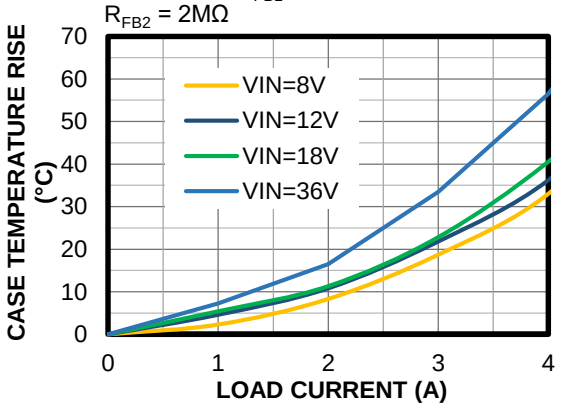
Line Regulation

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



Case Temperature Rise

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ

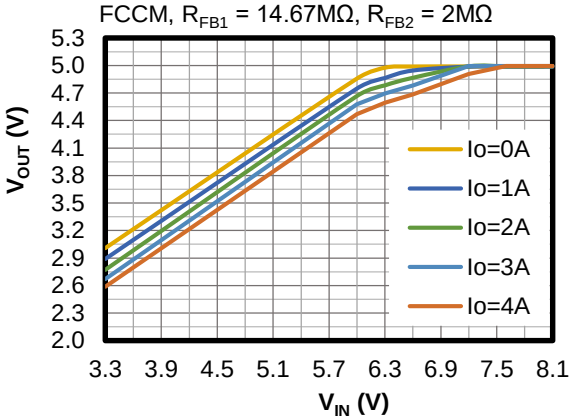


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH (DCR = 9.4mΩ), f_{SW} = 2.2MHz, 1-phase, T_A = 25°C, unless otherwise noted.

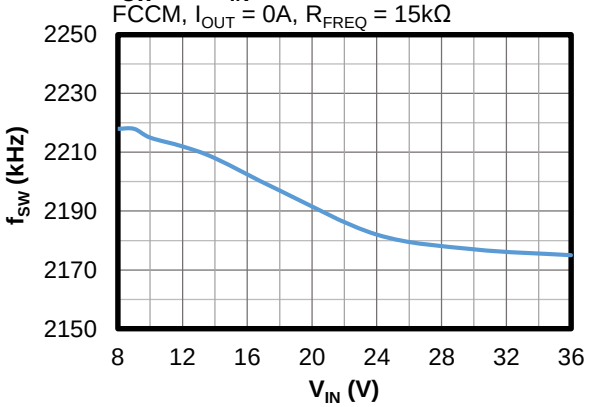
Low-Dropout Mode

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



f_{SW} vs. V_{IN}

FCCM, I_{OUT} = 0A, R_{FREQ} = 15kΩ

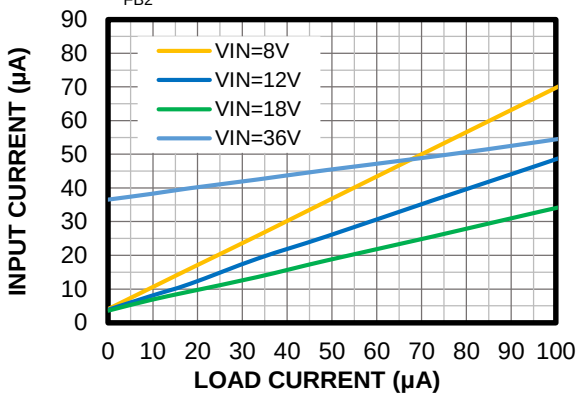


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH (DCR = 14.4mΩ), f_{SW} = 410kHz, 1-phase, T_A = 25°C, unless otherwise noted.

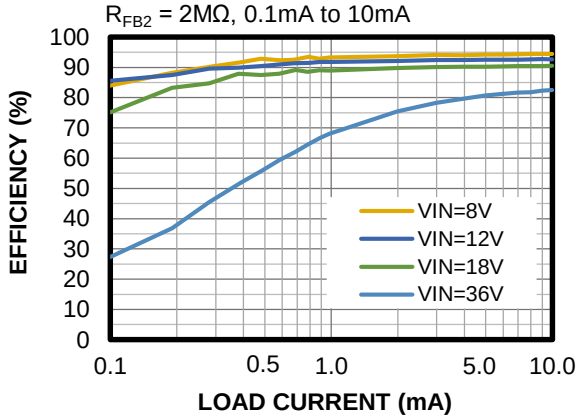
Input Current vs. Load Current

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



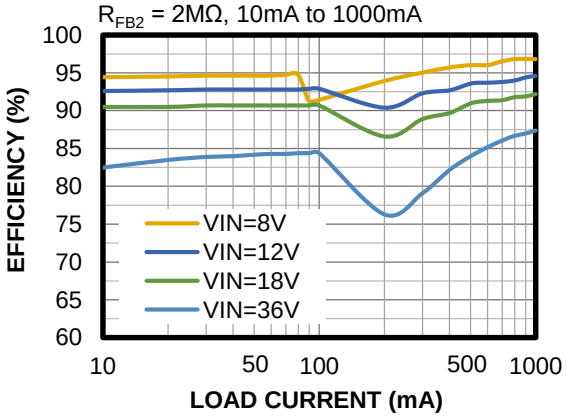
Efficiency vs. Load Current

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, 0.1mA to 10mA



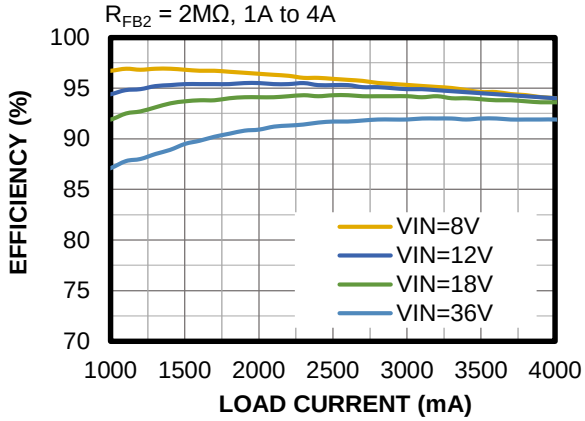
Efficiency vs. Load Current

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, 10mA to 1000mA



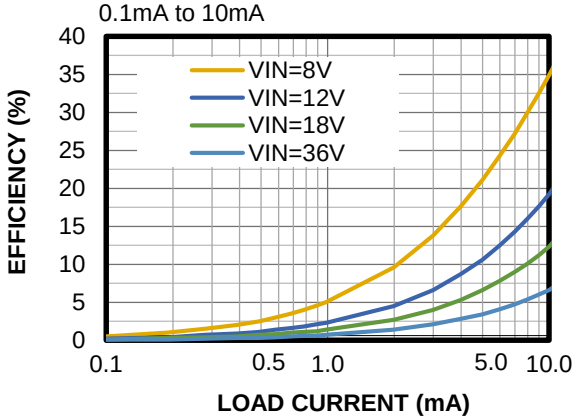
Efficiency vs. Load Current

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, 1A to 4A



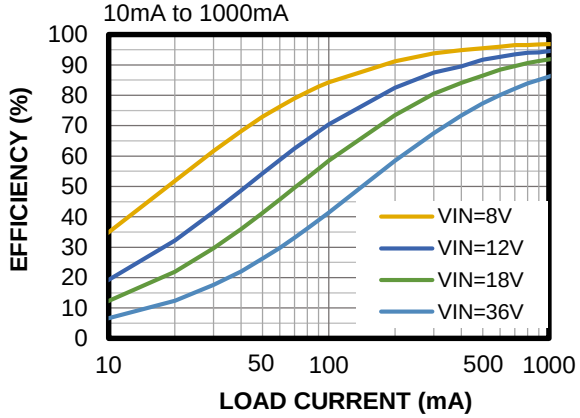
Efficiency vs. Load Current

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, 0.1mA to 10mA



Efficiency vs. Load Current

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, 10mA to 1000mA

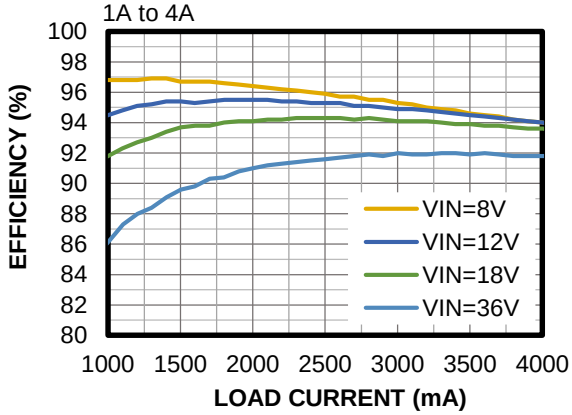


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH (DCR = 14.4mΩ), f_{SW} = 410kHz, 1-phase, T_A = 25°C, unless otherwise noted.

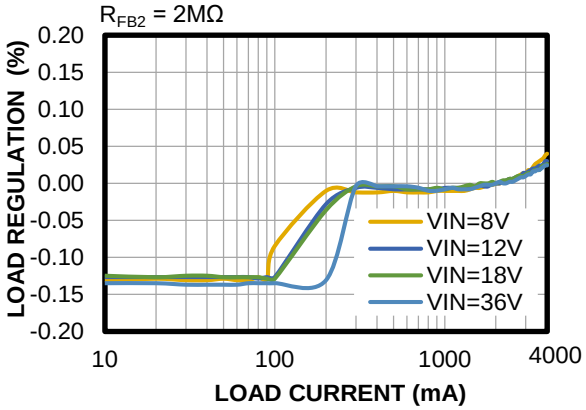
Efficiency vs. Load Current

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, 1A to 4A



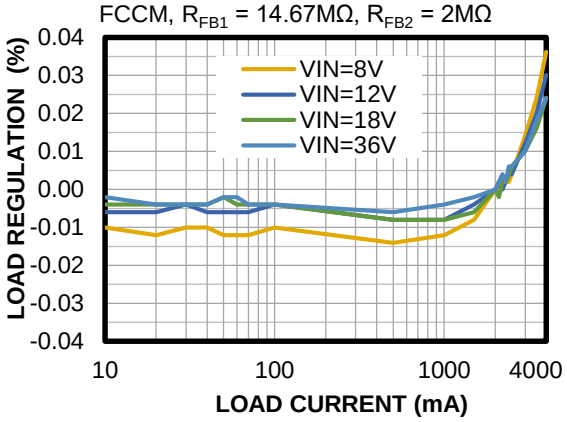
Load Regulation

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



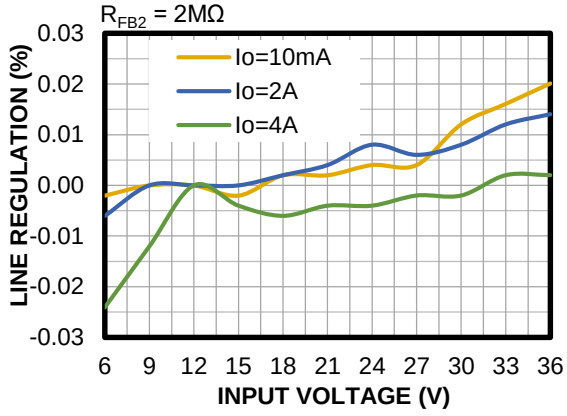
Load Regulation

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



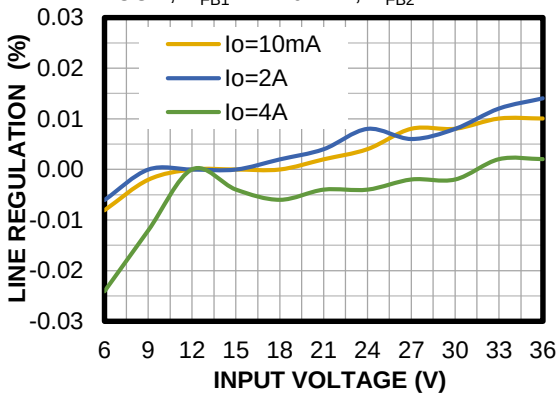
Line Regulation

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



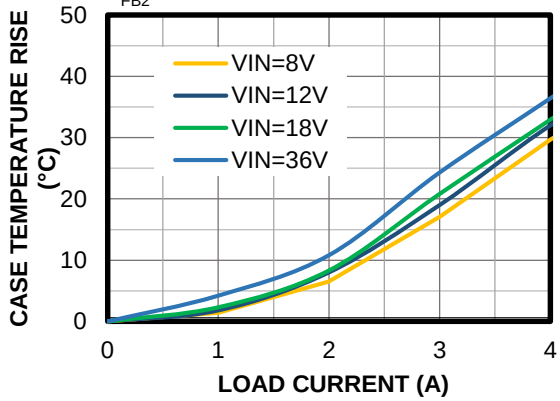
Line Regulation

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



Case Temperature Rise

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ

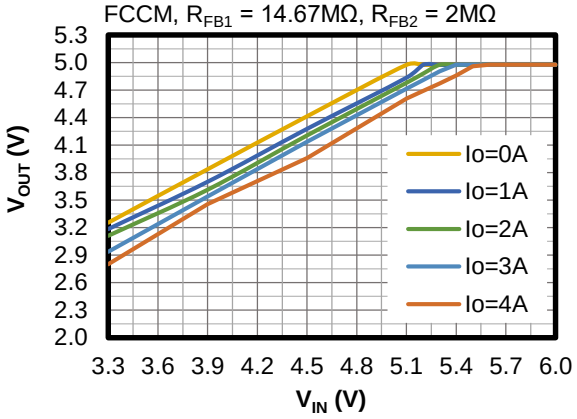


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH (DCR = 14.4mΩ), f_{SW} = 410kHz, 1-phase, T_A = 25°C, unless otherwise noted.

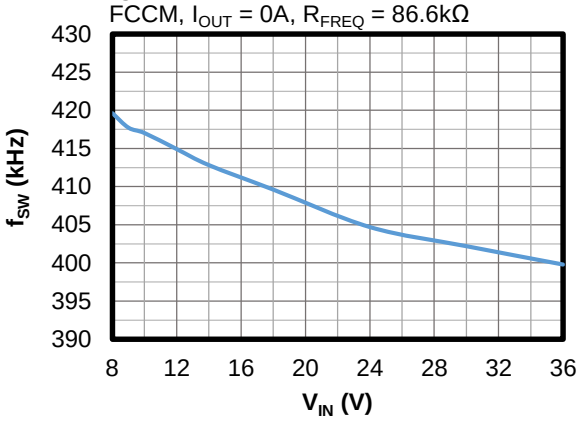
Low-Dropout Mode

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



f_{SW} vs. V_{IN}

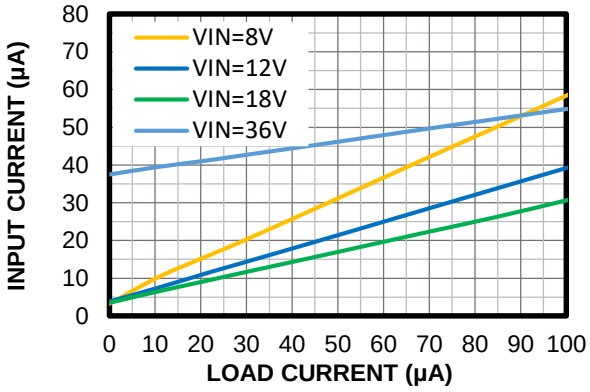
FCCM, I_{OUT} = 0A, R_{FREQ} = 86.6kΩ



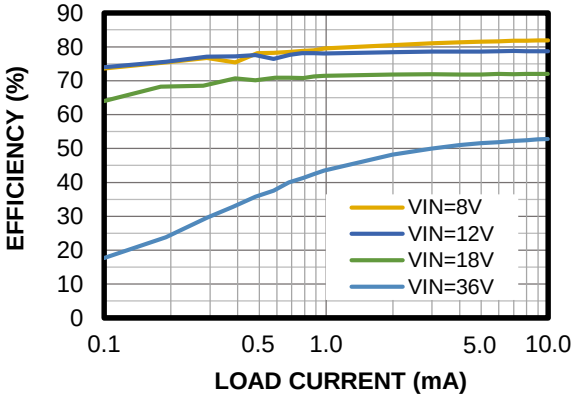
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 1µH (DCR = 9.4mΩ), f_{SW} = 2.2MHz, 1-phase, T_A = 25°C, unless otherwise noted.

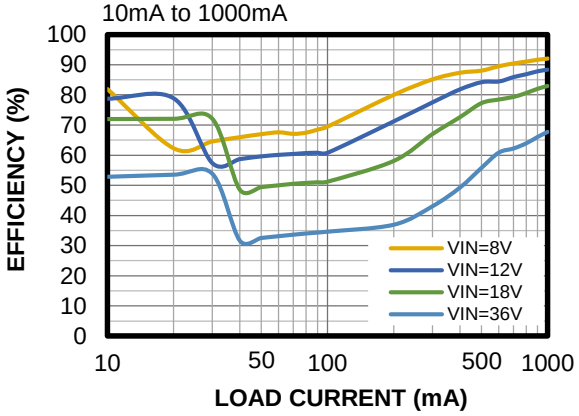
Input Current vs. Load Current
AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



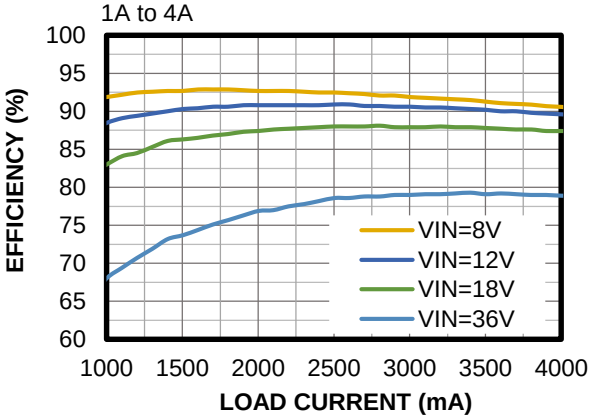
Efficiency vs. Load Current
AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ, 0.1mA to 10mA



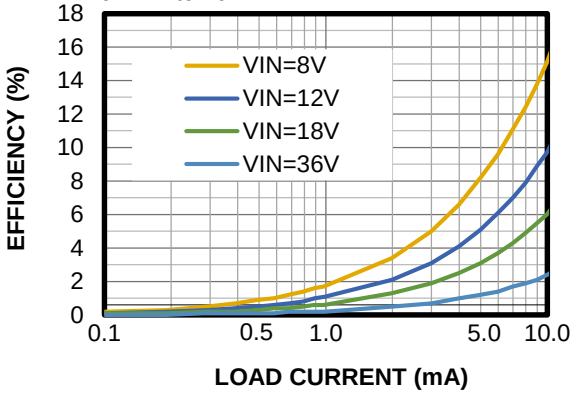
Efficiency vs. Load Current
AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ, 10mA to 1000mA



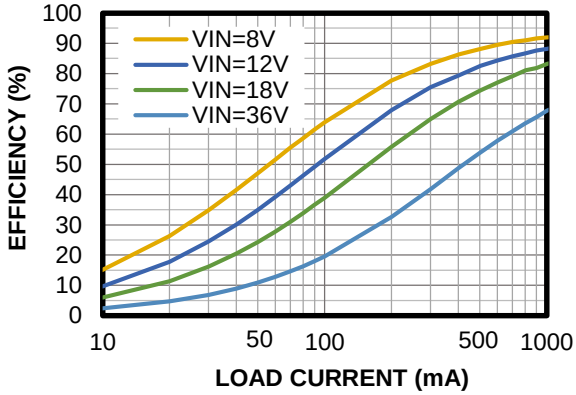
Efficiency vs. Load Current
AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ, 1A to 4A



Efficiency vs. Load Current
FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ, 0.1mA to 10mA



Efficiency vs. Load Current
FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ, 10mA to 1000mA

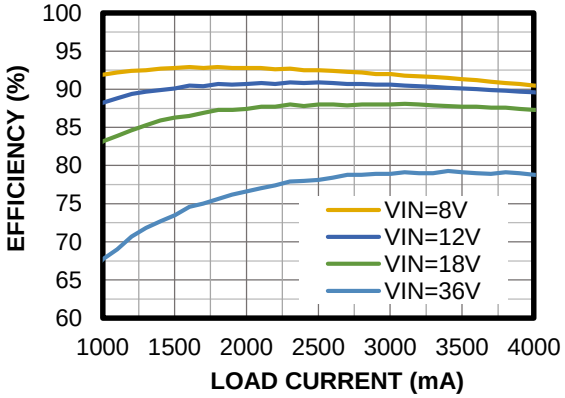


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 1µH (DCR = 9.4mΩ), f_{SW} = 2.2MHz, 1-phase, T_A = 25°C, unless otherwise noted.

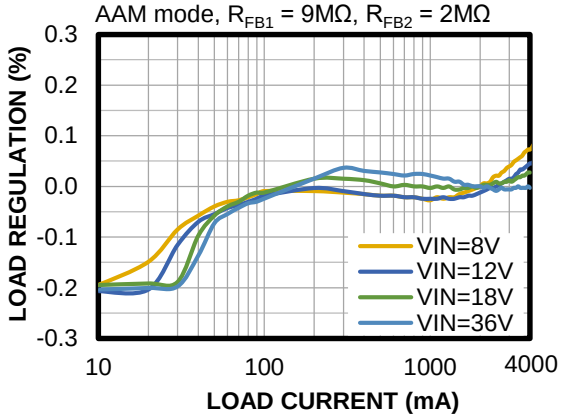
Efficiency vs. Load Current

FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ, 1A to 4A



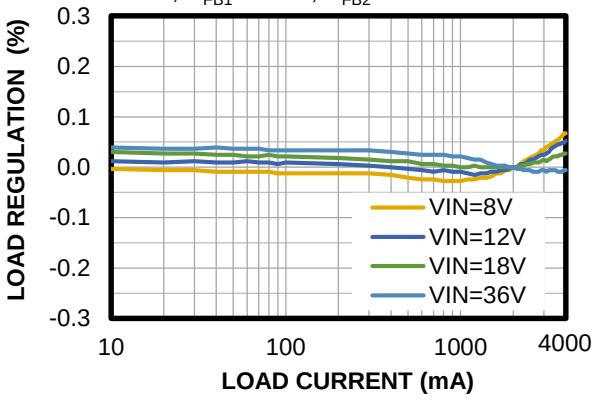
Load Regulation

AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



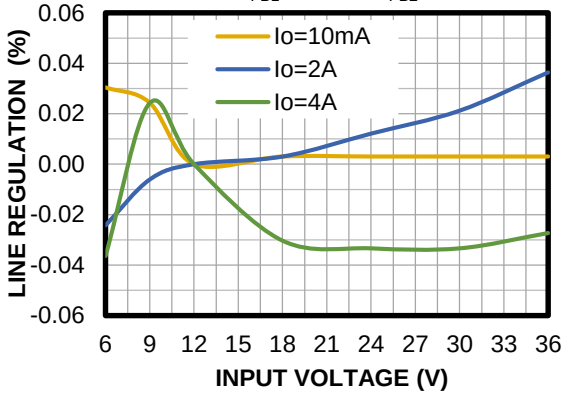
Load Regulation

FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



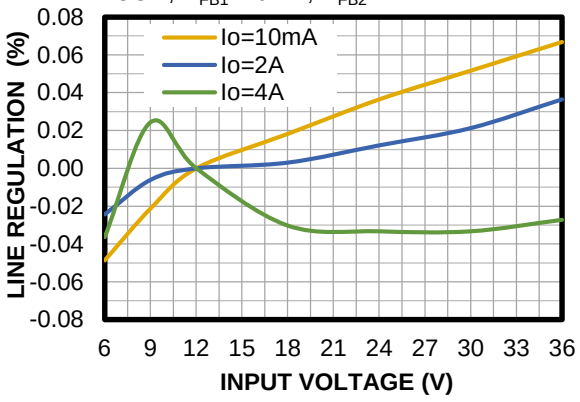
Line Regulation

AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



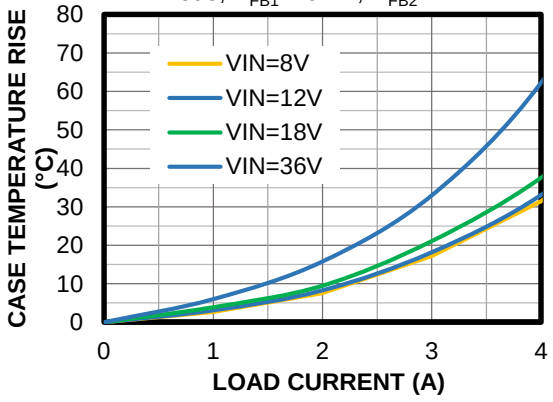
Line Regulation

FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



Case Temperature Rise

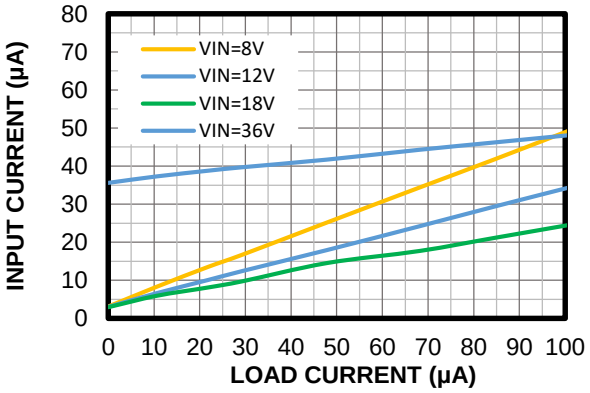
AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



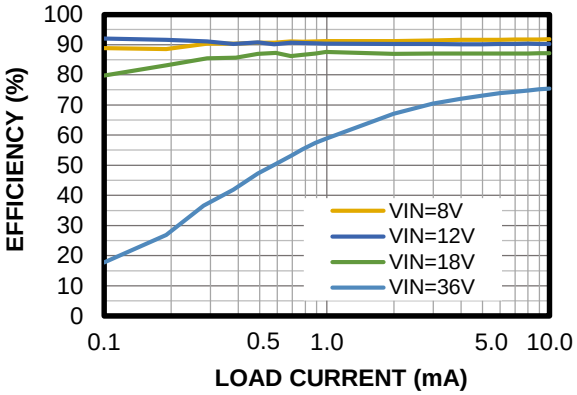
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH (DCR = 14.4mΩ), f_{SW} = 410kHz, 1-phase, T_A = 25°C, unless otherwise noted.

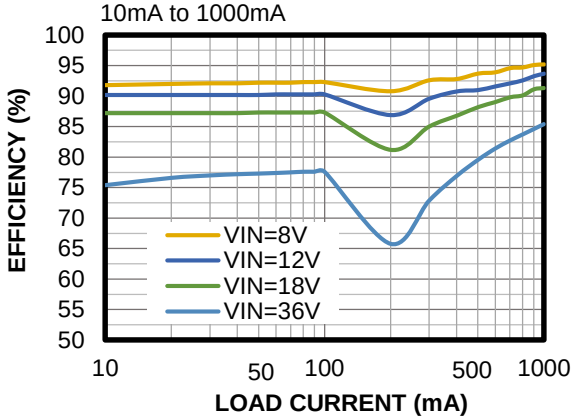
Input Current vs. Load Current
AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



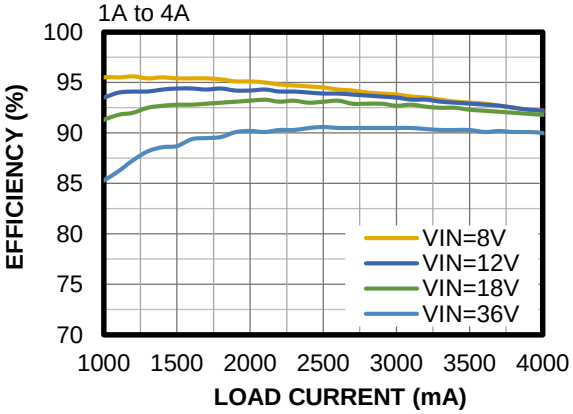
Efficiency vs. Load Current
AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ, 0.1mA to 10mA



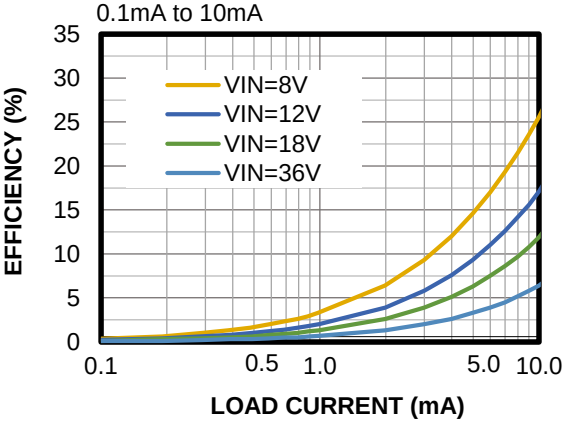
Efficiency vs. Load Current
AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ, 10mA to 1000mA



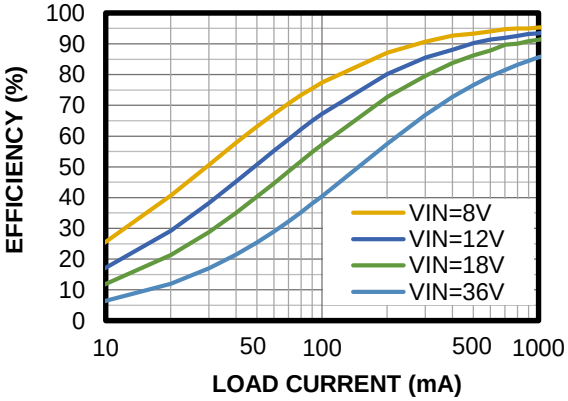
Efficiency vs. Load Current
AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ, 1A to 4A



Efficiency vs. Load Current
FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ, 0.1mA to 10mA



Efficiency vs. Load Current
FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ, 10mA to 1000mA

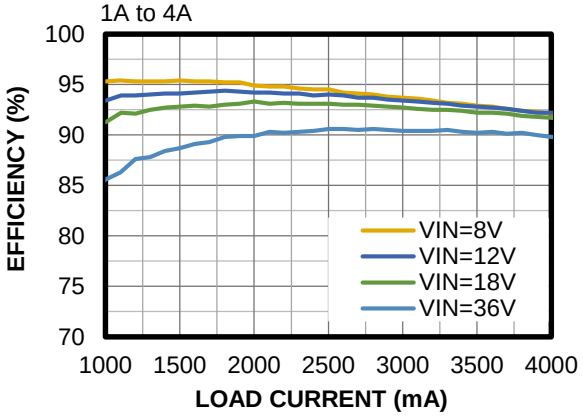


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH (DCR = 14.4mΩ), f_{SW} = 410kHz, 1-phase, T_A = 25°C, unless otherwise noted.

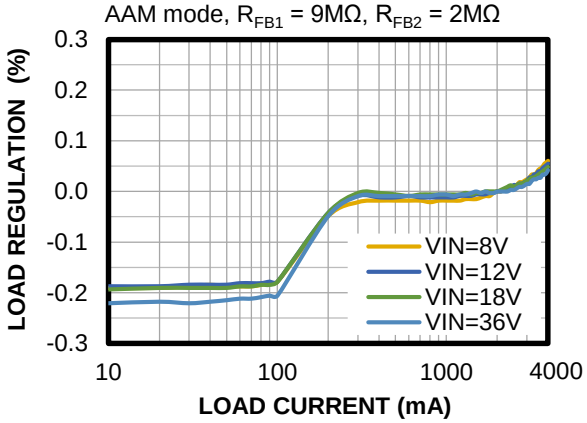
Efficiency vs. Load Current

FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ, 1A to 4A



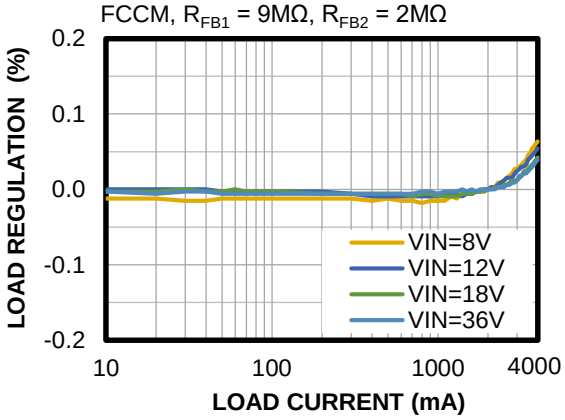
Load Regulation

AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



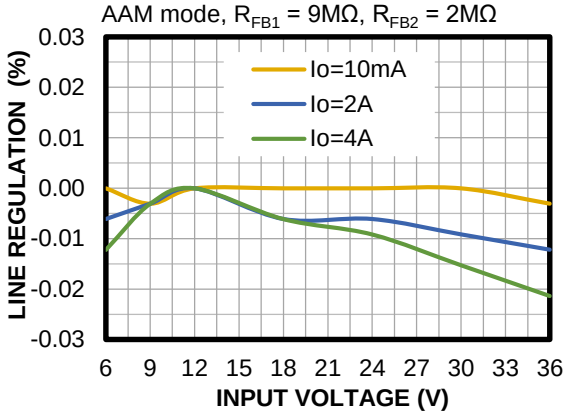
Load Regulation

FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



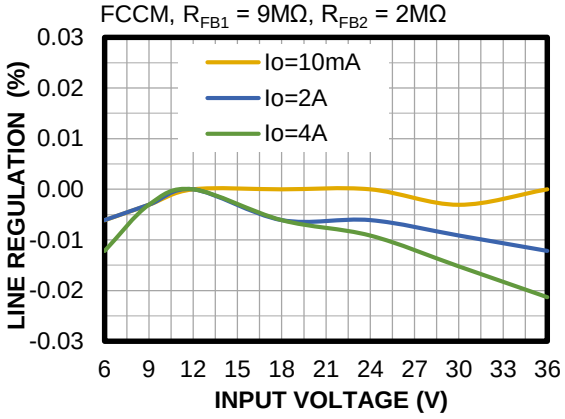
Line Regulation

AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



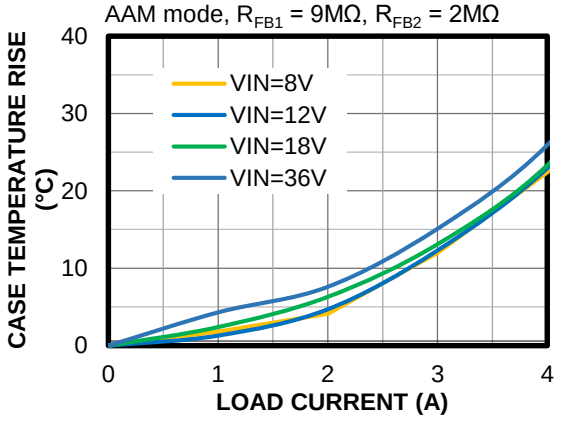
Line Regulation

FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



Case Temperature Rise

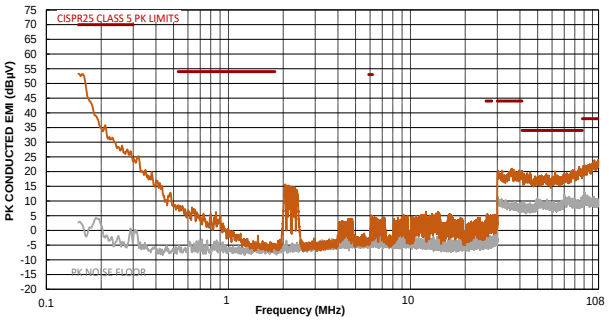
AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



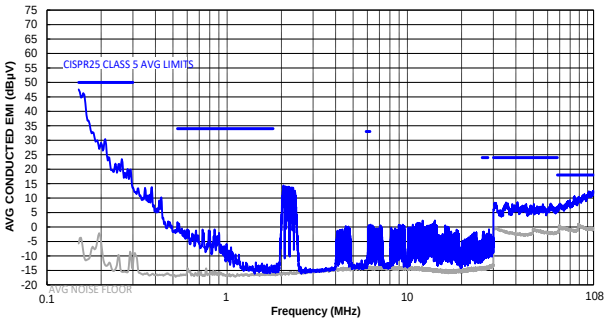
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, I_{OUT} = 4A, AAM mode, 1-phase, T_A = 25°C, unless otherwise noted. (10)

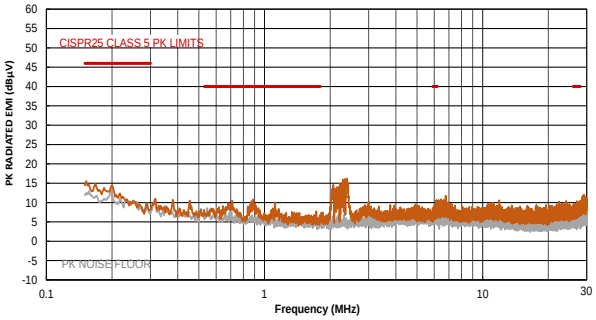
CISPR25 Class 5 Peak Conducted Emissions
150kHz to 108MHz



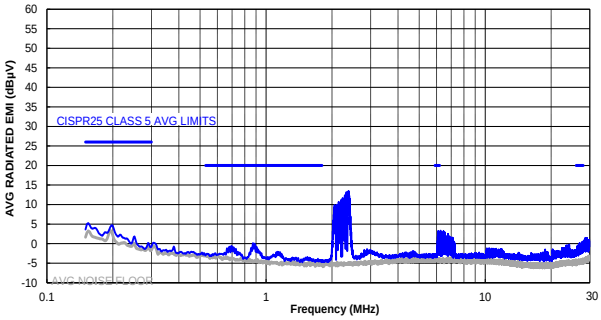
CISPR25 Class 5 Average Conducted Emissions
150kHz to 108MHz



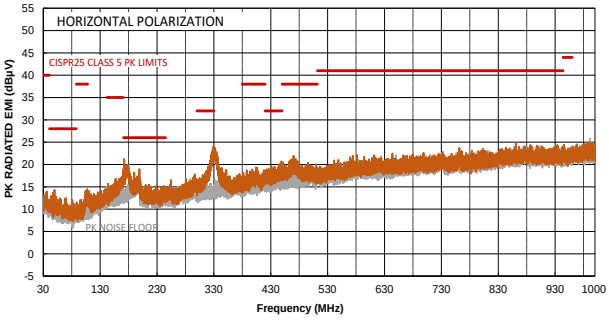
CISPR25 Class 5 Peak Radiated Emissions
150kHz to 30MHz



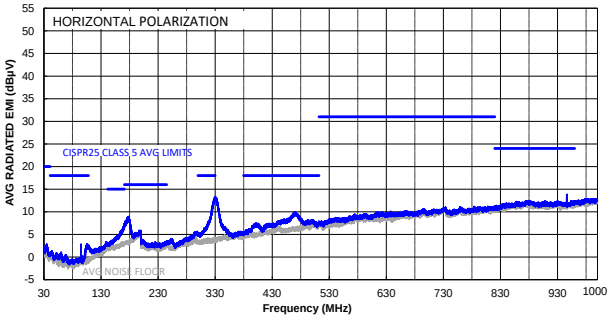
CISPR25 Class 5 Average Radiated Emissions
150kHz to 30MHz



CISPR25 Class 5 Peak Radiated Emissions
Horizontal, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions
Horizontal, 30MHz to 1GHz

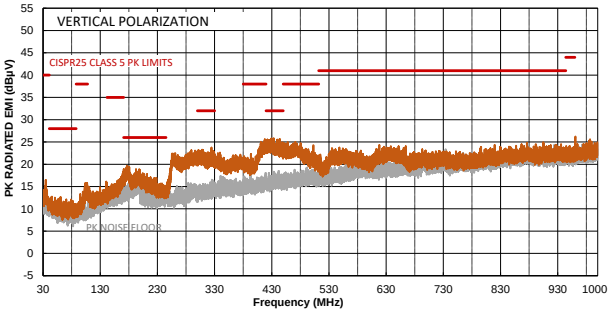


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, I_{OUT} = 4A, AAM mode, 1-phase, T_A = 25°C, unless otherwise noted. (10)

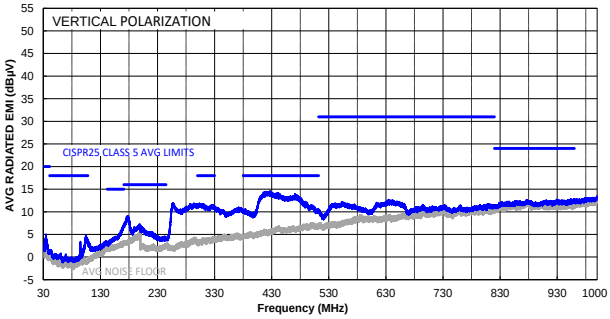
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

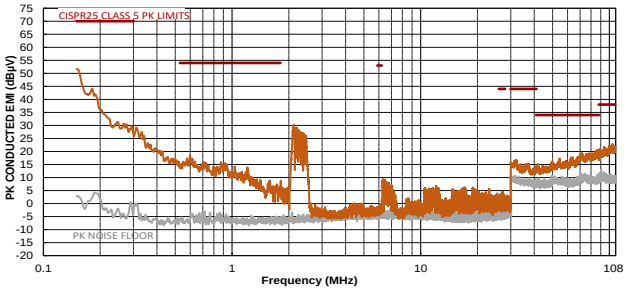
Vertical, 30MHz to 1GHz



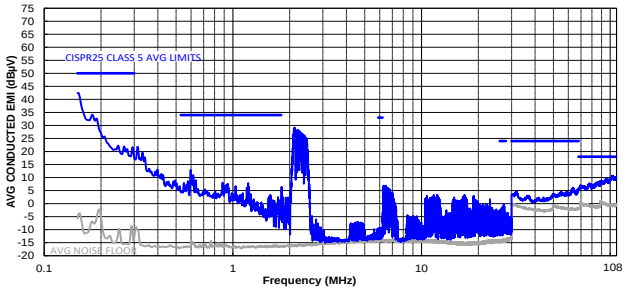
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, I_{OUT} = 8A, AAM mode, 2-phase, T_A = 25°C, unless otherwise noted. (11)

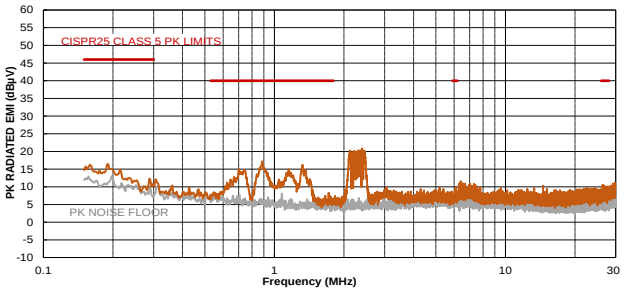
CISPR25 Class 5 Peak Conducted Emissions
150kHz to 108MHz



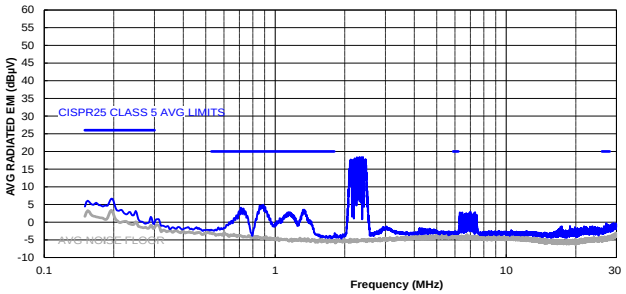
CISPR25 Class 5 Average Conducted Emissions
150kHz to 108MHz



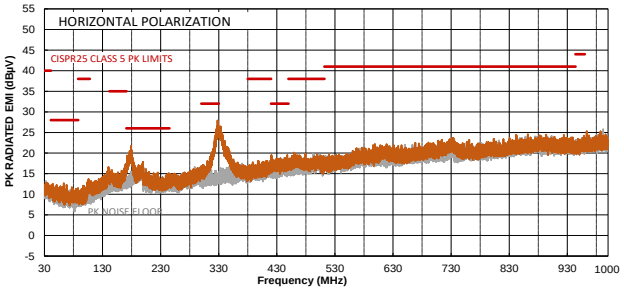
CISPR25 Class 5 Peak Radiated Emissions
150kHz to 30MHz



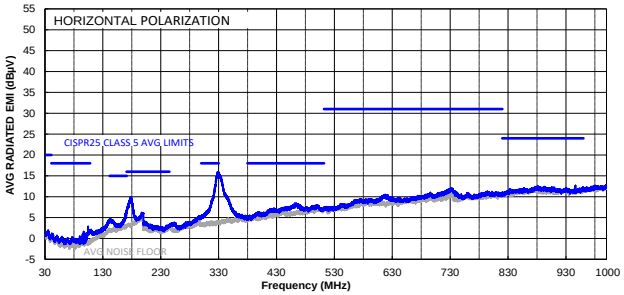
CISPR25 Class 5 Average Radiated Emissions
150kHz to 30MHz



CISPR25 Class 5 Peak Radiated Emissions
Horizontal, 30MHz to 1GHz



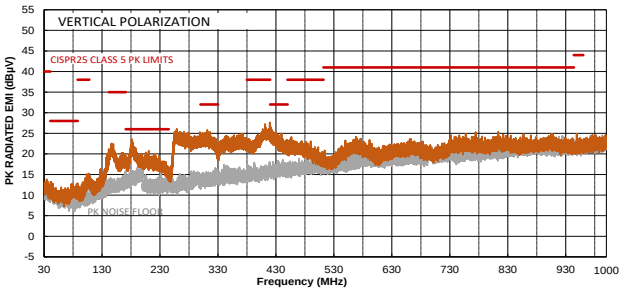
CISPR25 Class 5 Average Radiated Emissions
Horizontal, 30MHz to 1GHz



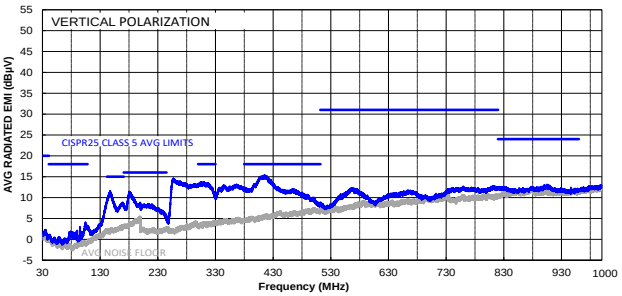
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, I_{OUT} = 8A, AAM mode, 2-phase, T_A = 25°C, unless otherwise noted. (11)

CISPR25 Class 5 Peak Radiated Emissions
Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions
Vertical, 30MHz to 1GHz



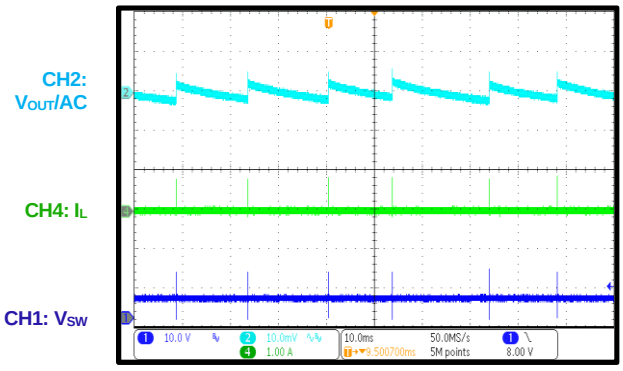
Notes:

10) The EMC test results are based on the typical application circuit with EMI filters (see Figure 15 on page 52).
11) The EMC test results are based on the typical application circuit with EMI filters (see Figure 17 on page 53).

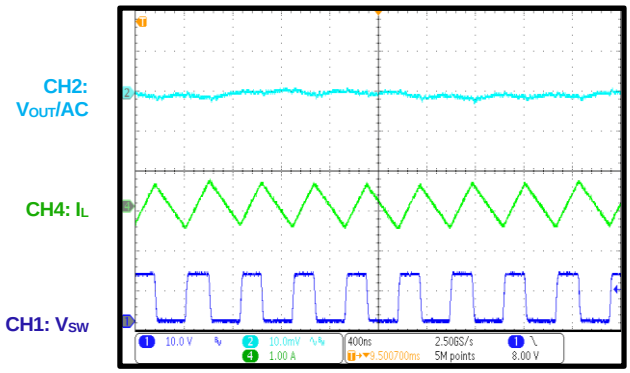
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, 1-phase, T_A = 25°C, unless otherwise noted.

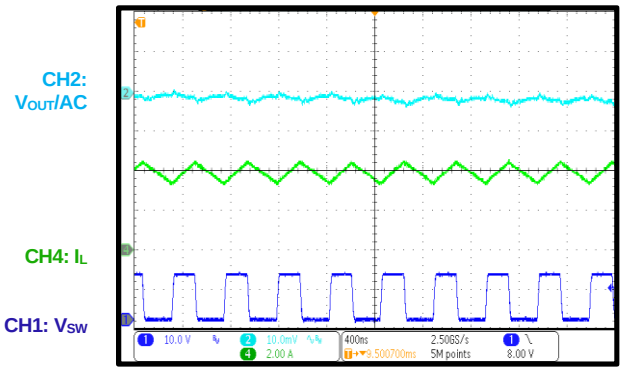
Steady State
I_{OUT} = 0A, AAM mode



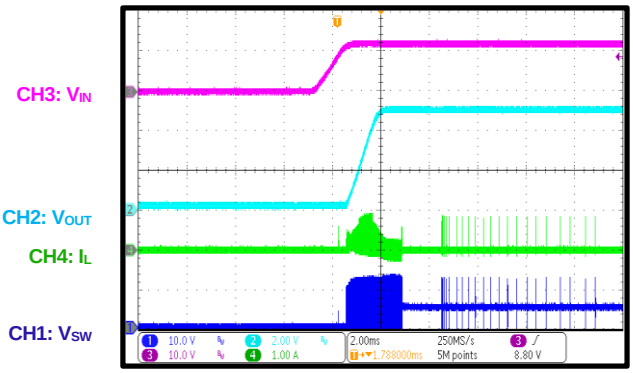
Steady State
I_{OUT} = 0A, FCCM



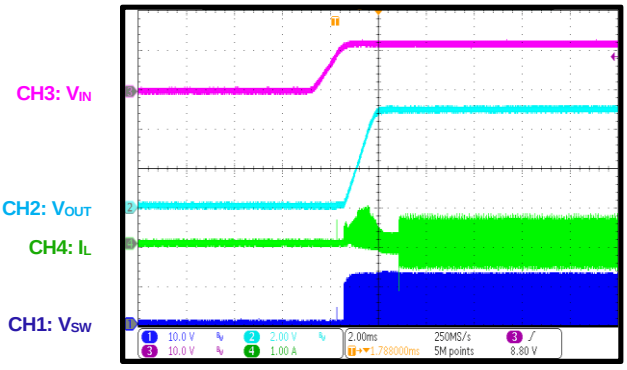
Steady State
I_{OUT} = 4A



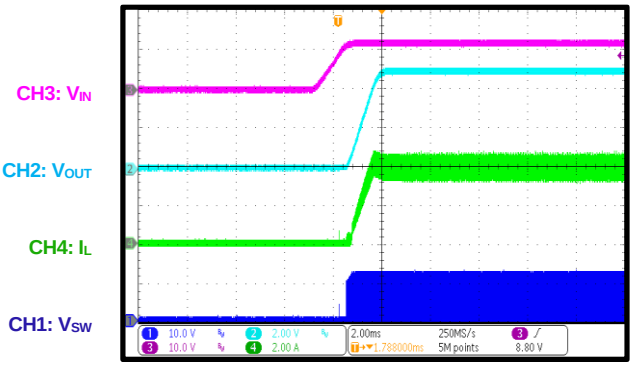
Start-Up through VIN
I_{OUT} = 0A, AAM mode



Start-Up through VIN
I_{OUT} = 0A, FCCM



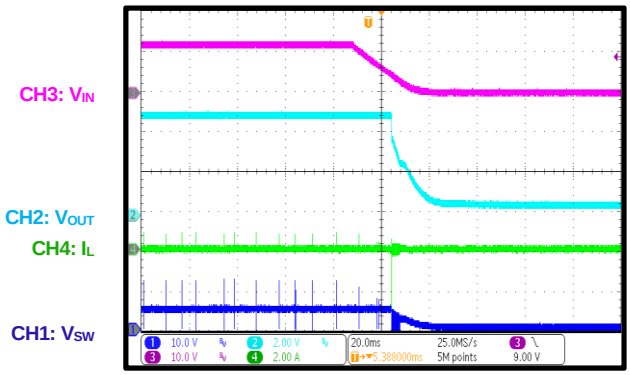
Start-Up through VIN
I_{OUT} = 4A



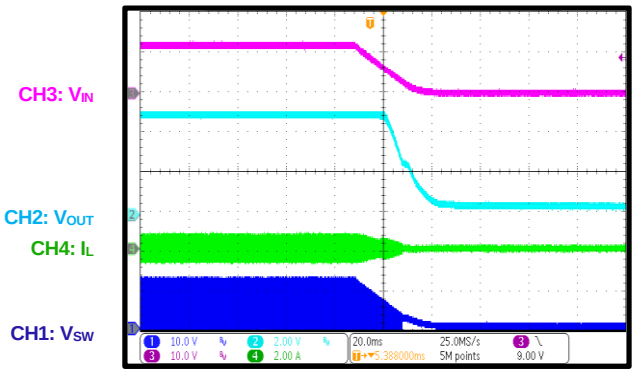
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, 1-phase, T_A = 25°C, unless otherwise noted.

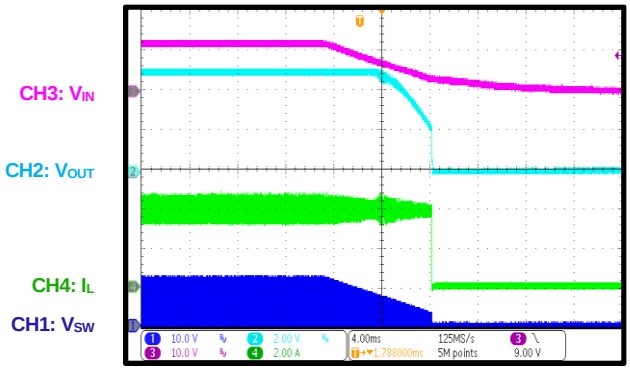
Shutdown through VIN
I_{OUT} = 0A, AAM mode



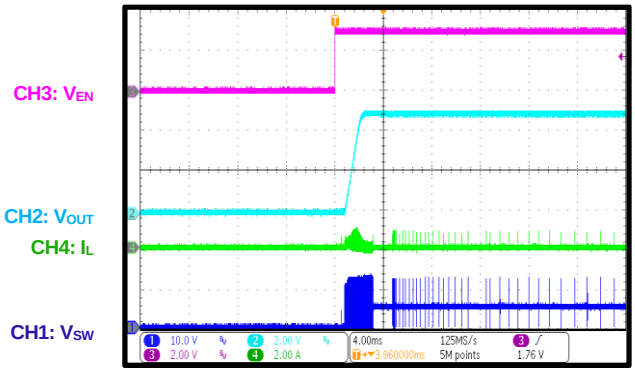
Shutdown through VIN
I_{OUT} = 0A, FCCM



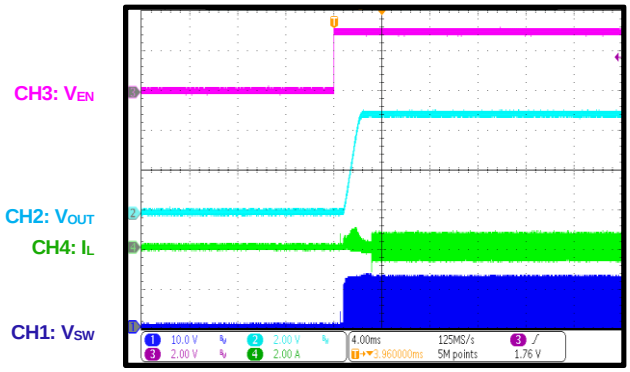
Shutdown through VIN
I_{OUT} = 4A



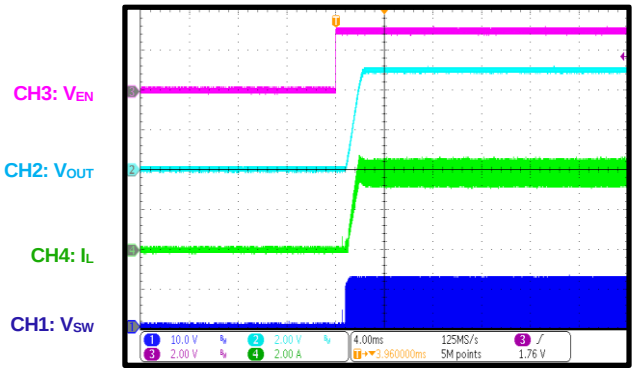
Start-Up through EN
I_{OUT} = 0A, AAM mode



Start-Up through EN
I_{OUT} = 0A, FCCM



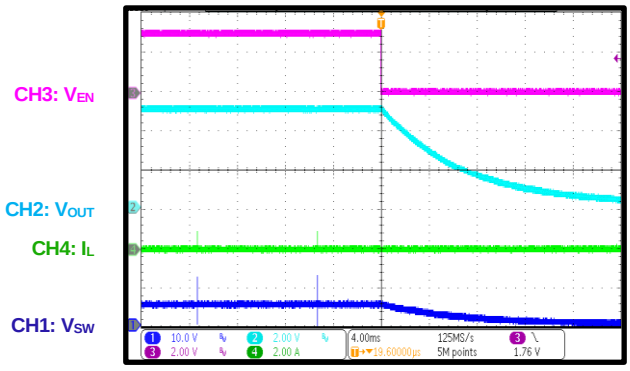
Start-Up through EN
I_{OUT} = 4A



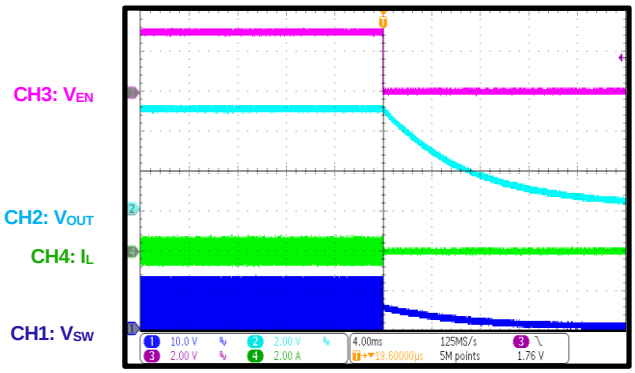
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, 1-phase, T_A = 25°C, unless otherwise noted.

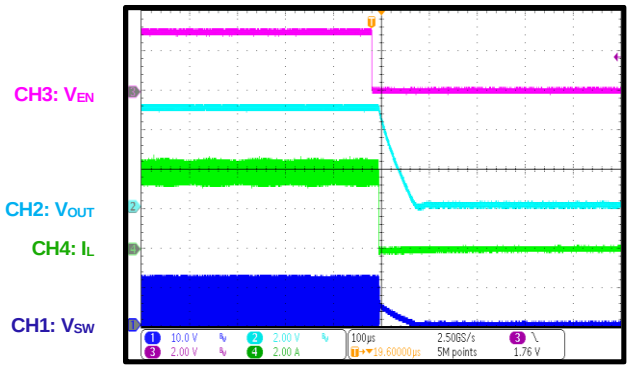
Shutdown through EN
I_{OUT} = 0A, AAM mode



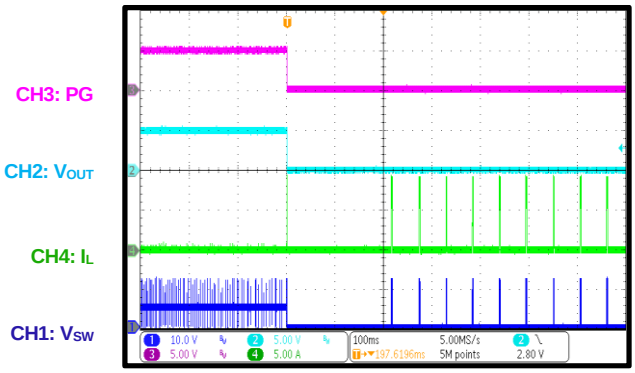
Shutdown through EN
I_{OUT} = 0A, FCCM



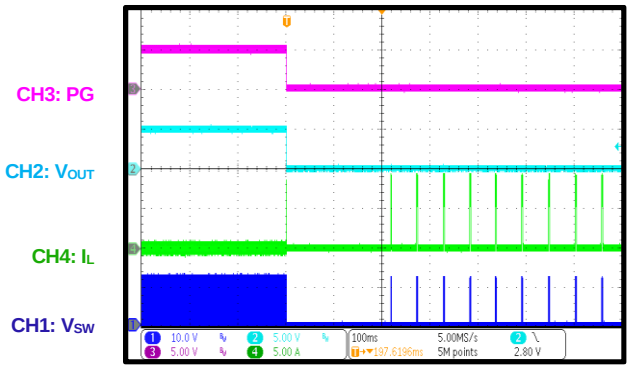
Shutdown through EN
I_{OUT} = 4A



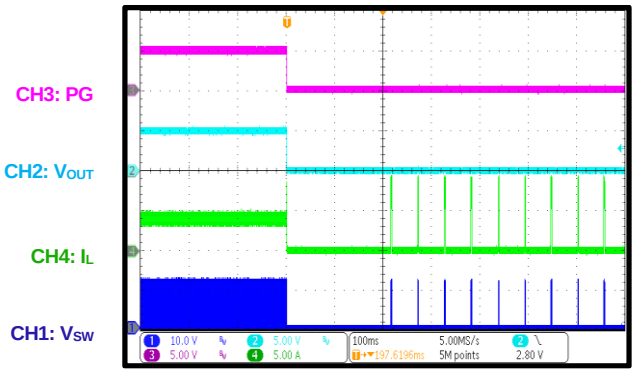
SCP Entry
I_{OUT} = 0A, AAM mode



SCP Entry
I_{OUT} = 0A, FCCM



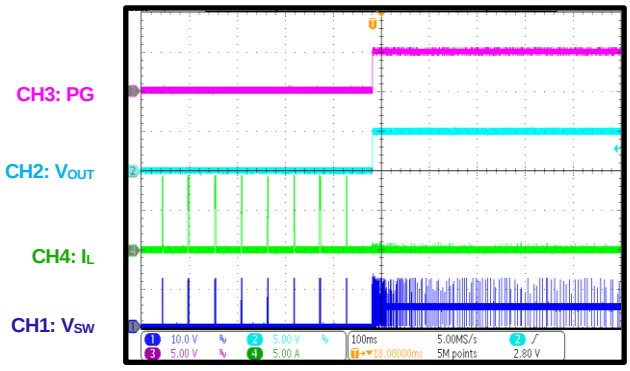
SCP Entry
I_{OUT} = 4A



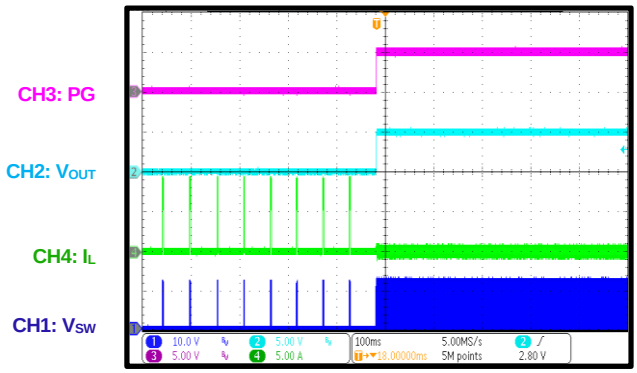
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, 1-phase, T_A = 25°C, unless otherwise noted.

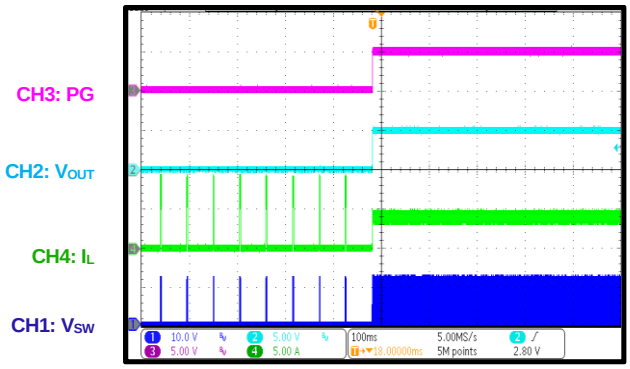
SCP Recovery
I_{OUT} = 0A, AAM mode



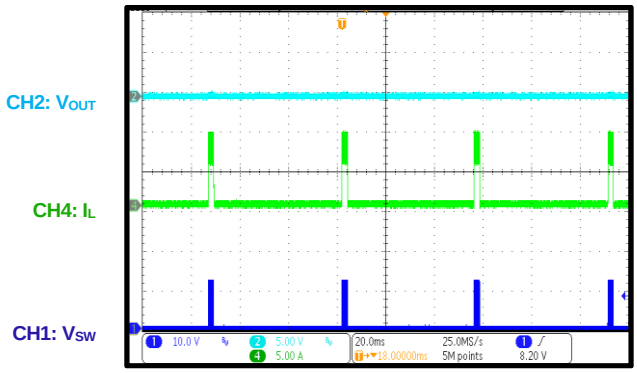
SCP Recovery
I_{OUT} = 0A, FCCM



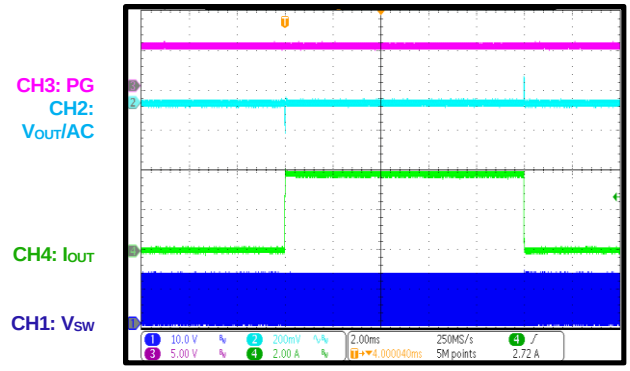
SCP Recovery
I_{OUT} = 4A



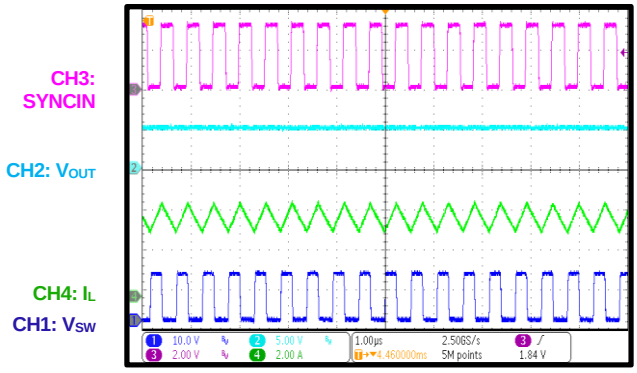
SCP Steady State



Load Transient
I_{OUT} = 0A to 4A, 1.6A/µs



SYNCIN Operation
I_{OUT} = 4A, f_{SW} = 2.2MHz,
SYNC frequency = 1.86MHz

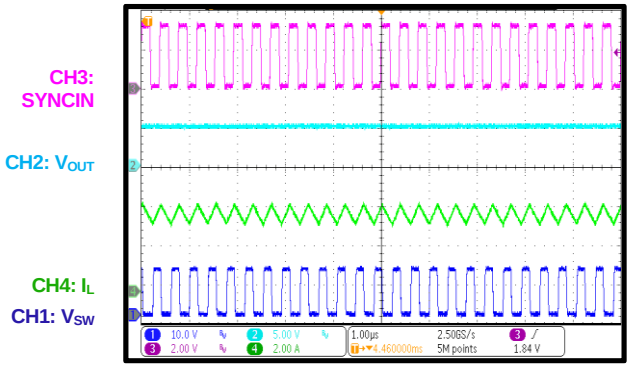


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, 1-phase, T_A = 25°C, unless otherwise noted.

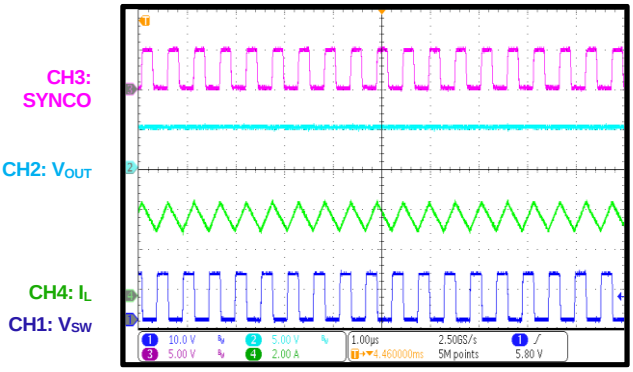
SYNCIN Operation

I_{OUT} = 4A, f_{SW} = 2.2MHz,
SYNC frequency = 2.6MHz



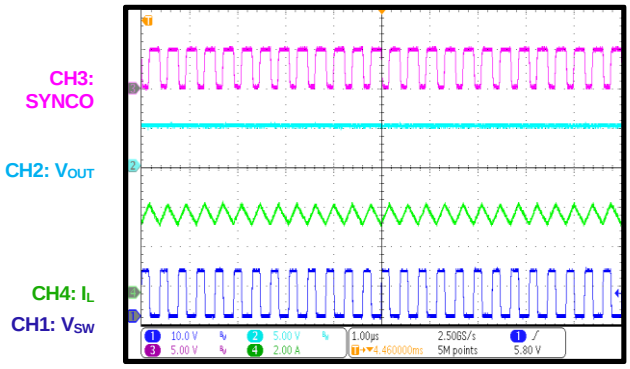
SYNCO Operation

I_{OUT} = 4A, f_{SW} = 2.2MHz,
SYNC frequency = 1.86MHz



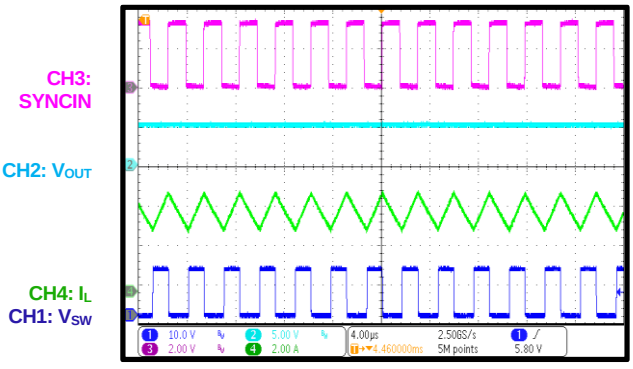
SYNCO Operation

I_{OUT} = 4A, f_{SW} = 2.2MHz,
SYNC frequency = 2.6MHz



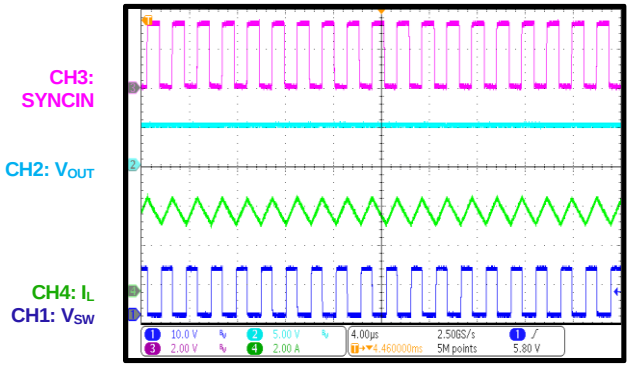
SYNCIN Operation

I_{OUT} = 4A, f_{SW} = 410kHz,
SYNC frequency = 340kHz



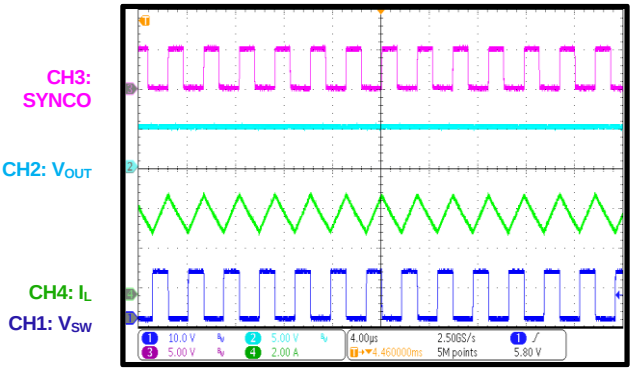
SYNCIN Operation

I_{OUT} = 4A, f_{SW} = 410kHz,
SYNC frequency = 480kHz



SYNCO Operation

I_{OUT} = 4A, f_{SW} = 410kHz,
SYNC frequency = 340kHz

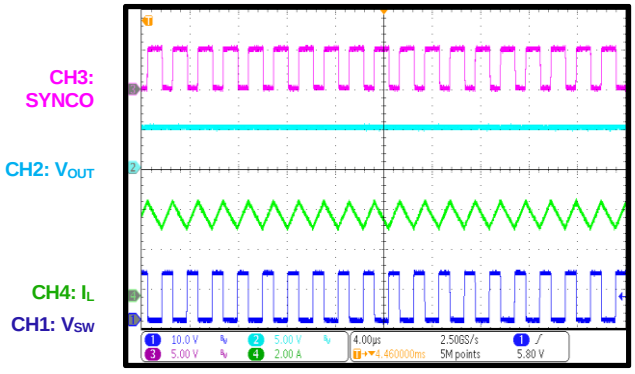


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, 1-phase, T_A = 25°C, unless otherwise noted.

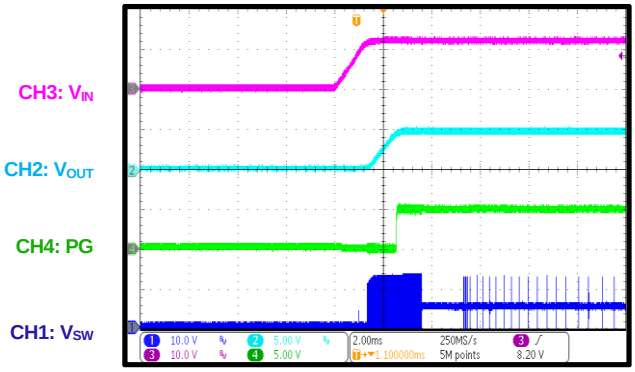
SYNCO Operation

I_{OUT} = 4A, f_{SW} = 410kHz,
SYNC frequency = 480kHz



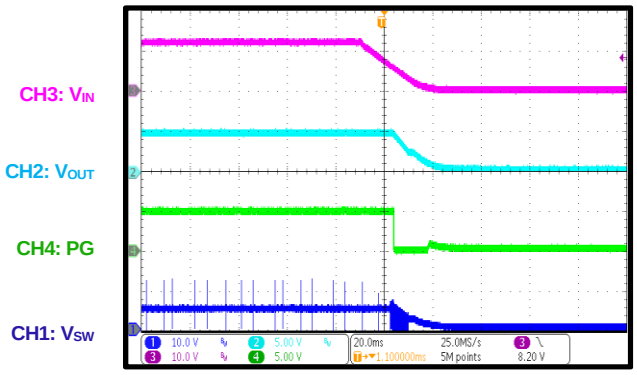
PG in Start-Up through VIN

I_{OUT} = 0A, AAM mode



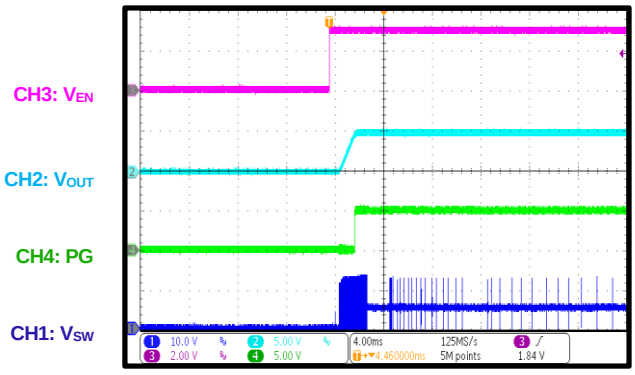
PG in Shutdown through VIN

I_{OUT} = 0A, AAM mode



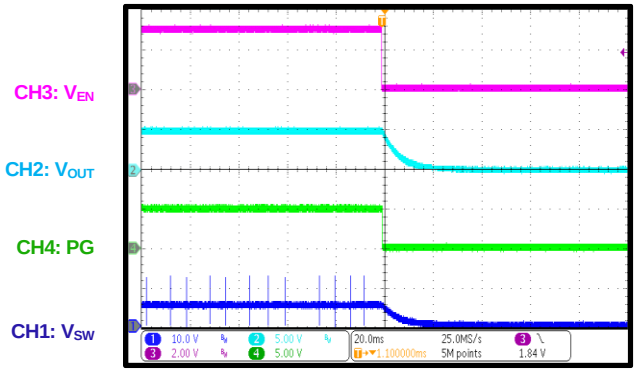
PG in Start-Up through EN

I_{OUT} = 0A, AAM mode



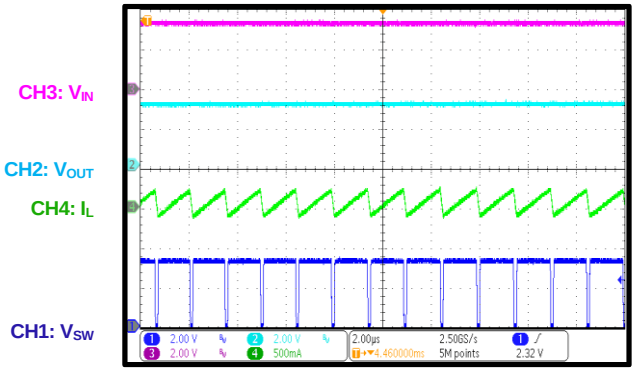
PG in Shutdown through EN

I_{OUT} = 0A, AAM mode



Low-Dropout Mode

V_{IN} = 3.3V, V_{OUT} set to 5V, I_{OUT} = 0A

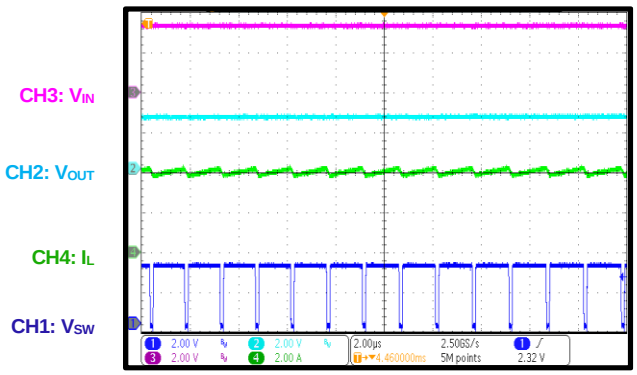


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, 1-phase, T_A = 25°C, unless otherwise noted.

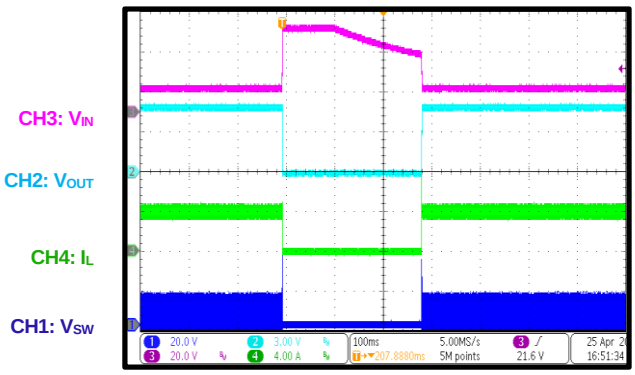
Low-Dropout Mode

V_{IN} = 3.3V, V_{OUT} set to 5V, I_{OUT} = 4A



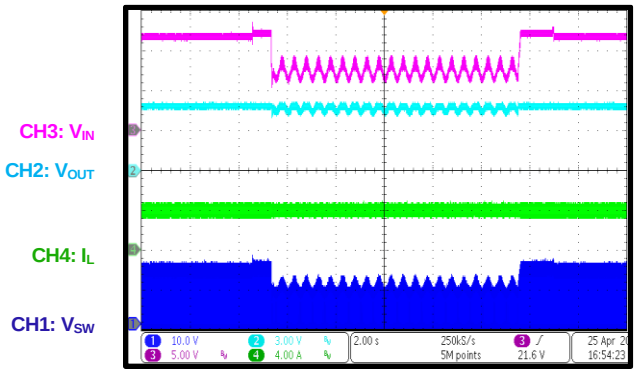
Load Dump

V_{IN} = 12V to 42V, I_{OUT} = 4A



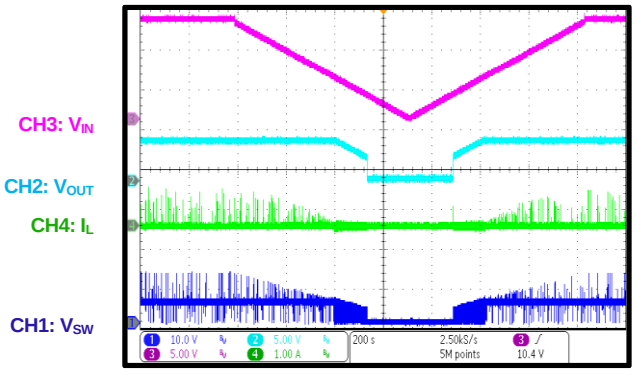
Cold Crank

I_{OUT} = 4A



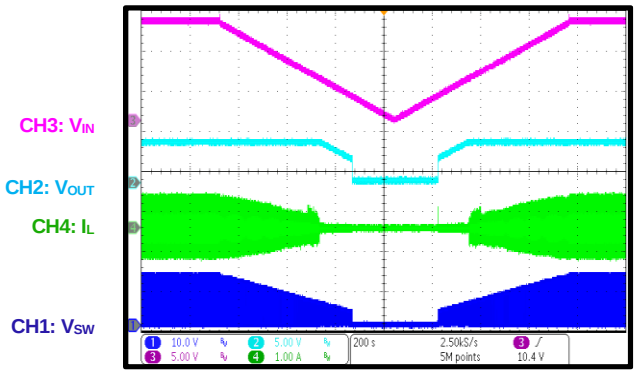
V_{IN} Ramping Up and Down

I_{OUT} = 0A, AAM mode



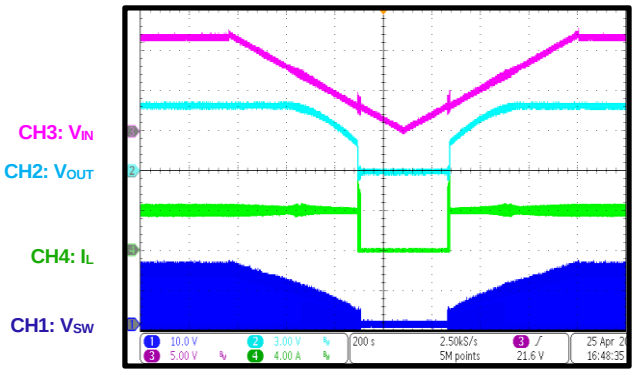
V_{IN} Ramping Up and Down

I_{OUT} = 0A, FCCM



V_{IN} Ramping Up and Down

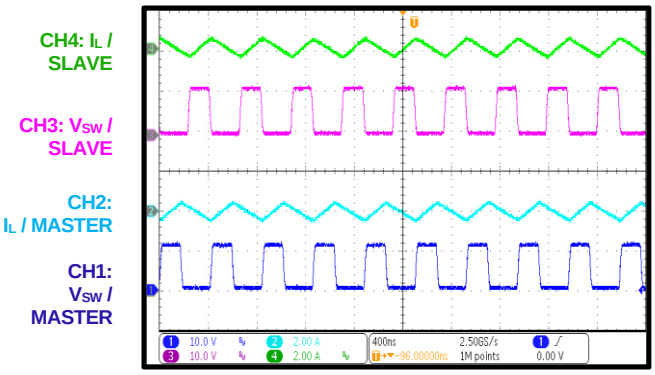
I_{OUT} = 4A



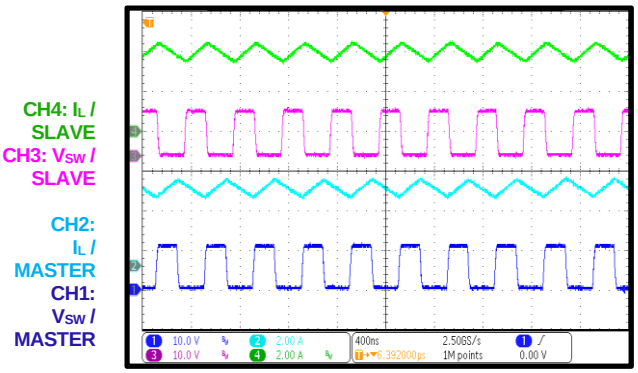
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, FCCM, 2-phase, T_A = 25°C, unless otherwise noted.

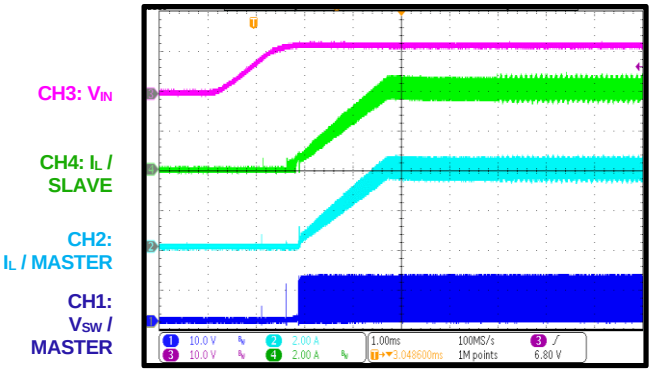
Steady State
I_{OUT} = 0A



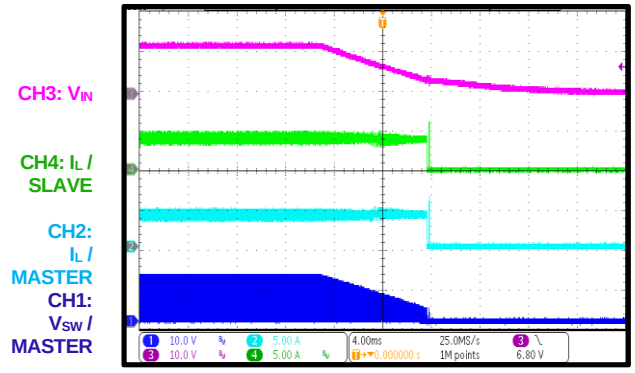
Steady State
I_{OUT} = 8A



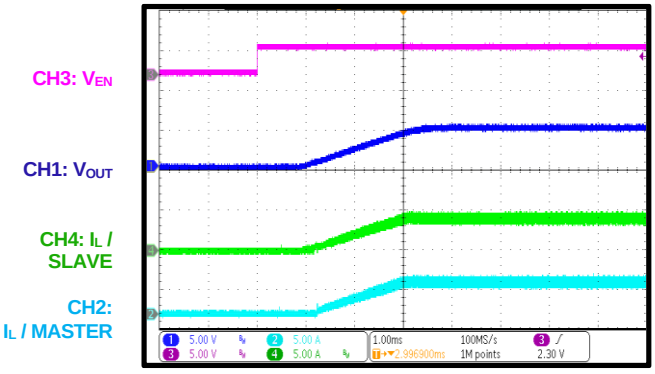
Start-Up through VIN
I_{OUT} = 8A



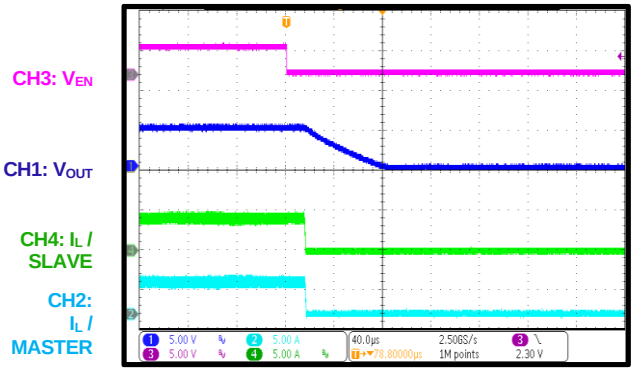
Shutdown through VIN
I_{OUT} = 8A



Start-Up through EN
I_{OUT} = 8A



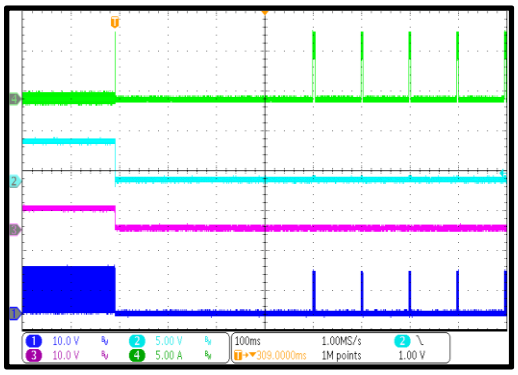
Shutdown through EN
I_{OUT} = 8A



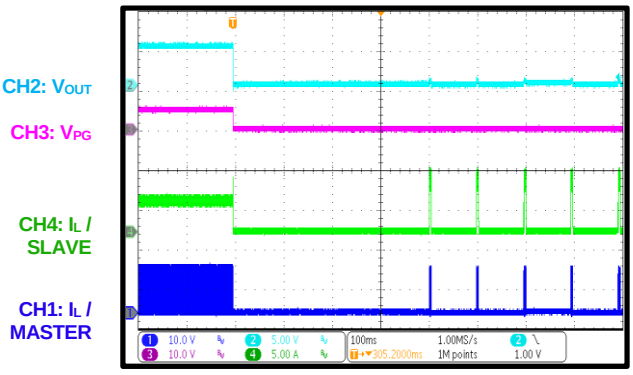
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, FCCM, 2-phase, T_A = 25°C, unless otherwise noted.

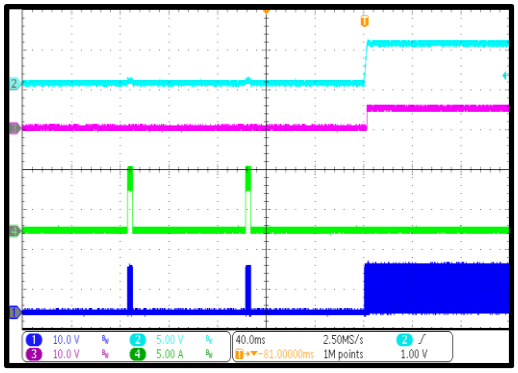
SCP Entry
I_{OUT} = 0A



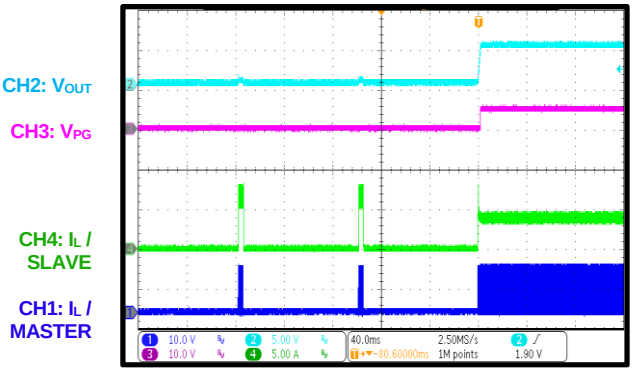
SCP Entry
I_{OUT} = 8A



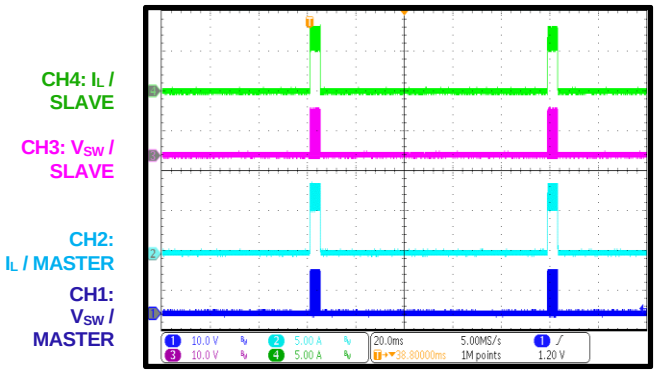
SCP Recovery
I_{OUT} = 0A



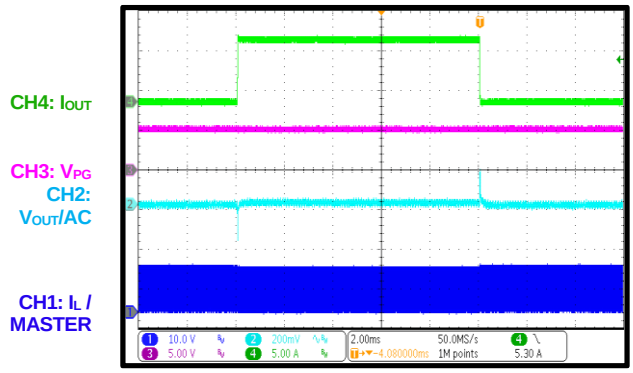
SCP Recovery
I_{OUT} = 8A



SCP Steady State



Load Transient
I_{OUT} = 0A to 8A, 1.6A/µs

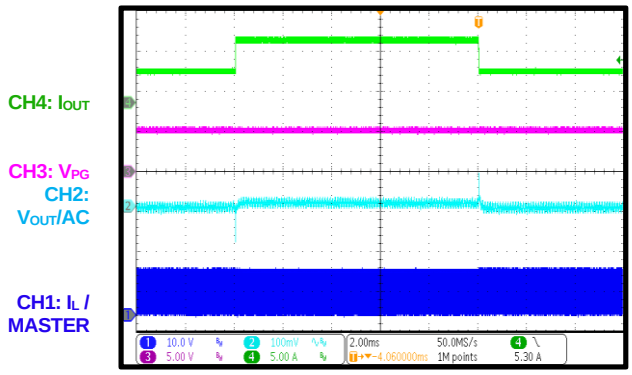


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, FCCM, 2-phase, T_A = 25°C, unless otherwise noted.

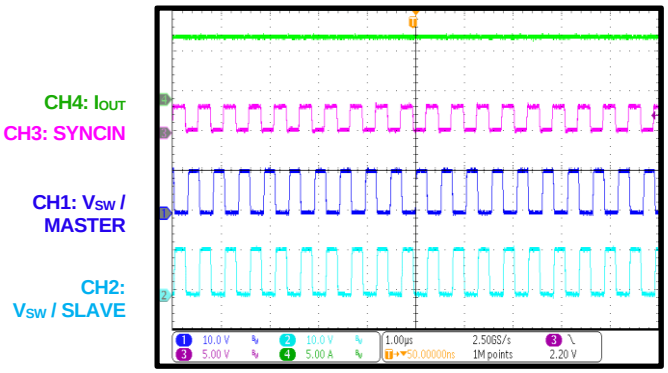
Load Transient

I_{OUT} = 4A to 8A, 1.6A/µs



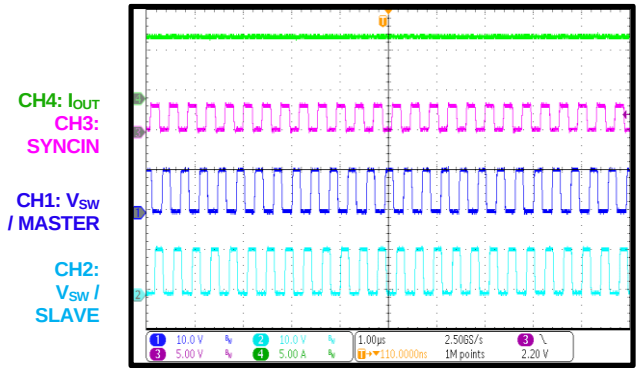
SYNCIN Operation

I_{OUT} = 8A, SYNC frequency = 1.9MHz



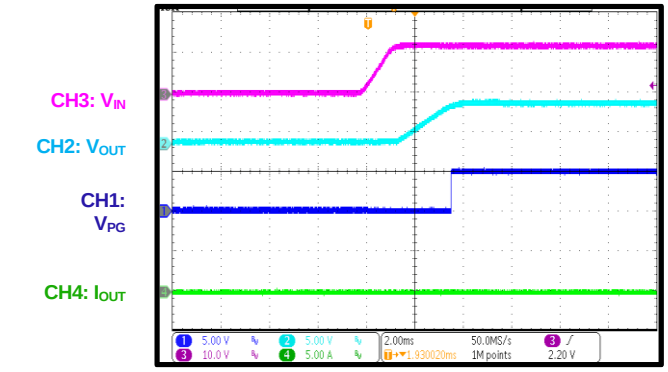
SYNCIN Operation

I_{OUT} = 8A, SYNC frequency = 2.6MHz



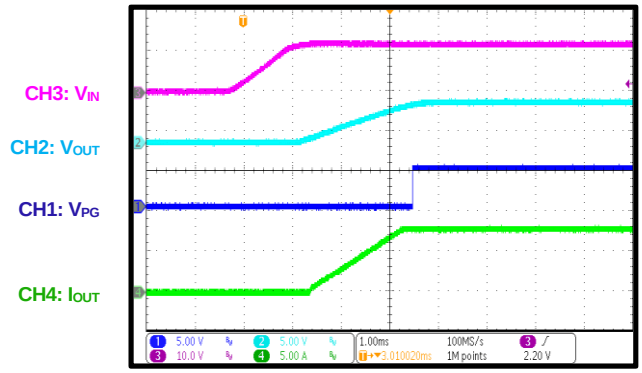
PG in Start-Up through VIN

I_{OUT} = 0A



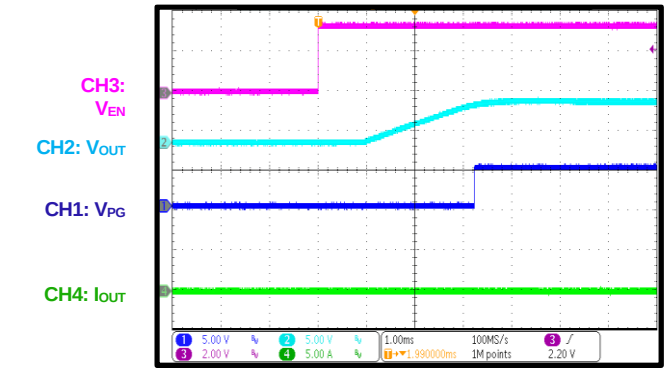
PG in Start-Up through VIN

I_{OUT} = 8A



PG in Start-Up through EN

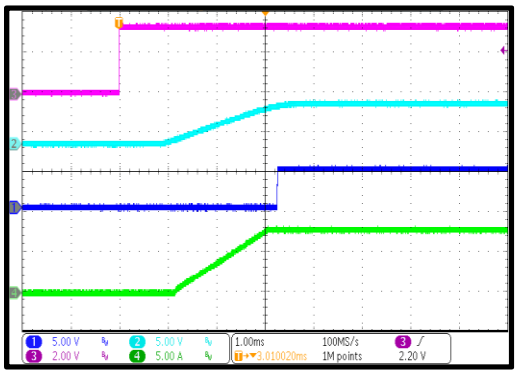
I_{OUT} = 0A



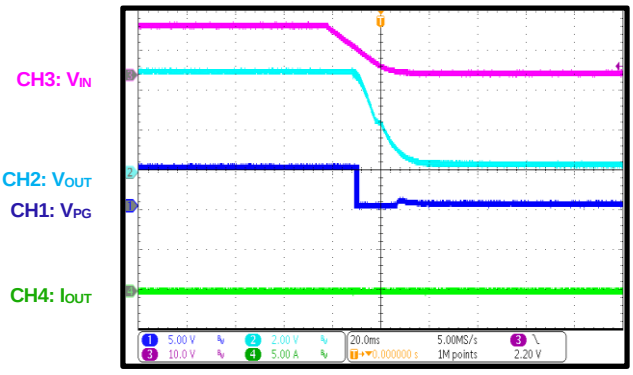
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, FCCM, 2-phase, T_A = 25°C, unless otherwise noted.

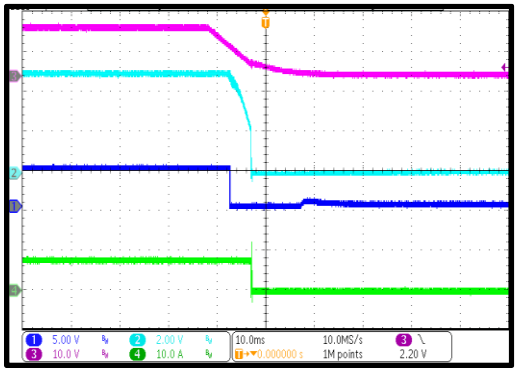
PG in Start-Up through EN
I_{OUT} = 8A



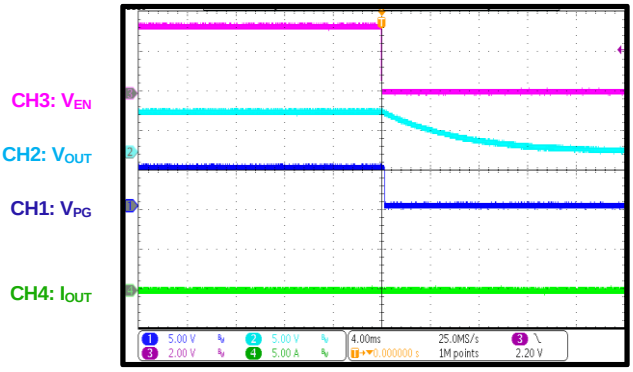
PG in Shutdown through VIN
I_{OUT} = 0A



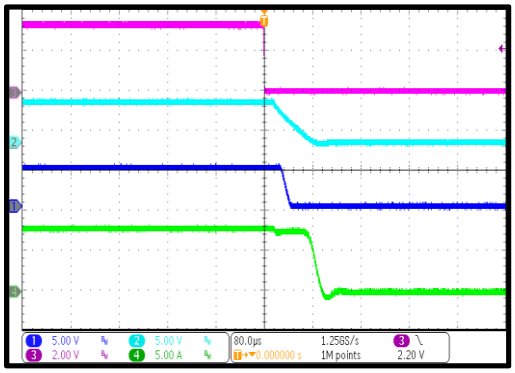
PG in Shutdown through VIN
I_{OUT} = 8A



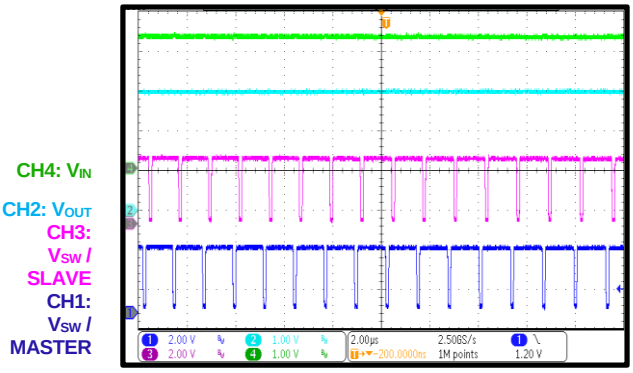
PG in Shutdown through EN
I_{OUT} = 0A



PG in Shutdown through EN
I_{OUT} = 8A



Low-Dropout Mode
V_{IN} = 3.3V, V_{OUT} set to 5V, I_{OUT} = 0A

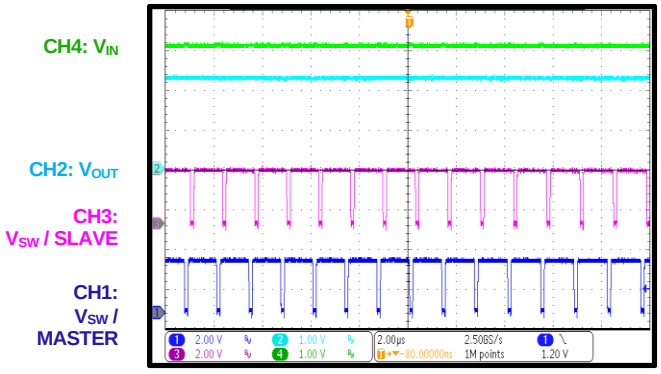


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, FCCM, 2-phase, T_A = 25°C, unless otherwise noted.

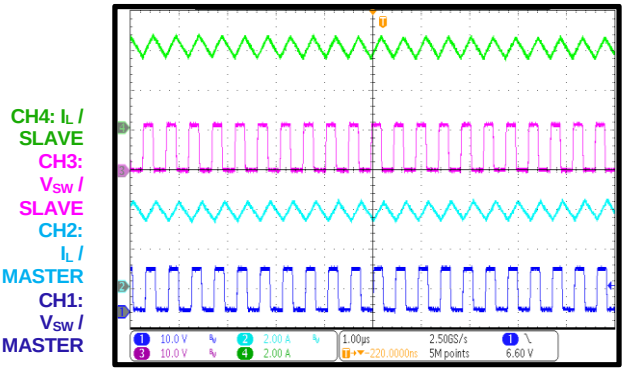
Low-Dropout Mode

V_{IN} = 3.3V, V_{OUT} set to 5V, I_{OUT} = 8A



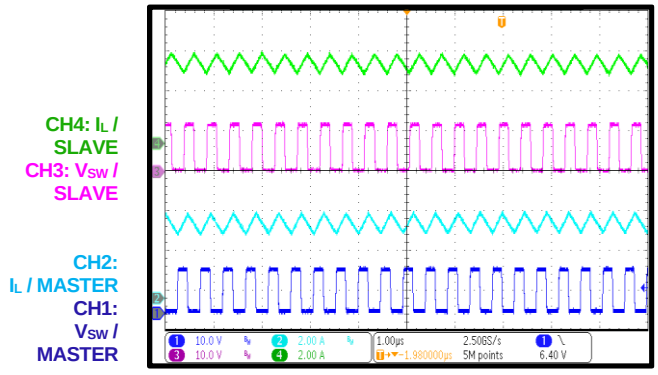
Phase Shift

I_{OUT} = 8A,
R_{FREQ} / SLAVE = 2 x R_{FREQ} / MASTER



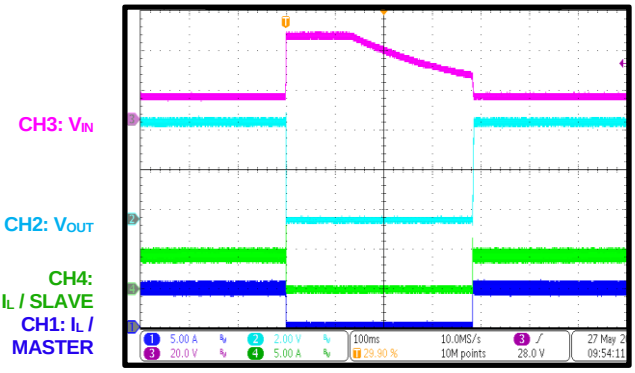
Phase Shift

I_{OUT} = 8A,
R_{FREQ} / SLAVE = 0.5 x R_{FREQ} / MASTER



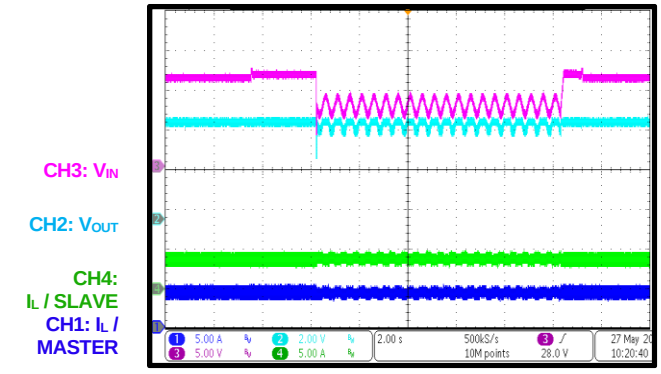
Load Dump

V_{IN} = 12V to 42V, I_{OUT} = 8A



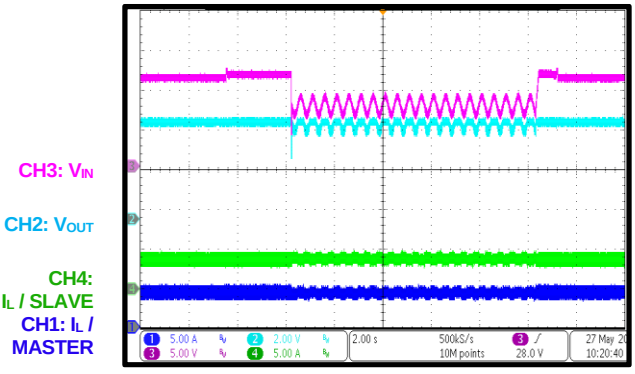
Cold Crank

I_{OUT} = 8A



V_{IN} Ramping Up and Down

I_{OUT} = 8A



FUNCTIONAL BLOCK DIAGRAM

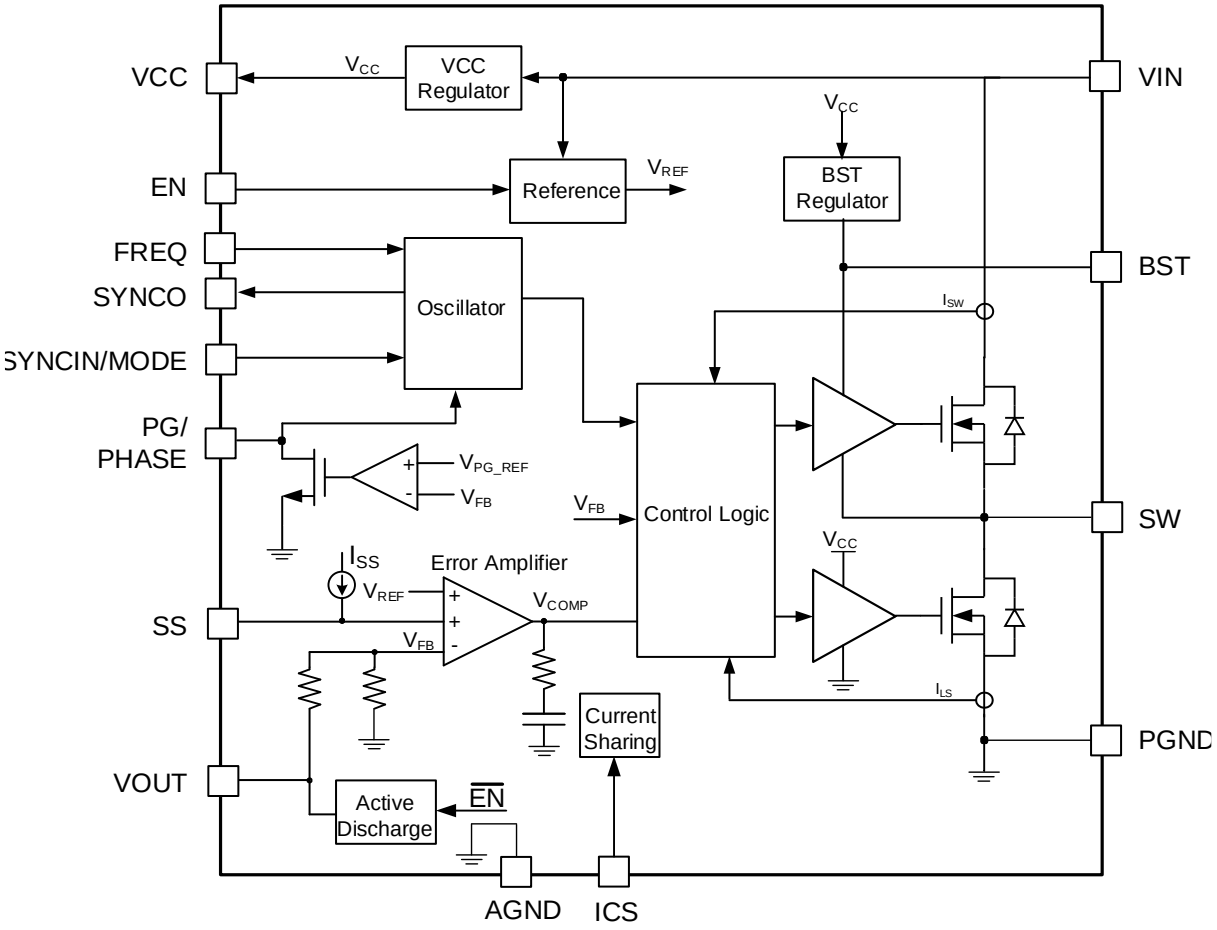


Figure 1: Functional Block Diagram

OPERATION

The MPQ4340/4340J is a synchronous, step-down switching converter with integrated internal high side and low side power MOSFETs (HS-FETs and LS-FETs, respectively). It provides up to 4A of highly efficient output current (I_{OUT}) with fixed-frequency, zero-delay pulse-width module (PWM) control.

The device features wide input voltage (V_{IN}) range, configurable 350kHz to 2.5MHz switching frequency (f_{SW}), external soft start, and precision current limiting. Its very low operational quiescent current (I_Q) makes the MPQ4340/4340J well-suited for battery-powered applications.

Zero-Delay Pulse-Width Modulation (PWM) Control (ZDP)

Automotive applications typically require fixed-frequency operation to reduce EMI, but traditional fixed-frequency control topologies have major limitations. Voltage mode is difficult to compensate in automotive environments, while peak current mode control struggles to keep up with stringent, modern system-on-chip (SoC) transient requirements without excessive output capacitance. With these requirements in mind, the MPQ4340/4340J introduces fixed-frequency zero-delay PWM control (ZDP).

ZDP combines current information with hysteretic-style output voltage (V_{OUT}) control in a clocked system. This provides near-optimal transient response, while maintaining a high phase margin across a wide variety of operating conditions and external component values. It also maintains superior EMI performance. The improved transient response reduces output capacitor requirements, lowering system cost. Trailing-edge modulation is used to facilitate a narrow minimum on-time (t_{ON_MIN}) for high conversion ratio applications.

At the beginning of the PWM cycle, the HS-FET turns off and the LS-FET turns on immediately, then remains on until the control signal reaches the COMP voltage (V_{COMP}). The HS-FET remains off for at least 120ns at the beginning of the cycle.

Light-Load Operation

At moderate to high output currents, the MPQ4340/4340J operates with a fixed frequency. Under light-load conditions, the device can work in two different operation modes by setting the state of the SYNCIN/MODE pin.

When the SYNCIN/MODE pin is pulled above 1.8V or an external clock is used, the MPQ4340/4340J works in forced continuous conduction mode (FCCM). In this mode, it works with a fixed frequency from no-load to full-load conditions. The part has a reverse current limit (about -4A) to prevent the negative current from dropping too low and potentially damaging the components. Once the negative inductor current (I_L) reaches the reverse current limit ($I_{LIMIT\_REVERSE}$), the HS-FET immediately turns on and the LS-FET turns off. The advantage of FCCM is its constant frequency and lower output voltage ripple at light loads.

When the SYNCIN/MODE pin is pulled below 0.4V, the MPQ4340/4340J works in advanced asynchronous modulation (AAM) mode. The device cannot enter AAM mode until soft start (SS) finishes. AAM mode optimizes efficiency under light-load and no-load conditions.

In AAM mode, the LS-FET emulates a diode and the HS-FET has a fixed one-shot on time to charge the inductor and keep V_{OUT} within regulation. As the load decreases, the interval between one-shots increases. When this interval exceeds 8µs, the part enters sleep mode which turns off some internal circuits and extends the on time to achieve an ultra-low I_Q. When the load increases and the interval becomes shorter than 6µs, the part exits sleep mode and re-enters AAM mode. During this mode, the part employs a zero-current detection (ZCD) circuit to turn off the LS-FET and prevent negative I_L flow at light loads. If the MODE pin goes high, the part exits AAM mode. If an over-voltage (OV) or over-temperature (OT) fault occurs in sleep mode, the internal circuits are not disabled.

Frequency Spread Spectrum (FSS)

The MPQ4340/4340J uses a 12kHz modulation frequency with fixed 128 steps triangular profile to spread the internal switching frequency (f_{SW}) across a 20% (±10%) window. The absolute frequency step size varies proportionally with f_{SW} to maintain the ±10% frequency spread (see Figure 2 on page 41).

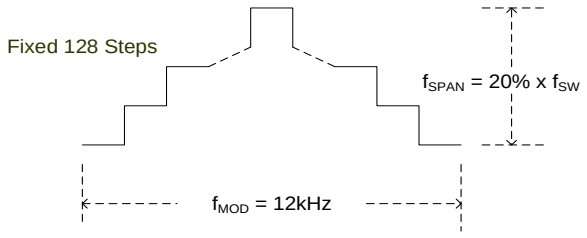


Figure 2: Frequency Spread Spectrum

Sidebands are created by modulating f_{SW} with the triangle modulation waveform. The emission power of the fundamental f_{SW} and its harmonics is distributed into smaller pieces, which significantly reduces the peak EMI noise.

Low-Dropout (LDO) Mode

When V_{IN} drops to about 7V, the MPQ4340/4340J folds back the frequency. When V_{IN} is almost equal to V_{OUT}, the IC enters low-dropout (LDO) mode.

The effective duty cycle during the regulator's dropout period is mainly influenced by the voltage drops across the MOSFET, the inductor resistance, the low-side diode, and the PCB resistance.

Start-Up and Shutdown

If both V_{IN} and the EN voltage (V_{EN}) exceed their respective thresholds, the device starts up. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

While the internal supply rail is up, an internal timer holds the MOSFET off for about 50µs to blank any start-up glitches. When the SS block is enabled, it first holds its SS output low to ensure the remaining circuits are ready, then slowly ramps up.

Three events can shut down the chip: EN going low, V_{IN} going low, and thermal shutdown. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. Then V_{COMP} and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

SYNCIN and SYNCO

f_{SW} can be synchronized to the rising edge of a clock signal applied to the SYNCIN/MODE pin. The recommended SYNCIN frequency range is between 90% and 115% of f_{SW}.

The SYNCO pin can output a clock signal in phase with the internal oscillator when there is no SYNCIN signal, or it can output a clock signal in phase with SYNCIN if an external clock signal is applied at SYNCIN (see Figure 3). This makes enabling a dual-phase, interleaved configuration easy (see Figure 4).

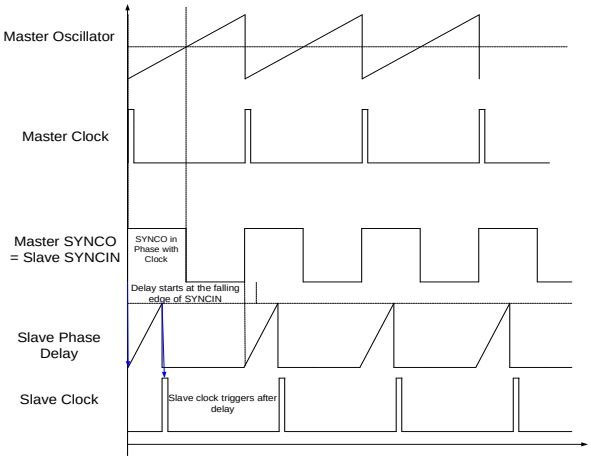


Figure 3: SYNCIN and SYNCO Scheme

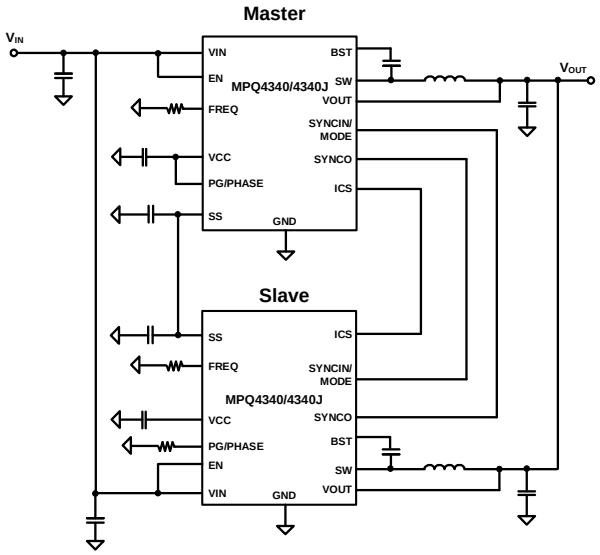


Figure 4: 2-Phase Configuration

For multi-phase applications, the VOUT and ICS pins of the chips in parallel must be connected together, respectively (see Figure 5). Connect the SYNCO pin of the master device to the SYNCIN/MODE pins of the slave devices being interleaved. The SYNCO pins of the slaves can be tied to the SYNCIN/MODE pin of the master device to select the mode of the slave devices. Place a resistor to AGND near the PG/PHASE pin of each slave to set the phase delay, enabling simple multi-phase operation. Short the PG/PHASE pin of the slave devices to set no delay on the SYNCIN signal.

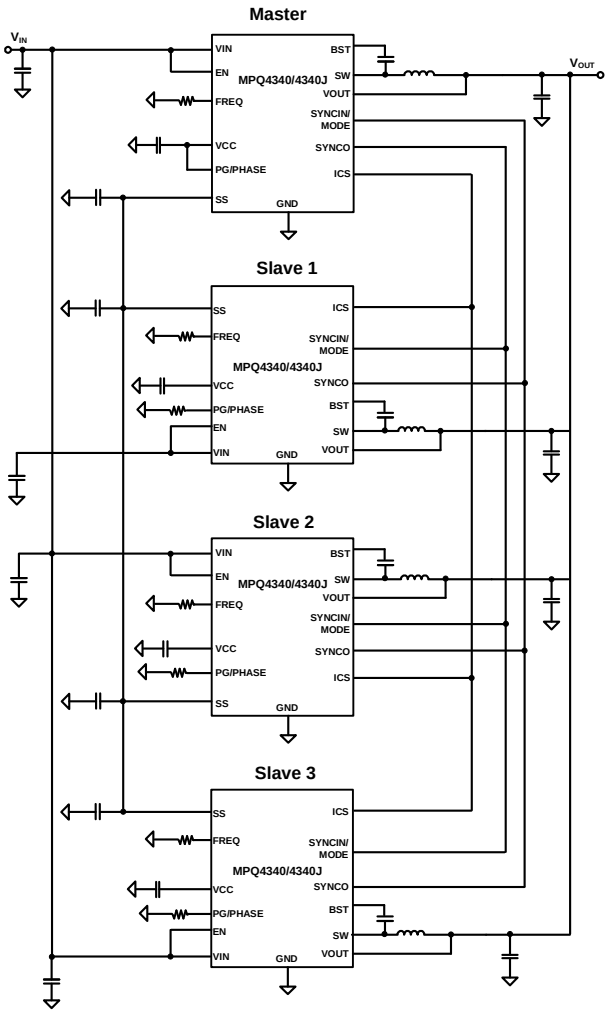


Figure 5: 4-Phase Configuration

Thermal Shutdown

Thermal shutdown is implemented to protect the chip from thermal runaway. When the silicon die temperature exceeds its upper threshold (170°C), the power MOSFETs shut down. Once the temperature drops below its lower threshold (150°C), the thermal shutdown condition is removed and the chip starts up again.

APPLICATION INFORMATION

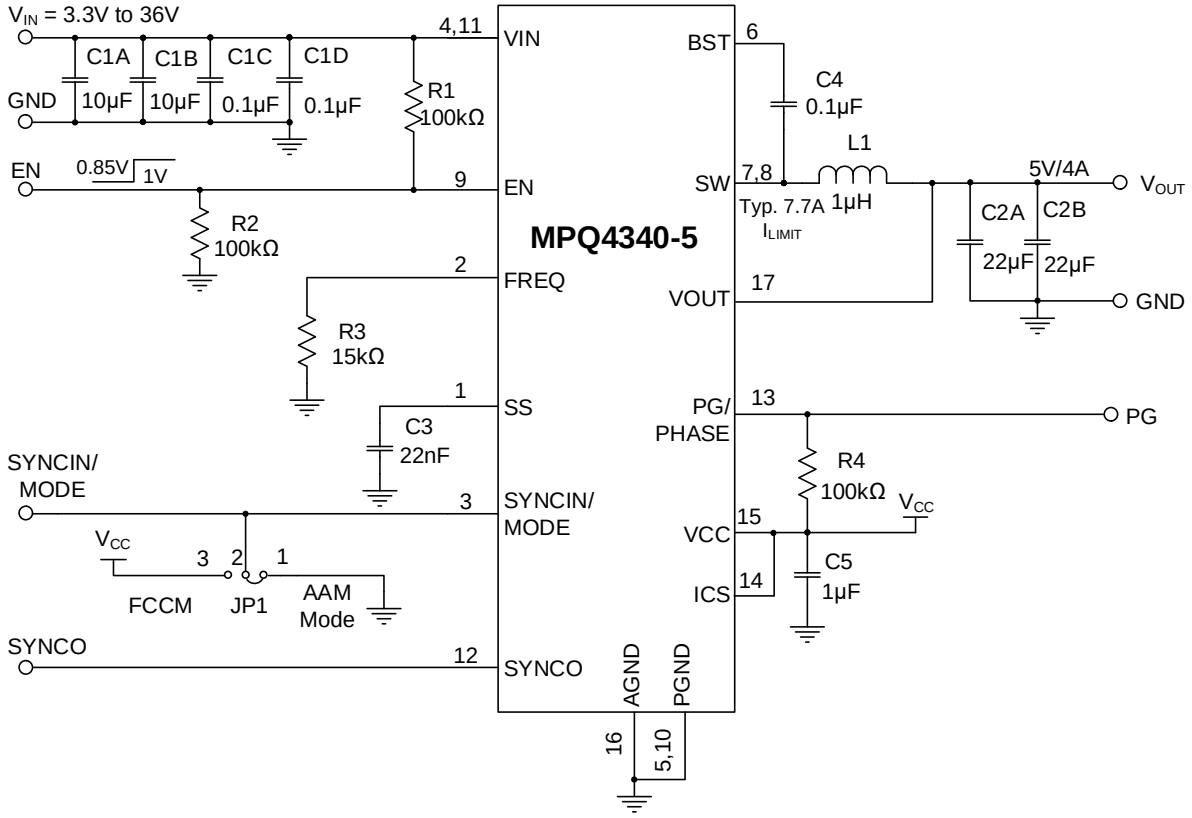


Figure 6: Typical Application Circuit for the MPQ4340GLE-5 (V_{OUT} = 5V, f_{SW} = 2.2MHz)

Table 1: Design Guide Index

Pin #	Pin Name	Component	Design Guide Index
1	SS	C3	Selecting the Soft-Start Capacitor (SS, Pin 1)
2	FREQ	R3	Setting the Switching Frequency (f_{SW}) (FREQ, Pin 2)
3	SYNCIN/MODE	-	SYNC Input and MODE Selection (SYNCIN/MODE, Pin 3)
4, 11	VIN	C1A, C1B, C1C, C1D	Selecting the Input Capacitors (VIN, Pins 4 and 11)
5, 10	PGND	-	GND Connection (GND, Pins 5, 10, and 16)
6	BST	C4	Floating Driver and Bootstrap Charging (BST, Pin 6)
7, 8	SW	L1, C2A, C2B	Selecting the Inductor (SW, Pins 7 and 8) Selecting the Output Capacitors (SW, Pins 7 and 8)
9	EN	R1, R2	Enable and V_{IN} Under-Voltage Lockout (UVLO) (EN, Pin 9)
12	SYNCO	-	SYNCO (Pin 12)
13	PG/PHASE	R4	Power Good (PG) Indicator and Phase Shift (PG/PHASE, Pin 13)
14	ICS	-	Current Sharing (ICS, Pin 14)
15	VCC	C5	Input Bias Supply (VCC, Pin 15)
16	AGND	-	GND Connection (GND, Pins 5, 10, and 16)
17	VOUT	-	VOUT (Pin 17)

Selecting the Soft-Start Capacitor (SS, Pin 1)

Soft start (SS) is implemented to prevent the converter's V_{OUT} from overshooting during start-up.

When SS begins, an internal current source begins charging the external SS capacitor (C_{SS}). When the SS voltage (V_{SS}) is below the internal reference voltage (V_{REF}), V_{SS} overrides V_{REF}, so the error amplifier (EA) uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, V_{REF} regains control.

C_{SS} can be calculated with Equation (1):

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} = 16.6 \times t_{SS}(ms) \quad (1)$$

The SS pin can be used for tracking and sequencing.

Setting the Switching Frequency (f_{SW}) (FREQ, Pin 2)

f_{SW} can be configured by an external resistor connected from the FREQ pin to ground, placed as close to the device as possible.

The resistance that sets f_{SW} (R3) can be selected using the f_{SW} vs R_{FREQ} curves. Figure 7 shows the f_{SW} vs. R_{FREQ} curve when f_{SW} is between 1000kHz and 2500kHz.

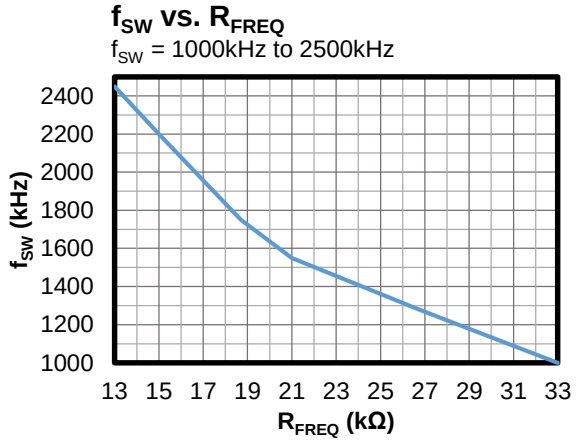


Figure 7: f_{SW} vs. R_{FREQ}

Figure 8 shows the f_{SW} vs. R_{FREQ} curve when f_{SW} is between 350kHz and 1000kHz.

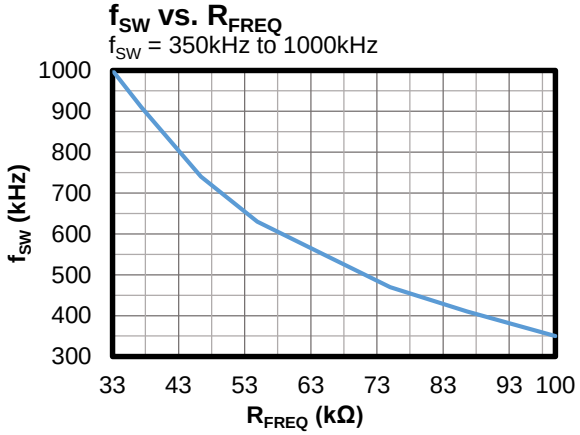


Figure 8: f_{SW} vs. R_{FREQ}

Table 2 shows some common f_{SW} and R_{FREQ} values when selecting f_{SW} .

Table 2: f_{SW} vs. R_{FREQ}

R_{FREQ} (kΩ)	f_{SW} (kHz)
100	350
86.6	410
75	470
64.9	550
54.9	630
46.4	740
37.4	910
33	1050
26.7	1280
21	1550
18.7	1750
15	2200
13	2450

SYNC Input and MODE Selection (SYNCIN/MODE, Pin 3)

When the SYNCIN/MODE pin is used as the SYNC input pin (SYNCIN), f_{SW} can be synchronized to the rising edge of a clock signal applied to SYNCIN/MODE. The recommended SYNCIN frequency range is 90% to 115% of f_{SW}.

When SYNCIN/MODE is used for mode selection (MODE), pulling this pin high allows the device to operate in FCCM, while pulling it low allows the device to operate in AAM mode (see Table 3 on page 45).

Table 3: Mode Selection

SYNCIN/MODE Input	Operation Mode
<0.4V	AAM mode
>1.8V	FCCM
External clock in	FCCM

Selecting the Input Capacitor (VIN, Pins 4 and 11)

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC V_{IN}. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, it is recommended to use a 4.7µF to 10µF capacitor. It is strongly recommended to use another, lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and GND as possible.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current for C_{IN} (I_{CIN}) can be estimated with Equation (2):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (2)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (3):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (3)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input.

The input voltage ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (4):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

When V_{IN} is above 25V, the device allows the V_{IN} OVP circuit to turn on. See the V_{IN} Over-Voltage Protection (OVP) section on page 48 for more details.

GND Connection (Pins 5, 10, and 16)

See the PCB Layout Guidelines section on page 49 for more details.

Floating Driver and Bootstrap Charging (BST, Pin 6)

The bootstrap (BST) capacitor (C4) is recommended to be between 0.1µF and 0.22µF.

It is not recommended to place a resistor (R_{BST}) in series with the BST capacitor (C_{BST}) unless there is a strict EMI requirement. R_{BST} helps enhance EMI performance and reduce voltage stress at high input voltages, but it also increases power consumption and reduces efficiency. When R_{BST} is necessary, it should be below 10Ω.

C_{BST} is charged and regulated to about 5V by the dedicated internal BST regulator. When the voltage between the BST and SW nodes is below its regulation, an N-channel MOSFET pass transistor connected from VCC to BST turns on to charge C_{BST}. The external circuit should provide sufficient voltage headroom to facilitate charging.

When the HS-FET is on, the BST voltage (V_{BST}) exceeds V_{CC}, so C_{BST} cannot be charged.

At higher duty cycles, the time available for bootstrap charging is shorter, so C_{BST} may not be sufficiently charged. If the external circuit has both insufficient voltage and time to charge C_{BST}, use additional external circuitry to ensure V_{BST} remains within the normal operation range.

Selecting the Inductor (SW, Pins 7 and 8)

A 1µH to 10µH inductor with a DC current rating at least 25% greater than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical size,

higher series resistance, and lower saturation current. A good rule for determining the inductor value is to allow the inductor ripple current to be approximately 30% of the maximum load current. The inductance value can be calculated with Equation (5):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum peak inductor current (I_{LP}) can be calculated with Equation (6):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

Selecting the Output Capacitor (SW, Pins 7 and 8)

The output capacitor (C_{OUT}) maintains the DC V_{OUT}. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep the output voltage ripple (ΔV_{OUT}) low. ΔV_{OUT} can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (7)$$

Where L is the inductance, and R_{ESR} is the equivalent series resistance (ESR) value of C_{OUT}.

For ceramic capacitors, the capacitance dominates the impedance at f_{SW} and causes the majority of ΔV_{OUT}. For simplification, ΔV_{OUT} can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (9)$$

The C_{OUT} characteristics also affect the stability of the regulation system. The part can be optimized for a wide range of capacitances and ESR values.

Enable and V_{IN} Under-Voltage Lockout (UVLO) (EN, Pin 9)

EN is a digital control pin that turns the regulator on and off.

Enabled by External Logic High/Low Signal

When the EN voltage (V_{EN}) reaches about 0.7V, the VCC supply turns on. When V_{IN} exceeds 2.7V, it provides an accurate reference voltage for the EN threshold. Forcing EN above its 1V rising threshold turns on the device. Driving EN below 0.85V turns off the device.

Configurable V_{IN} Under-Voltage Lockout (UVLO)

When V_{IN} is sufficiently high, the chip can be enabled and disabled via the EN pin. An internal pull-down resistor in this circuit can generate a configurable V_{IN} under-voltage lockout (UVLO) and hysteresis.

The device requires a higher voltage (≥3.3V) for V_{IN} to directly start up. The part has an internal, fixed UVLO threshold. The rising threshold is 3V, while the falling threshold is about 2.8V. For applications that require a higher UVLO point, an external resistor divider placed between VIN and EN can raise the equivalent UVLO threshold (see Figure 9).

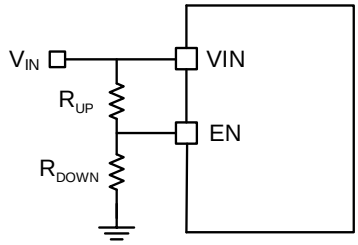


Figure 9: Adjustable UVLO Using EN Divider

The UVLO rising threshold ($V_{IN\_UVLO\_RISING}$) can be calculated with Equation (10):

$$V_{IN\_UVLO\_RISING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN\_RISING} \quad (10)$$

The UVLO falling threshold ($V_{IN\_UVLO\_FALLING}$) can be calculated with Equation (11):

$$V_{IN\_UVLO\_FALLING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN\_FALLING} \quad (11)$$

Where V_{EN_RISING} is 1V, and $V_{EN\_FALLING}$ is 0.85V.

SYNCO (Pin 12)

During start-up, the MPQ4340/4340J checks the SYNCO pin's status to confirm whether the part is intended to operate in master or slave mode. If the SYNCO is in a high-impendence (Hi-Z) state, the part acts as a master; if not, the part acts as a slave device.

If the part is operating as a master, SYNCO can be left floating. When operating as a master, SYNCO outputs a clock signal in phase with the internal oscillator signal or the external SYNCIN clock.

If SYNCO is connected to AGND, external voltage, or an external clock, the part operates as a slave device. In this mode, SYNCO can be pulled high or low to select the mode.

Power Good (PG) Indicator and Phase Shift (PG/PHASE, Pin 13)

When operating as a master device, the value of the power good (PG) resistor (R4, also called R_{PG}) is recommended to be about 100kΩ. The device includes an open-drain power good (PG) output that indicates whether the regulator's output is within its nominal V_{OUT} range. If using PG, connect it to a logic high power source (e.g. 3.3V) via a pull-up resistor. If the V_{OUT} is within 94% to 106% of its nominal voltage, PG goes high. If V_{OUT} exceeds 107% or is below 93% of its nominal voltage, PG goes low. Float PG if it is not used.

When operating as a slave device, the PG/PHASE pin can be used to set the phase shift by connecting R_{PG} to AGND. The phase shift phase can be calculated using Equation (12):

$$\text{Phase Shift} = \frac{RPG}{R_{FREQ}} \times 180° \quad (12)$$

Current Sharing (ICS, Pin 14)

The ICS pin's voltage exceeds 2.4V, current sharing is disabled. Connect this pin to VCC to disable current sharing for single-phase applications.

For multi-phase applications, connect the ICS pins of the devices in parallel.

Setting the VCC Capacitor (VCC, Pin 15)

Most of the internal circuitry is powered by the internal, 5V VCC regulator. This regulator uses V_{IN} as its input and operates across the full V_{IN} range. When V_{IN} exceeds 5V, V_{CC} is in full regulation. When V_{IN} is below 5V, the output V_{CC} degrades.

The VCC capacitor (C_{VCC}) should have a capacitance at least 10 times greater than the boost capacitor, and at least 1µF nominally. A C_{VCC} above 68µF nominal is not recommended.

VOUT (Pin 17)

Because the feedback resistor divider is integrated internally, connect the VOUT pin directly to the output (see Figure 10).

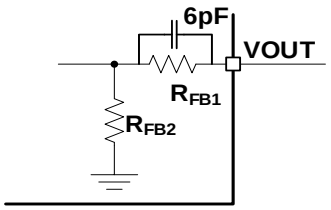


Figure 10: Feedback Divider Network for Fixed-Output Version

The following fixed outputs can be selected: 1V, 1.1V, 1.8V, 2.5V, 3V, 3.3V, 3.8V, or 5V.

Table 4 shows the relationship between the internal R_{FB} and V_{OUT}.

Table 4: R_{FB} vs. V_{OUT}

V_{OUT} (V)	R_{FB1} (MΩ)	R_{FB2} (MΩ)
1	1.33	2
1.1	1.67	2
1.8	4	2
2.5	6.33	2
3	8	2
3.3	9	2
3.8	10.67	2
5	14.67	2

Peak and Valley Current Limits

Both the HS-FET and LS-FET have cycle-by-cycle current-limit protection. If the inductor current (I_L) reaches the high-side (HS) peak current limit (typically 7.7A) or the rising edge of the internal clock is reached while the current is rising and the HS-FET is on, then the HS-FET is forced off immediately to prevent the current from rising further. When the LS-FET is on, the valley current limit circuit block the PWM from

turning on the HS-FET until I_L returns to below the low-side (LS) valley current limit (typically 5.9A). This current limit scheme prevents current runaway if an overload or short-circuit event occurs.

Short-Circuit Protection (SCP)

If the output is shorted to ground, V_{OUT} drops below 70% of its nominal output, and the LS-FET current exceeds the 5.9A valley current limit, then the IC turns on the LS-FET until I_L is fully discharged. The device also begins slowly discharging C_{SS}. Once C_{SS} is fully discharged, the device restarts with a full SS. This hiccup process repeats until the fault is removed.

Output Over-Voltage Protection (OVP) and Discharge

There is an internal V_{OUT} OVP circuit. If the device is operating in discontinuous conduction mode (DCM) and V_{OUT} exceeds 106% of the target voltage, an output discharge path from VOUT to PGND is activated to discharge V_{OUT}. The output discharge path remains activated until V_{OUT} returns to its regulated value, at which point the device begins switching.

If the device is operating in FCCM and V_{OUT} exceeds 106% of the target voltage, the output discharge path turns on. If the negative current limit is triggered 265 times, the part enters hiccup mode and switching stops. Once V_{OUT} drops to or below 105% of the target value, a new SS cycle begins. The V_{OUT} discharge path remains on until V_{OUT} returns to its regulated value, at which point the device begins switching.

V_{IN} Over-Voltage Protection (OVP)

The MPQ4340/4340J has a built-in V_{IN} over-voltage protection (OVP) circuit. V_{IN} OVP becomes active at 25V. When V_{IN} exceeds the OVP threshold (typically 38V), the LS-FET turns on until I_L is fully discharged, and then switching stops. When V_{IN} drops to the over-voltage (OV) falling threshold (typically 28V) and the hiccup restart delay time expires, the device completes a SS cycle and resumes normal regulation.

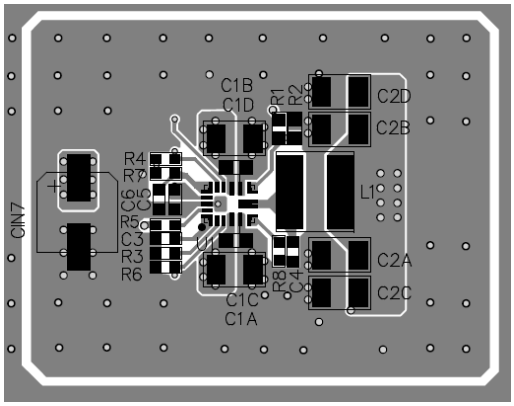
PCB Layout Guidelines (12)

Efficient PCB layout is critical for stable operation. A 4-layer layout is strongly recommended to achieve better thermal performance. For best results, refer to Figure 11 and follow the guidelines below:

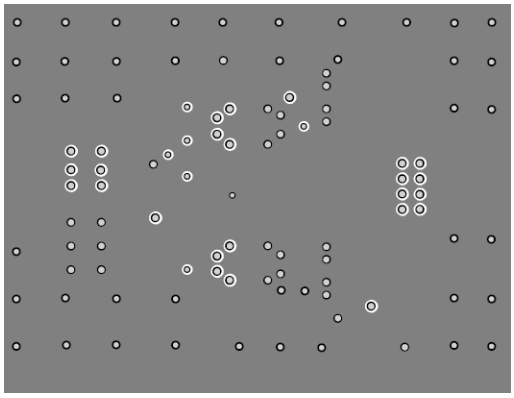
1. Place symmetric input capacitors as close to VIN and PGND as possible.
2. Connect a large ground plane directly to PGND.
3. If the bottom layer is a ground plane, add vias near PGND.
4. Ensure that the high-current paths at PGND and VIN have short, direct, and wide traces.
5. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high-frequency noise.
6. Keep the connection between the input capacitor and VIN as short and wide as possible.
7. Place the VCC capacitor as close to VCC and AGND as possible.
8. Route SW and BST away from sensitive analog areas, such as FB.
9. Use multiple vias to connect the power planes to the internal layers.

Note:

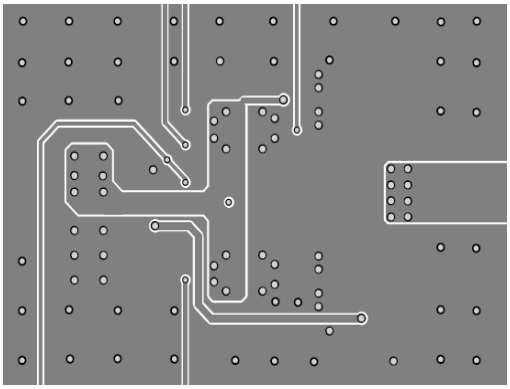
12) The recommended PCB layout is based on Figure 12 on page 50.



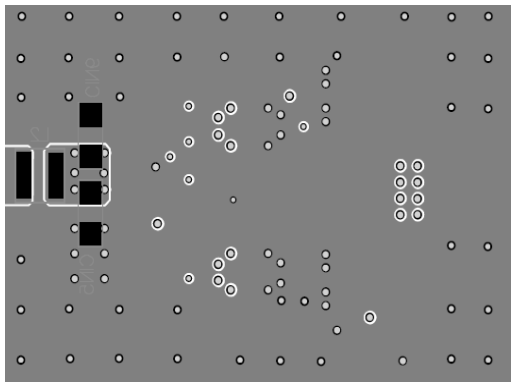
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 10: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

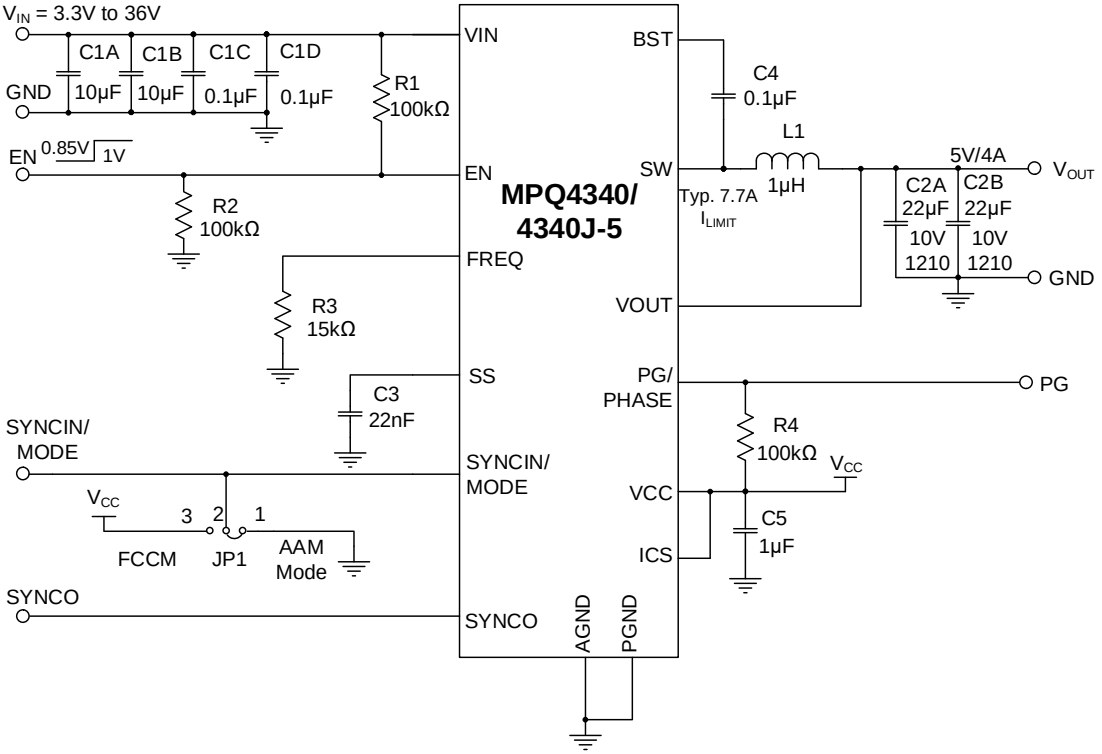


Figure 11: Typical Application Circuit (1-Phase, V_{OUT} = 5V, f_{SW} = 2.2MHz)

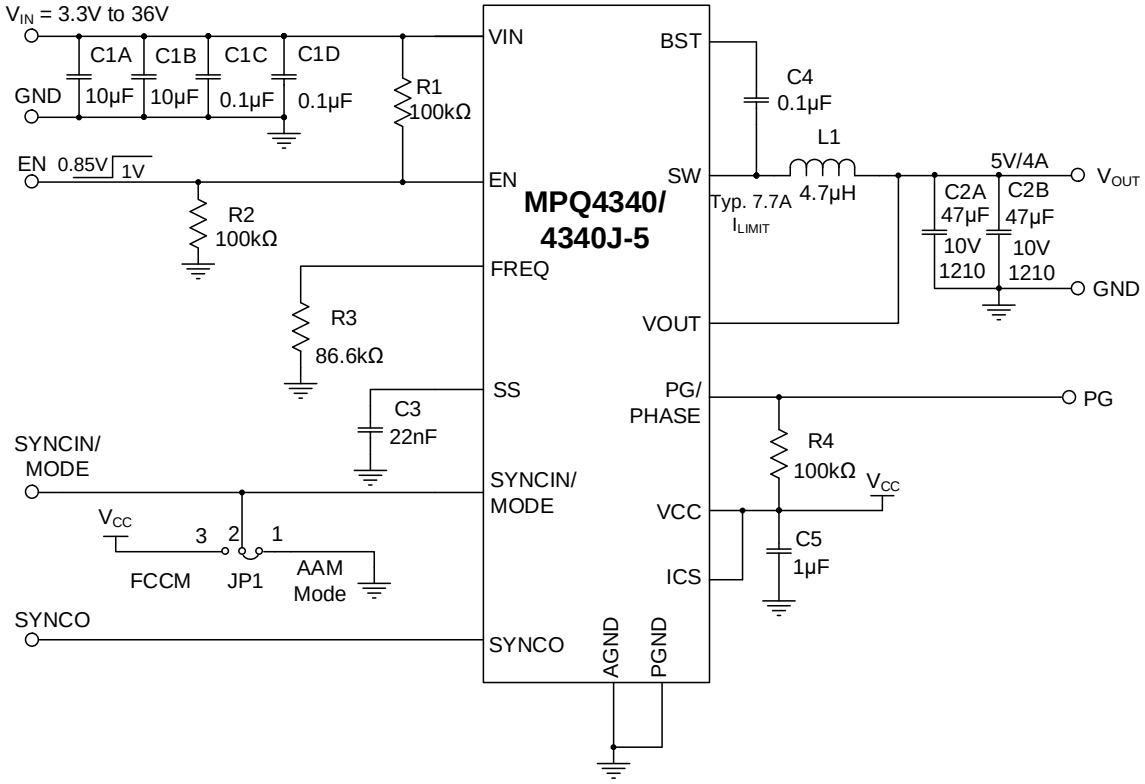


Figure 12: Typical Application Circuit (1-Phase, V_{OUT} = 5V, f_{SW} = 410kHz)

TYPICAL APPLICATION CIRCUITS *(continued)*

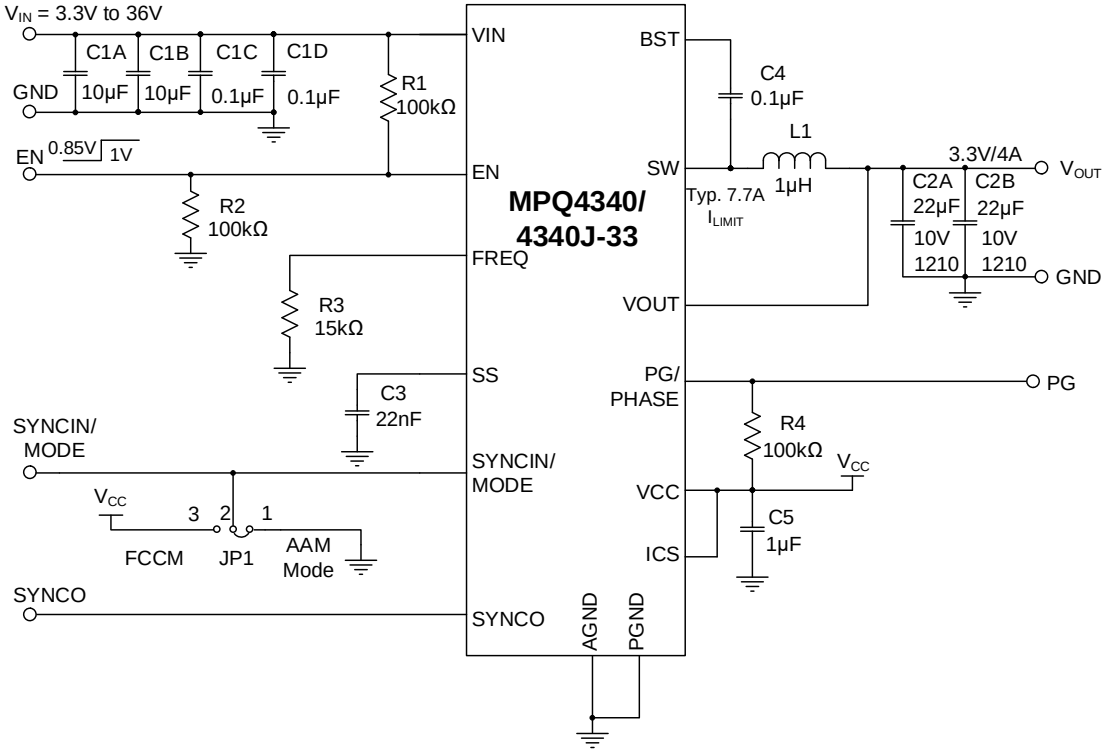


Figure 13: Typical Application Circuit (1-Phase, V_{OUT} = 3.3V, f_{SW} = 2.2MHz)

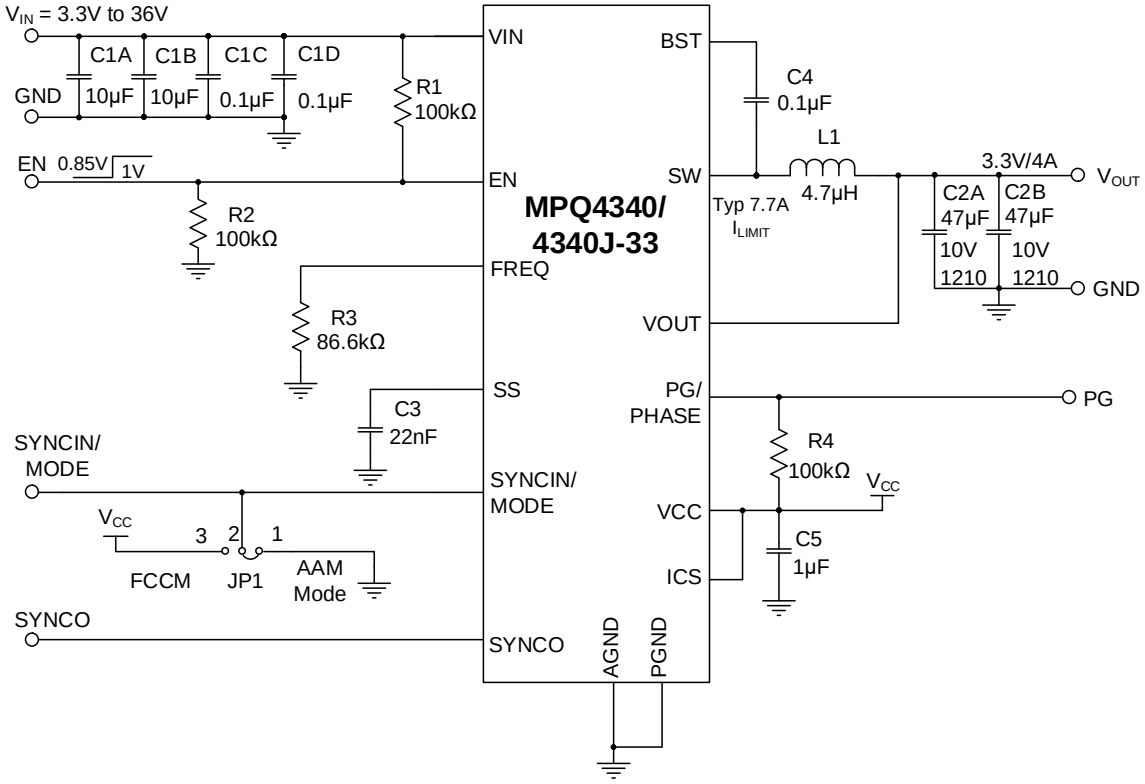


Figure 14: Typical Application Circuit (1-Phase, V_{OUT} = 3.3V, f_{SW} = 410kHz)

TYPICAL APPLICATION CIRCUITS *(continued)*

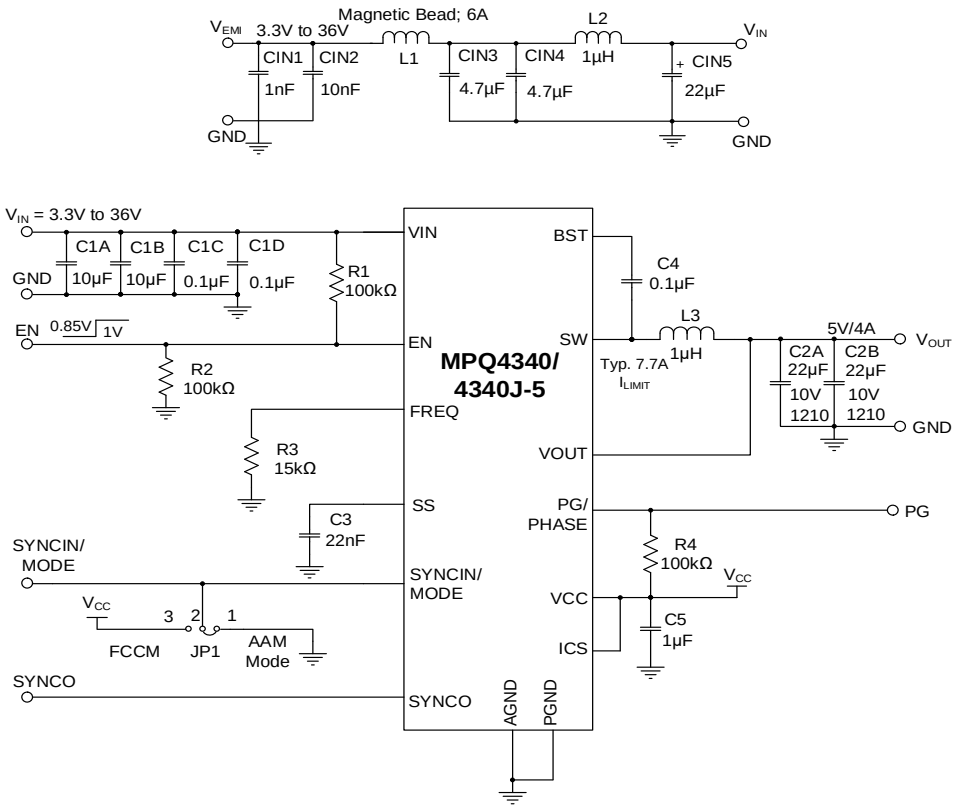


Figure 15: Typical Application Circuit (1-Phase, V_{OUT} = 5V, f_{SW} = 2.2MHz with EMI Filter)

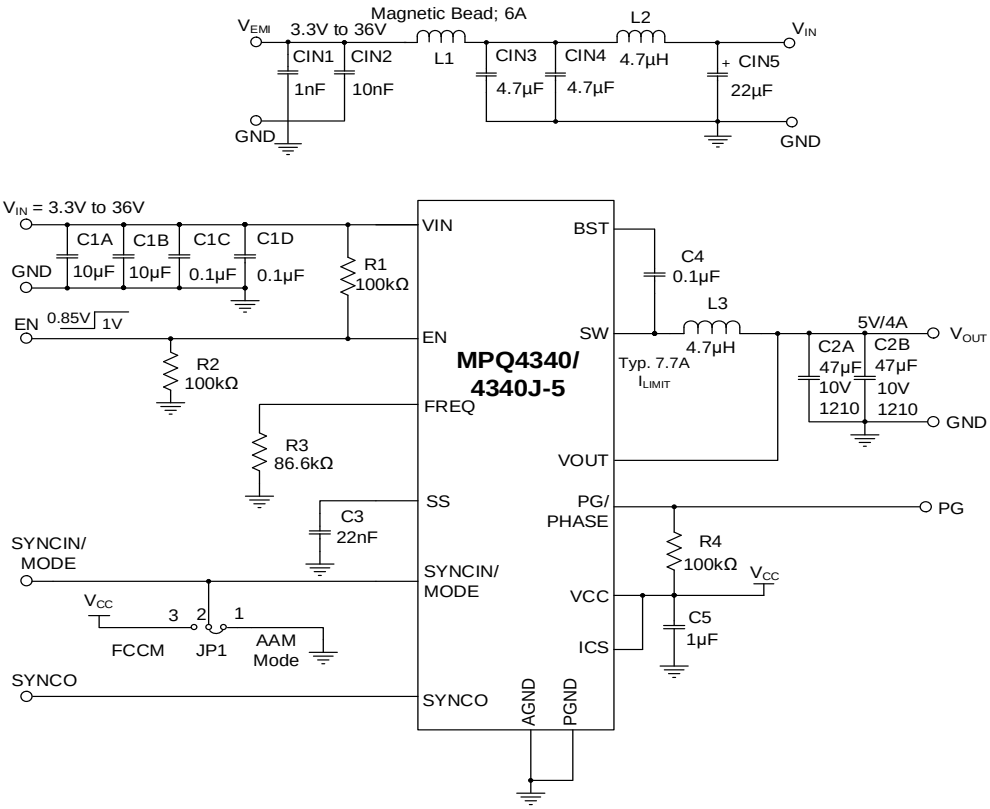


Figure 16: Typical Application Circuit (1-Phase, V_{OUT} = 5V, f_{SW} = 410kHz with EMI Filter)

TYPICAL APPLICATION CIRCUITS *(continued)*

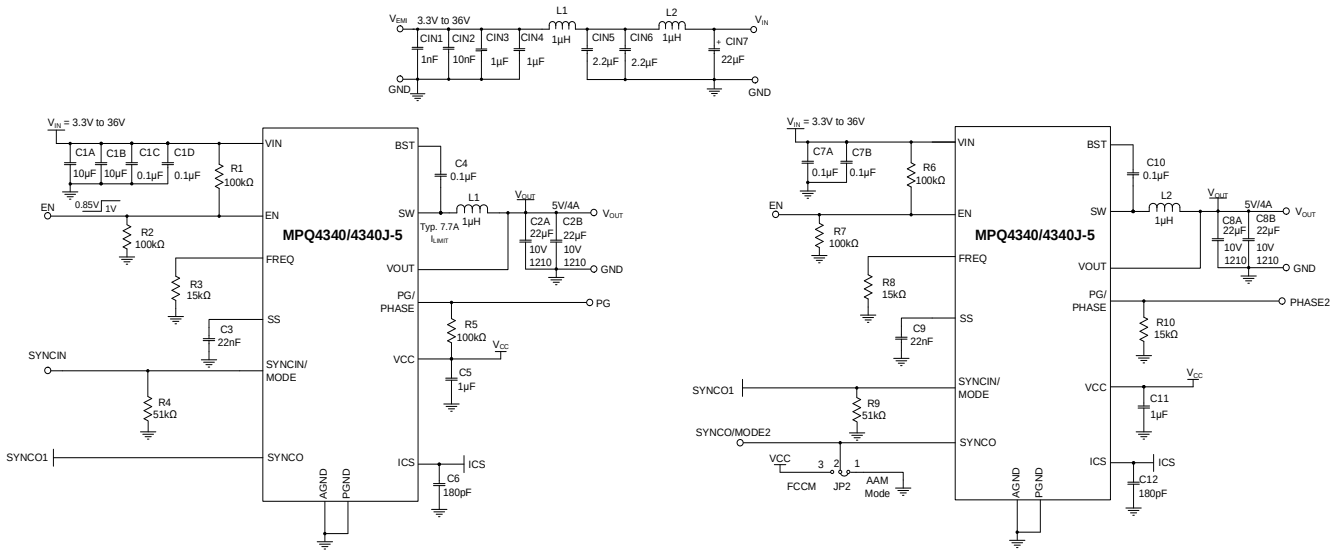


Figure 17: Typical Application Circuit (2-Phase, V_{OUT} = 5V, f_{SW} = 2.2MHz with EMI filter)

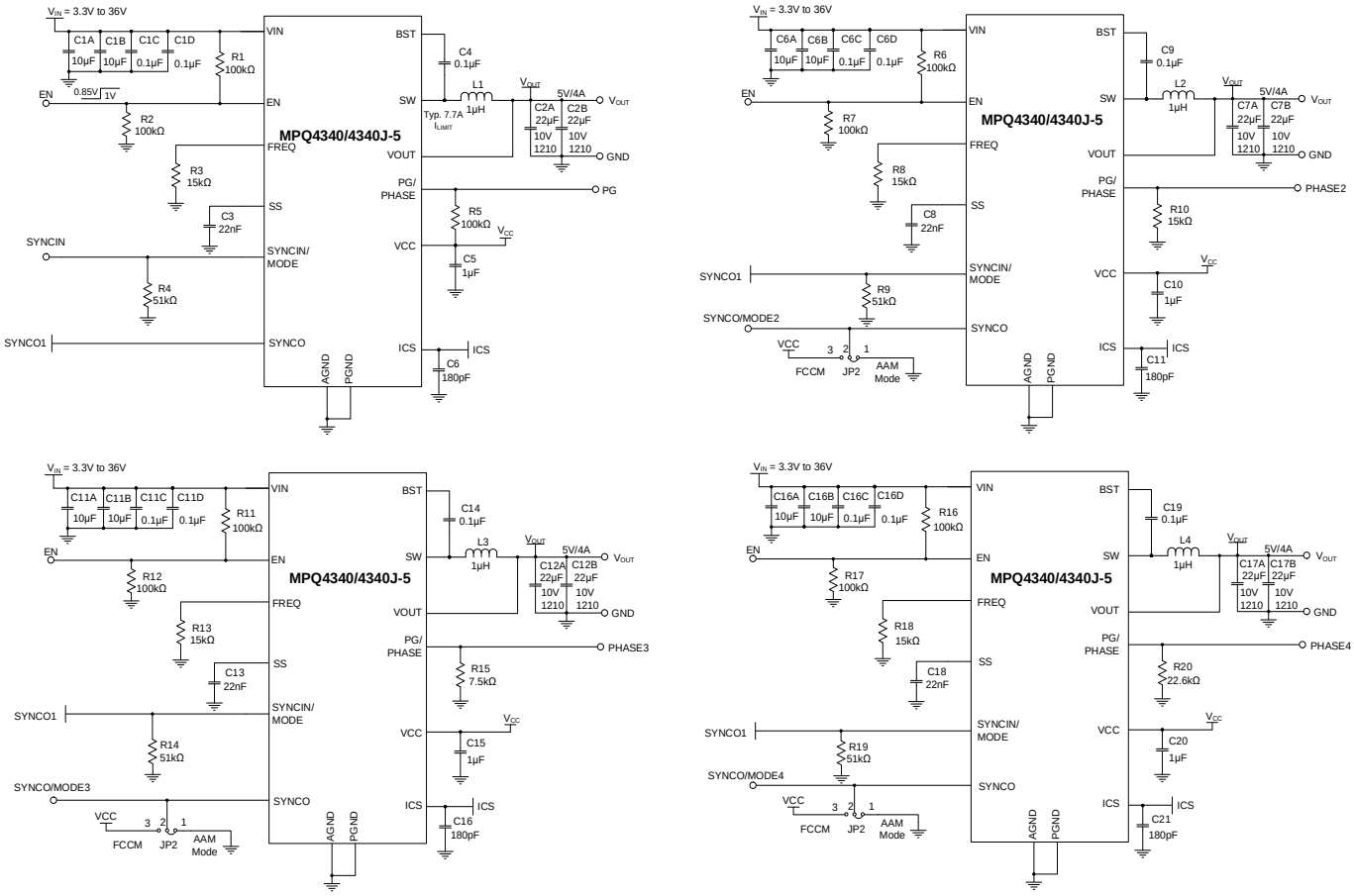
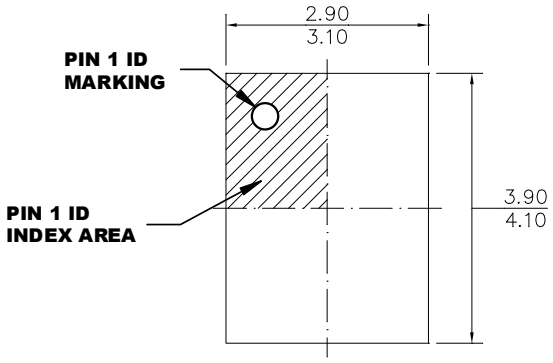


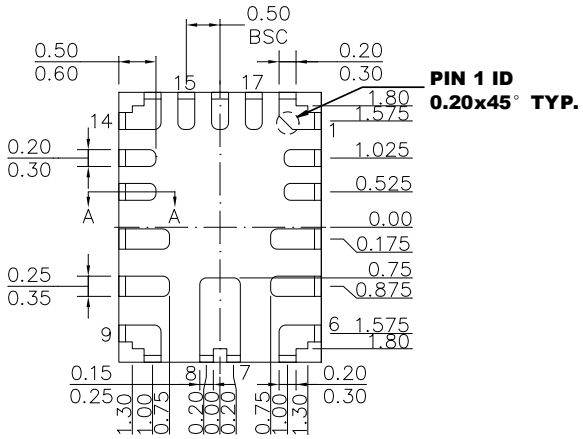
Figure 18: Typical Application Circuit (4-Phase, V_{OUT} = 5V, f_{SW} = 2.2MHz)

PACKAGE INFORMATION

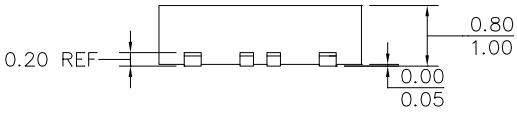
QFN-17 (3mmx4mm)



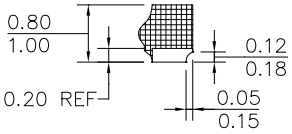
TOP VIEW



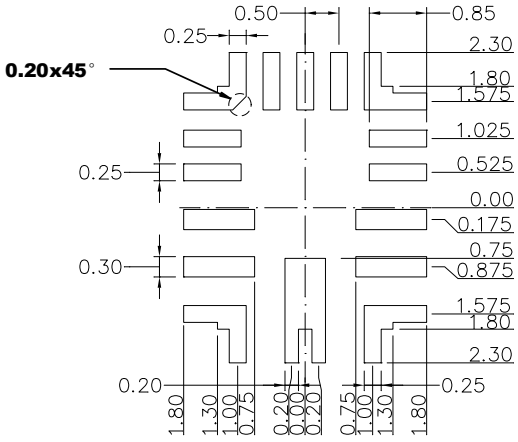
BOTTOM VIEW



SIDE VIEW



SECTION A-A



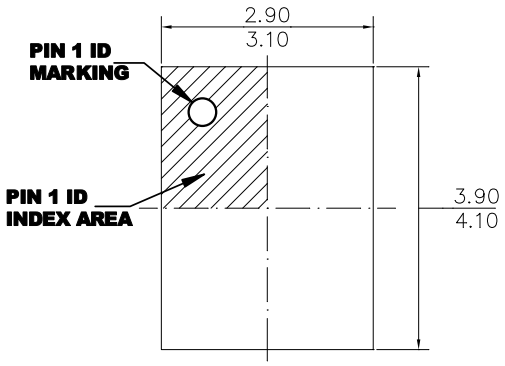
RECOMMENDED LAND PATTERN

NOTE:

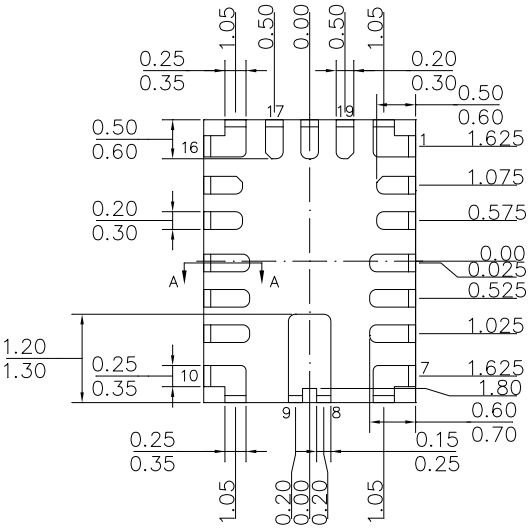
1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

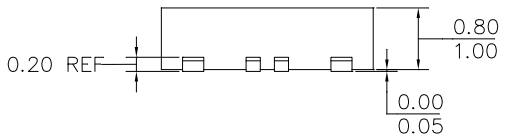
QFN-19 (3mmx4mm)



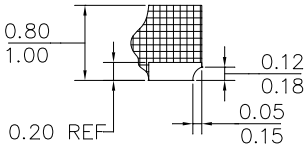
TOP VIEW



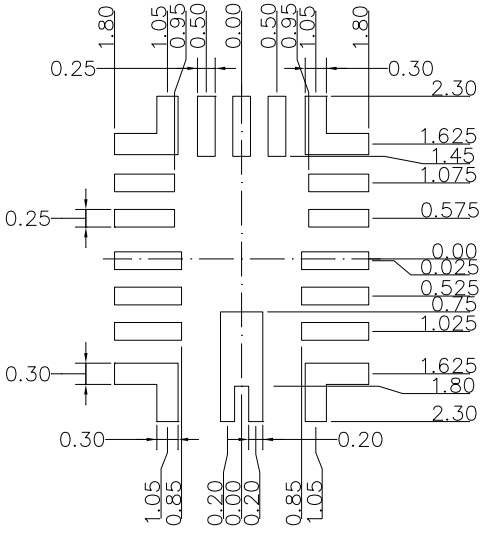
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

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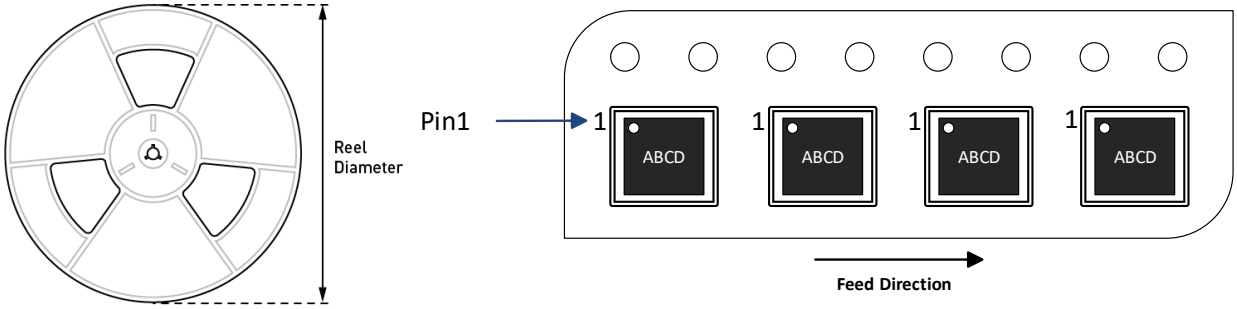
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube (13)	Quantity/ Tray (13)	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4340GLE-33-AEC1-Z	QFN-17 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ4340GLE-5-AEC1-Z	QFN-17 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ4340JGLE-33-AEC1-Z	QFN-19 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ4340JGLE-5-AEC1-Z	QFN-19 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

Note:

13) N/A indicates “not available” in tubes or trays. For 500-piece tape & reel prototype quantities, contact the factory. (The order code for the 500-piece partial reel is “-P”; the tape & reel dimensions remain the same as the full reel.)

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/16/2023	Initial Release	-