MPQ5031

Single Port USB PD Controller for Source Only, AEC-Q100 Qualified

DESCRIPTION

The MPQ5031 is a USB power delivery controller compatible with Type-C 2.0 and USB PD3.0 specifications. It targets DFP (provider) applications, such as charging-only USB PD ports and USB hubs.

The device is backward compatible, supporting DCP schemes for Quick Charge 3.0, battery charging specifications (BC1.2), Apple divider mode, Huawei FCP, and 1.2V/1.2V mode without outside user interaction. It also supports BC1.2 CDP handshaking. The I^2C interface and GPIO pins provide good communication with an external power converter.

The MPQ5031 supports up to 100W PD power and PPS as well. It can flexibly configure the PDO list, select slave devices, configure charging protocols, and set the protection mode.

Two NTC pins can be used to monitor for abnormal temperature rise, such as on the Type-C receptacle and PCB board. Power sharing functionality supports smart power budget management between two USB PD ports. PDO capability is reduced when the car battery voltage is low. High-voltage I/O pins support short to battery and short to VBUS protection for the DC/DC converter.

The MPQ5031 is available in a QFN-20 (4mmx4mm) package with wettable flanks.

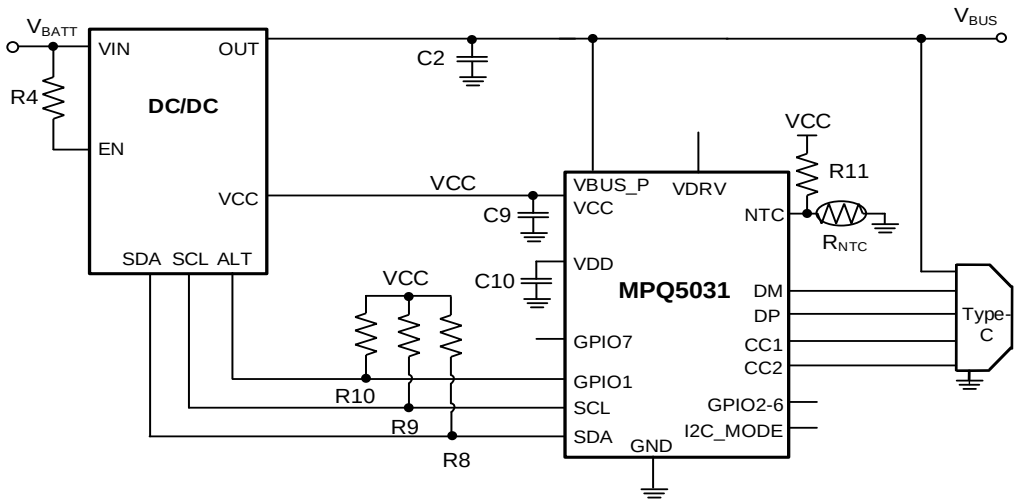
FEATURES

- Supports a 3.3V to 21V Bus Voltage Range
- 4.6V to 5.5V VCC Supply Voltage Range
- Integrated Physical Layer for BMC
- Integrated Protocol Layer
- Integrated Policy Engine
- Low Standby I_Q: 100µA
- Supports One Type-C DFP Port with USB PD3.0 and PPS
- Supports DCP Schemes for BC1.2, 3A Divider, and 1.2V/1.2V Mode
- Supports QC3.0, Huawei FCP
- VBUS Isolation N-Channel MOSFET Driver
- EN Off Timer Up to 120 Minutes
- I^2C Master/Slave Interface and Interrupt
- Load-Shedding with NTC or Battery Low Detection Function
- High-Voltage Pins for CC1, CC2, DP, and DM
- Integrated High-Voltage V_{CONN} Supply Power Switch
- Passed 60W USB-IF PPS Certification with the MPQ4230 (TID: 2313)
- Passed 100W USB-IF PPS Certification with the MPQ4214 (TID: 2316)
- Available in a QFN-20 (4mmx4mm) Package with Wettable Flanks
- Available in Automotive AEC-Q100 Grade 1

APPLICATIONS

- USB Power Delivery (Provider) Charging Ports
- USB PD Hubs

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL
MPQ5031GRE-0001-AEC1	QFN-20 (4mmx4mm)	*See Below*	1
MPQ5031GRE-0002-AEC1			
MPQ5031GRE-0003-AEC1			
MPQ5031GRE-0004-AEC1			
MPQ5031GRE-0013-AEC1			
MPQ5031GRE-0015-AEC1			
MPQ5031GRE-xxxx-AEC1**			
EVKT-MPQ5031	-	-	-

* For Tape & Reel, add suffix –Z (e.g. MPQ5031GRE-xxxx-AEC1–Z).

** “xxxx” is the configuration code identifier for the register setting stored in the OTP. Each “x” can be a hexadecimal value between 0 and F.

TOP MARKING

MPSYWW
MP5031
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
MP5031: Part number
LLLLLL: Lot number
E: Wettable lead flank

EVALUATION KIT EVKT-MPQ5031

EVKT-MPQ5031 kit contents (items listed below can be ordered separately):

#	Part Number	Item	Quantity
1	EVQ5031-4230-RE-00A	MPQ5031 + MPQ4230 evaluation board.	1
2	EVKT-USBI2C-02 bag	Includes USB to I^2C communication interface, one USB cable, and one ribbon cable.	1
3	MPQ5031GRE-0000-AEC1	IC with default configuration. Can be used for OTP configurations.	2

Order directly from MonolithicPower.com or our distributors.

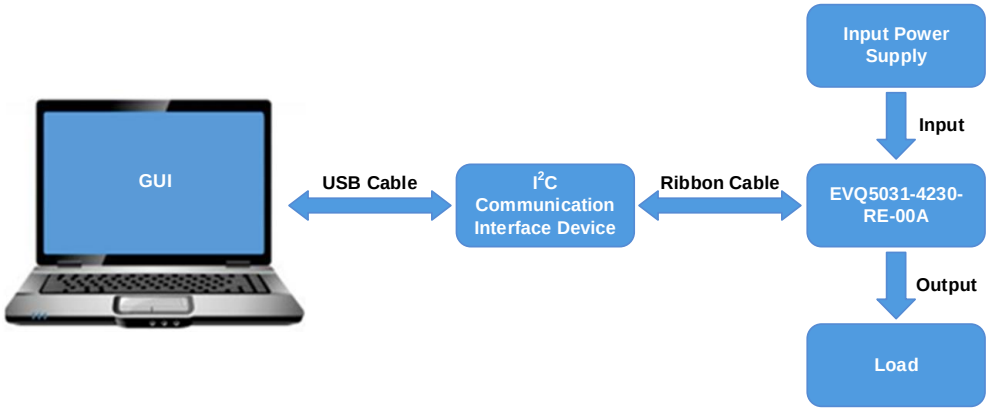
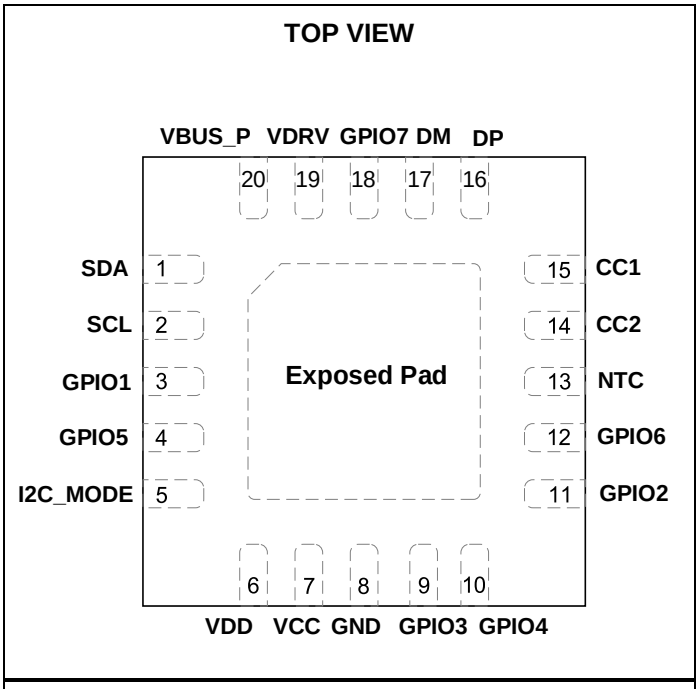


Figure 1: EVKT-MPQ5031 Evaluation Kit Set-Up

PACKAGE REFERENCE



QFN-20 (4mmx4mm) with Exposed Pad and Wettable Flank

PIN FUNCTIONS

Pin #	Name	I/O	Description
1	SDA	Bidirectional	**I²C data line.**
2	SCL	Bidirectional	**I²C clock signal input.** When the MPQ5031 is selected as the master, SCL is an output pin.
3	GPIO1	Bidirectional	**General purpose I/O 1.** See the GPIO register section on page 34 for more details.
4	GPIO5	Bidirectional	**General purpose I/O 5.** See the GPIO register section on page 35 for more details.
5	I2C_MODE	Input	**I²C operation mode setting.** Float or pull the I2C_MODE pin low to set the MPQ5031 as the I²C master. Pull this pin high to set the MPQ5031 as an I²C slave. When the MPQ5031 is set to I²C slave mode, the slave functions on GPIO5 and GPIO6 are disabled. Only pin 1 and pin 2 (SDA and SCL) are the I²C slave entrance. This pin has an internal 1MΩ pull-down resistor.
6	VDD	Output	**Internal 1.8V LDO regulator output.** Decouple with 0.47µF capacitor.
7	VCC	Input	**5V power supply for all internal circuitry.** The MPQ5031 operates from a 4.5V to 5.5V input voltage. A 4.7µF ceramic capacitor (C_{IN}) must be used to supply power to the internal circuitry, including VCONN.
8	GND	N/A	**Ground.**
9	GPIO3	Bidirectional	**General purpose I/O 3.** See the GPIO register section on page 34 for more details.
10	GPIO4	Bidirectional	**General purpose I/O 4.** See the GPIO register section on page 33 for more details.
11	GPIO2	Bidirectional	**General purpose I/O 2.** See the GPIO register section on page 34 for more details.
12	GPIO6	Bidirectional	**General purpose I/O 6.** See the GPIO register section on page 35 for more details.
13	NTC	Input	**External temperature-sense pin.** See the I²C register description on page 34 for the NTC trigger response.
14	CC2	Bidirectional	**Configuration channel (CC).** CC2 is used for the discovery, configuration, and management of connections across a USB Type-C cable.
15	CC1	Bidirectional	**Configuration channel (CC).** CC1 is used for the discovery, configuration, and management of connections across a USB Type-C cable.
16	DP	Bidirectional	**D+ data line to USB connector.** The DP and DM pins are the input/output used for handshaking with portable devices.
17	DM	Bidirectional	**D- data line to USB connector.** The DP and DM pins are the input/output used for handshaking with portable devices.
18	GPIO7	Bidirectional	**General purpose I/O 7.** See the GPIO register section on page 35 for more details.
19	VDRV	Output	**External N-Channel MOSFET gate driver signal.** When the sink is attached, VDRV drives the external N-channel MOSFET to turn on. Then power flows from the DC/DC output to the sink. When the sink is detached, VDRV drives the external N-channel MOSFET to turn off to isolate the power path.
20	VBUS_P	Input	**Bus voltage sensing and discharge pin.**
Exposed pad	N/A	N/A	**Exposed pad.** Connect to ground when designing the PCB layout.

ABSOLUTE MAXIMUM RATINGS (1)

VBUS_P .....-0.3V (-5V for <10ns) to +24V
VDRV .....VBUS_P + 5V
VDD..... -0.3V to +3V
DM, DP, CC1, CC2.....
……-0.3V (-5V for <10ns) to +24V
GPIO4, GPIO6, NTC ..... -0.3V to +5.5V
All other pins..... -0.3V to +6V
Continuous power dissipation (T_A = 25°C) (2)
QFN-20 (4mmx4mm).....2.1W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) .....±2kV
Charged device model (CDM).....±750V

Recommended Operating Conditions (3)

Power supply to VCC..... 5V/25mA
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-20 (4mmx4mm) ..... 60 ..... 12 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Standby supply current	I_{STB}	VCC current, unattached		100		µA
Supply current (on)	I_{ON}	CC1 to GND with 5.1kΩ Rd (as defined by USB Type-C Cable and Connector Specification Revision 2.0, which can be downloaded from the official USB website at https://usb.org/).		3.5	4.5	mA
Thermal shutdown (5)	T_{OTP_R}			150		°C
Thermal hysteresis (5)	T_{OTP_HYS}			20		°C
VDD regulator	V_{DD}		1.7	1.8	1.9	V
VDD load regulation	V_{DD_REG}	I_{DD} = 5mA		3		%
VCC UVLO rising threshold	V_{CC_RS}		4	4.3	4.6	V
VCC UVLO threshold hysteresis	V_{CC_HYS}			350		mV
VBUS_P_UV falling threshold	$V_{BUS\_P\_UV}$	I²C set VBUS_UV_THD = 0b	2.79	2.97	3.15	V
GPIO7						
DISCHG output high	V_{DIS_HIGH}	Discharge turn-on, 50kΩ load		4.4		V
DISCHG output low	R_{DIS_LOW}			3.3		kΩ
ADJ sink current	I_{ADJ}	GPIO3_ISENS+ = 1.5V	1	2	3	µA
EN_OUT_MID	$V_{EN\_OUT\_MID}$	100kΩ, pull-up resistor to 12V	0.8	1	1.2	V
EN_OUT high	$V_{EN\_OUT\_H}$	Open drain, 100kΩ, pull-up resistor to VCC	4.5			V
EN_OUT low	$V_{EN\_OUT\_L}$				0.4	V
GPIO5, GPIO6						
VBUS_UV_FIXPDO falling threshold	$V_{BUS\_UVFIX\_FALL}$	VBUS = 5V	0.91	0.96	1.01	V
IPWM duty cycle	$IPWM_{DUTY}$	4.7kΩ, pull-up resistor to VCC, 3A PDO		50		%
SYNC_OUT1 frequency	f_{SYNC1}	4.7kΩ, pull-up resistor to VCC		450		kHz
SYNC_OUT2 frequency	f_{SYNC2}	4.7kΩ, pull-up resistor to VCC		450		kHz
I²C_SLV_SDA/SCL frequency	$f_{I2C\_SLV\_SDA\_SCL}$	4.7kΩ, pull-up resistor to VCC		400		kHz
VSEL2 output low	V_{SEL_LOW}	100kΩ to VCC			0.4	V
GPIO4, GPIO3						
EN UVLO rising threshold	V_{EN_H}		1.33	1.43	1.53	V
EN UVLO falling hysteresis voltage	V_{EN_L}			220		mV
EN_OFF_DELAY	$t_{EN\_OFF\_DELAY}$	EN_OFF_TIMER = 010b		22		min
VBATT low falling threshold	$V_{BATT\_LOW\_F}$	Set GPIO4 = 11b	1.07	1.12	1.17	V
VBATT low rising threshold	$V_{BATT\_LOW\_R}$	Set GPIO4 = 11b	1.12	1.18	1.24	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 5V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
ATTACH output high	V_{ATTACH_HIGH}		4.5			V
ATTACH output low	V_{ATTACH_LOW}	Sink is attached			0.4	V
IPWM duty cycle	$IPWM_{DUTY}$	4.7kΩ, pull-up resistor to VCC, 3A PDO		50		%
Plug orientation (POL) output low	V_{POL_L}	CC1 = 5.1kΩ			0.4	V
POL output high	V_{POL_H}	CC2 = 5.1kΩ, 10kΩ, pull-up resistor to VCC	4.5			V
GPIO2						
Power share input low	V_{PS_LOW}	10kΩ pull-up resistor to VCC			0.4	V
Power share input high	V_{PS_H}	10kΩ pull-up resistor to VCC	3			V
POL output low	V_{POL_L}	CC1 = 5.1kΩ			0.4	V
POL output high	V_{POL_H}	CC2 = 5.1kΩ, 10kΩ, pull-up resistor to VCC	4.5			V
QC_12 pull low resistance	R_{QC_12}	DP/DM enter QC 12V		8		Ω
I2C_MODE						
Logic high threshold	V_{I2C_H}	Slave mode	1	1.2	1.4	V
Hysteresis	$V_{I2C\_H\_HYS}$			100		mV
Resistance	R_{I2C_MODE}			1		MΩ
GPIO1						
VSEL1 pull low resistance	R_{VSEL1}	12V PDO is selected		100		kΩ
VSEL1 output high	V_{SEL_HIGH}	100kΩ to VCC	4.5			V
INT logic high	V_{INT_HIGH}		4.5			V
INT logic low	V_{INT_LOW}				0.4	V
Leakage	I_{INT_LKG}				1	µA
PDO_SEL_OUTPUT (Configure SLAVE_DEVICE_SEL = 101b)						
PDO2 to PDO3 SEL_OUT pull low resistance	R_{PDO2_LOW}			7		Ω
PDO2-4 SEL OUT leakage	V_{PDO_HIGH}	5V PDO is selected			1	µA
NTC, NTC2						
External thermal-sense trip threshold	V_{NTC_R}	R_P = 47kΩ, R_{NTC} = 4.72kΩ (100°C)	7.5	9.1	10.5	%VCC
External thermal-sense recovery threshold	V_{NTC_F}	R_P = 47kΩ, R_{NTC} = 9.45kΩ (80°C)		16.7		%VCC
Gate Drive (VDRV)						
Gate drive voltage	V_{DRV}	V_{DRV} - V_{BUS_P}		4.85		V
Gate drive voltage at 15µA	V_{DRV_1}	I_{SOURCE} = 15µA		4.4		V
Pull-down resistor	R_{PULL_DOWN}			5		kΩ
BC1.2 DCP Mode						
DP and DM short resistance	$R_{DP\_DM\_SHORT}$	V_{DP} = 0.8V, I_{DM} = 1mA, T_J = 25°C		25	40	Ω

ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 5V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Divider Mode						
DP output voltage	$V_{DIVIDER\_DP}$	V_{OUT} = 5V	2.55	2.75	2.95	V
DM output voltage	$V_{DIVIDER\_DM}$	V_{OUT} = 5V	3.35	3.6	3.85	V
DP output impedance	$R_{DIVIDER\_DP}$			22		kΩ
DM output impedance	$R_{DIVIDER\_DM}$			22		kΩ
1.2V/1.2V Mode						
DP/DM output voltage	$V_{DP\_DM\_1.2V}$	V_{OUT} = 5V	1.05	1.20	1.35	V
DP/DM output impedance	$R_{DP\_DM\_1.2V}$			300		kΩ
Quick Charge 3.0 Mode						
DP/DM low voltage	V_{QC_LOW}		0.2	0.3	0.4	V
DP/DM high voltage	V_{QC_HIGH}		1.8	2	2.2	V
DP output impendence	R_{DP_QC}			350	1500	kΩ
DM output impendence	R_{DM_QC}			20		kΩ
DM low glitch time (5)	t_{GLITCH_DM}			10		ms
DP high glitch time	t_{GLITCH_DP}		1000		1500	ms
Output voltage change glitch time (5)	$t_{GLITCH\_V\_CHANGE}$		20	40	60	ms
Bus voltage step (5)	$V_{BUS\_CONT\_STEP}$		150	200	250	mV
Time for VBUS to discharge to 5V when DP < 0.6V (5)	t_{V_UNPLUG}				500	ms
FCP Mode						
DM Tx high voltage	V_{FCPT_H}	R_{LOAD} = 15kΩ	2.55		5	V
DM Tx low voltage	V_{FCPT_L}	R_{LOAD} = 15kΩ			0.4	V
DM Rx high voltage	V_{FCPR_H}		1.5		5	V
DM Rx low voltage	V_{FCPR_L}				1	V
DM pull-low resistance (5)	R_{LD_D-}			15		kΩ
Unit interval of PHY (5)	UI	f_{CLK} = 125kHz	144	160	176	µs
CDP Mode (I^2C set CDP_EN=1)						
DM CDP output voltage	V_{DM_SRC}	V_{DP} = 0.6V, DM_SINK = 250µA	0.5	0.6	0.7	V
DP rising lower window threshold for V_{DM_SRC}	V_{DAT_REF}		0.25	0.35	0.45	V
DP rising lower window threshold hysteresis	$V_{DAT\_REF\_HYS}$			50		mV
DP rising upper window threshold for V_{DM_SRC}	V_{LGC_SRC}		0.8	0.95	1.1	V
DP rising upper window threshold hysteresis	$V_{LGC\_SRC\_HYS}$			80		mV
USB Type-C – CC1 and CC2 pins						
CC pull-up current 1	I_{RP1}	VBUS = 5V/3A, T_J = 25°C	304	330	356	µA
CC pull-up current 2	I_{RP2}	VBUS = 5V/1.5A, T_J = 25°C	162	180	198	µA
CC voltage to enable V_{CONN} for 3A Type-C mode	V_{RA1}	T_J = 25°C			0.75	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 5V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
CC voltage to enable V_{BUS} for 3A Type-C mode	V_{RD1}	T_J = 25°C	0.85		2.45	V
CC detach threshold for 3A Type-C mode	V_{OPEN1}	T_J = 25°C	2.75			V
CC voltage falling debounce timer	$t_{CC\_DEBOUNCE}$	VBUS enable deglitch	100	150	200	ms
CC voltage rising debounce timer	$t_{PD\_DEBOUNCE}$	VBUS disable deglitch	5	10	15	ms
V_{CONN} output power	P_{V_CONN}	VCC supplies V_{CONN}	0.1			W
USB PD						
Unit interval	t_{UI}	T_J = 25°C	3.0	3.35	3.7	µs
Transmitter						
End drive BMC (5)	t_{EDBMC}				23	µs
Fall time (5)	t_{FALL}		300			ns
Rise time (5)	t_{RISE}		300			ns
Hold low BMC (5)	t_{HLBMC}		1			µs
Logic high voltage	V_{LH}		1	1.15	1.3	V
Logic low voltage	V_{LL}				100	mV
Output impedance	R_{TX}			50		Ω
Receiver (5)						
CC receiver capacitance	$C_{RECEIVER}$				600	pF
Transitions for signal detection	$N_{TRANSITION}$		3			edges
Rx bandwidth limiting filter	t_{RX_FILTER}		100			ns
Time Window for Detecting Non-idle	$t_{TRANSITION\_WINDOW}$		12		20	µs
Receiver input impedance	R_{BMC_RX}		1			MΩ
I²C Interface Specifications (5)						
Input logic high	V_{IL}		1.4			V
Input logic low	V_{IH}				0.6	V
Output voltage logic low	V_{OUT_L}				0.4	V
SCL clock frequency	f_{SCL}			400		kHz
SCL high time	t_{HIGH}		60			ns
SCL low time	t_{LOW}		160			ns
Data set-up time	t_{SU_DAT}		10			ns
Data hold time	t_{HD_DAT}			70		ns
Set-up time for repeated start	t_{SU_STA}		160			ns
Hold time for a repeated start condition	t_{HD_STA}		160			ns
Bus free time between a start and a stop condition	t_{BUF}		160			ns

ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 5V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Set-up time for a stop condition	$t_{SU.STO}$		160			ns
SCL and SDA rise time	t_R		10		300	ns
SCL and SDA fall time	t_F		10		300	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance bus for each bus line	C_B				400	pF

Note:

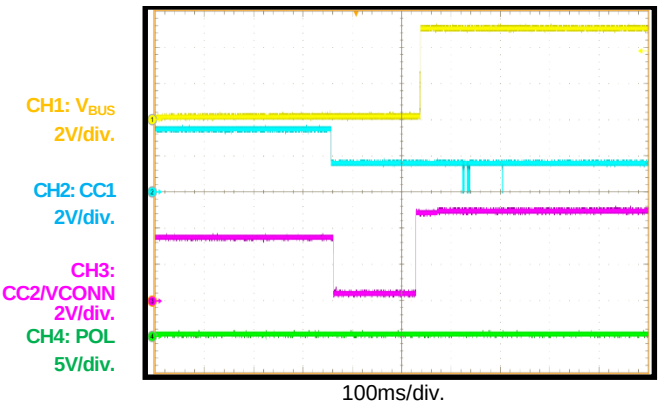
5) Guaranteed by characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 5V, V_{BUS} = 5V to 20V, T_A = 25°C, unless otherwise noted. Connect the MPQ5031's VBUS_P pin to the MPQ4230's output.

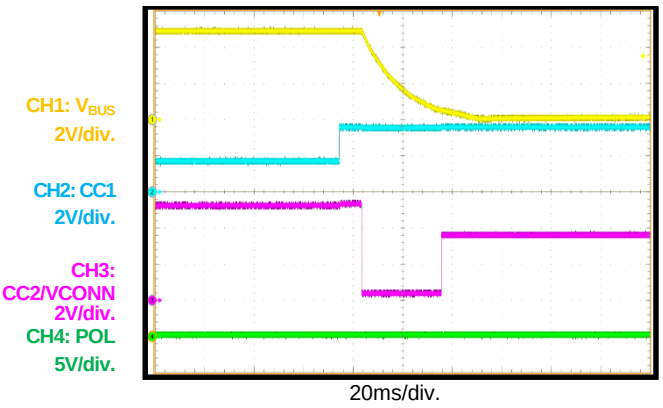
CC1 Attached Rd to Enable VBUS

I_{OUT} = 0A



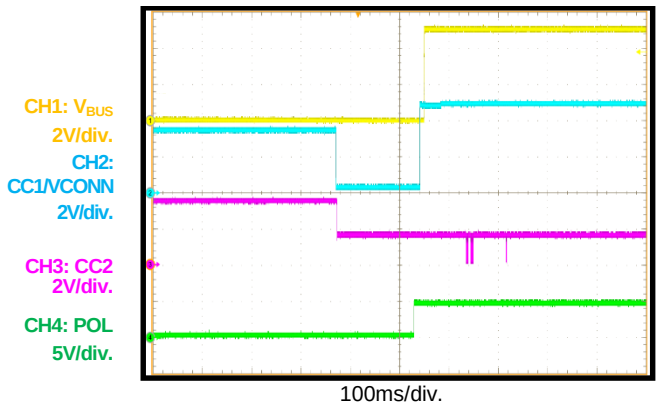
CC1 Detached Rd to Disable VBUS

I_{OUT} = 0A



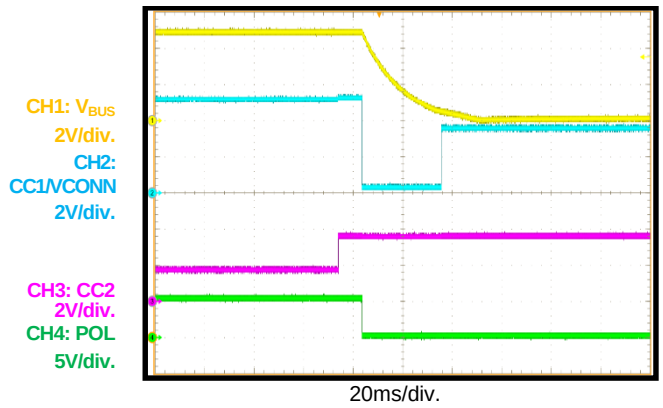
CC2 Attached Rd to Enable VBUS

I_{OUT} = 0A



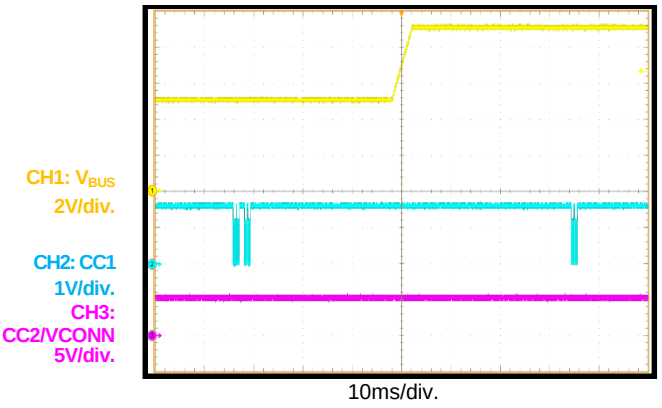
CC2 Detached Rd to Disable VBUS

I_{OUT} = 0A



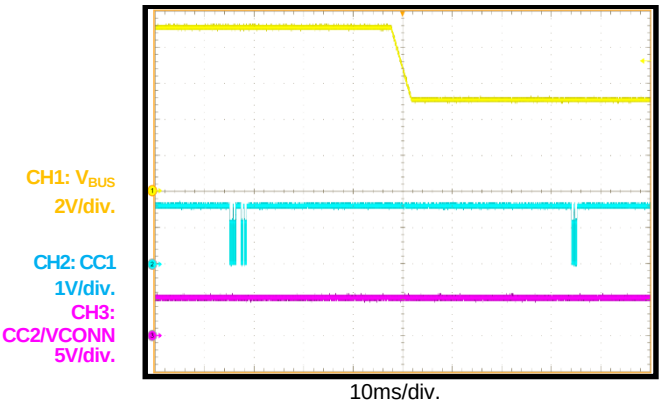
PDO Transition

5V PDO to 9V PDO



PDO Transition

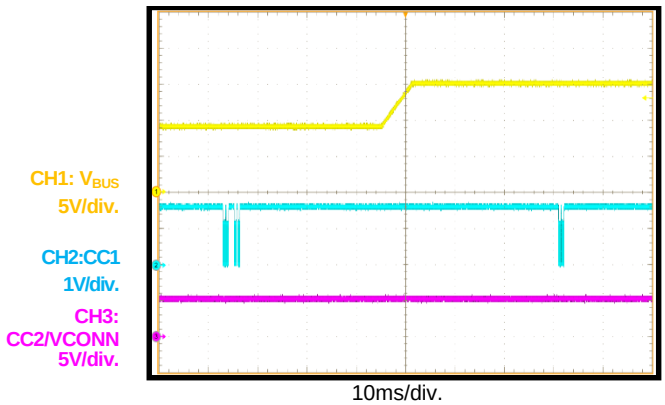
9V PDO to 5V PDO



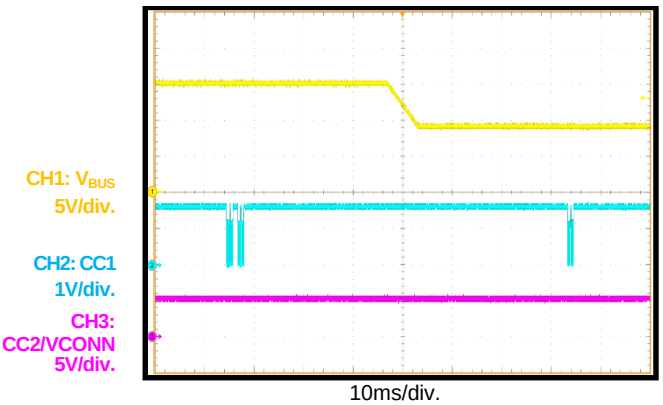
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{CC} = 5V, V_{BUS} = 5V to 20V, T_A = 25°C, unless otherwise noted. Connect the MPQ5031's VBUS_P pin to the MPQ4230's output.

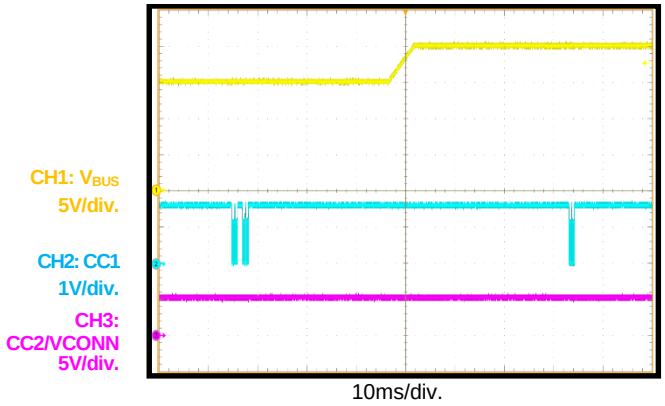
PDO Transition
9V PDO to 15V PDO



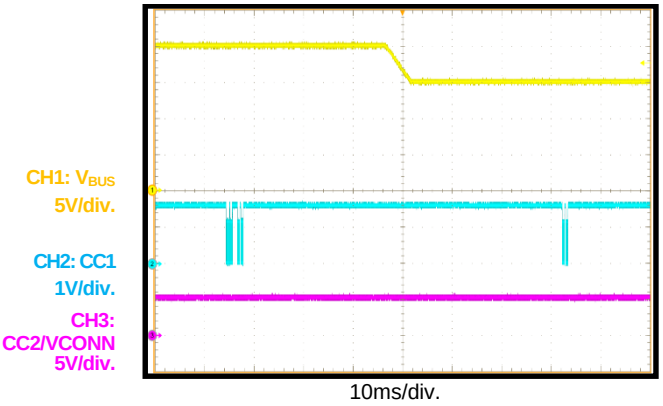
PDO Transition
15V PDO to 9V PDO



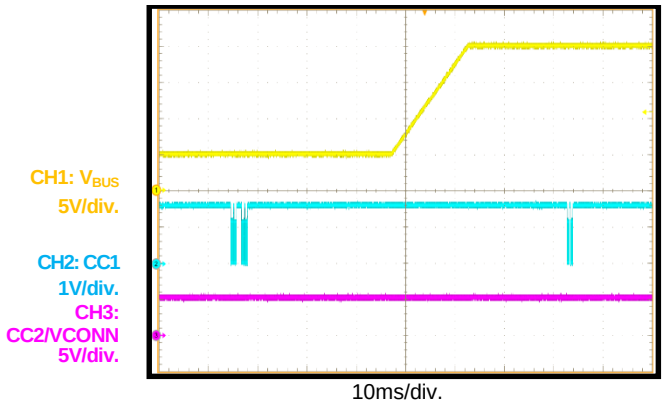
PDO Transition
15V PDO to 20V PDO



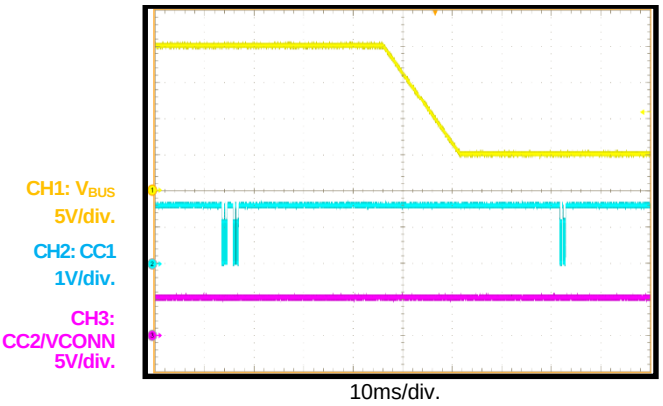
PDO Transition
20V PDO to 15V PDO



PDO Transition
5V PDO to 20V PDO



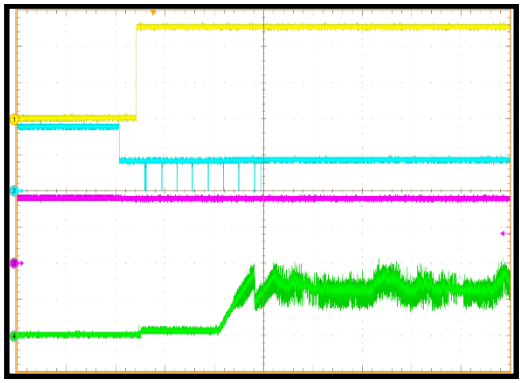
PDO Transition
20V PDO to 5V PDO



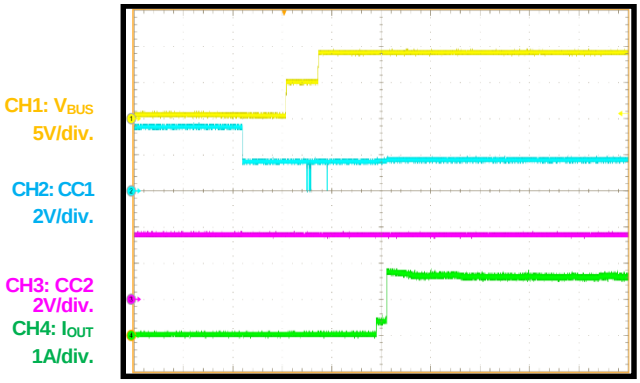
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{CC} = 5V, V_{BUS} = 5V to 20V, T_A = 25°C, unless otherwise noted. Connect the MPQ5031's VBUS_P pin to the MPQ4230's output.

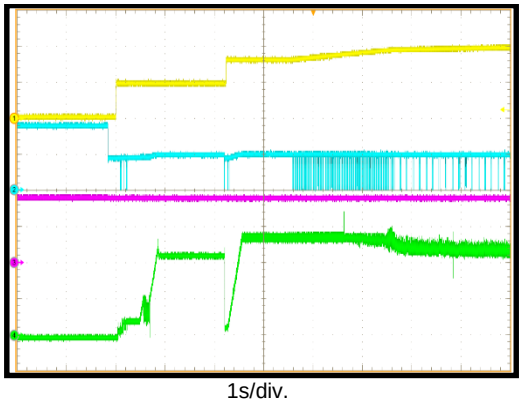
Mobile Phone Charging Test
Phone requests 5V PDO



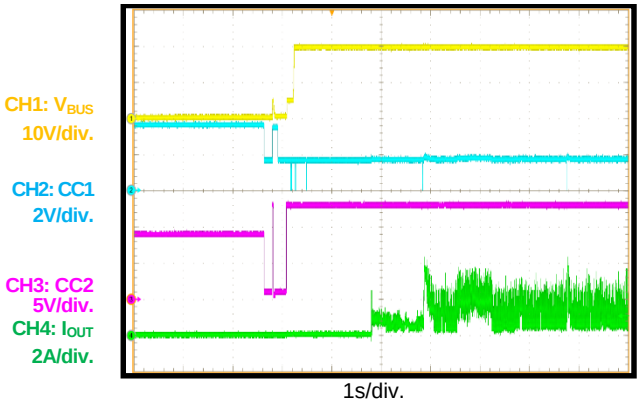
Mobile Phone Charging Test
Phone requests 9V PDO



Mobile Phone Charging Test
Phone requests 3.3V to 21V APDO



Laptop Charging Test
Laptop requests 20V PDO



FUNCTIONAL BLOCK DIAGRAM

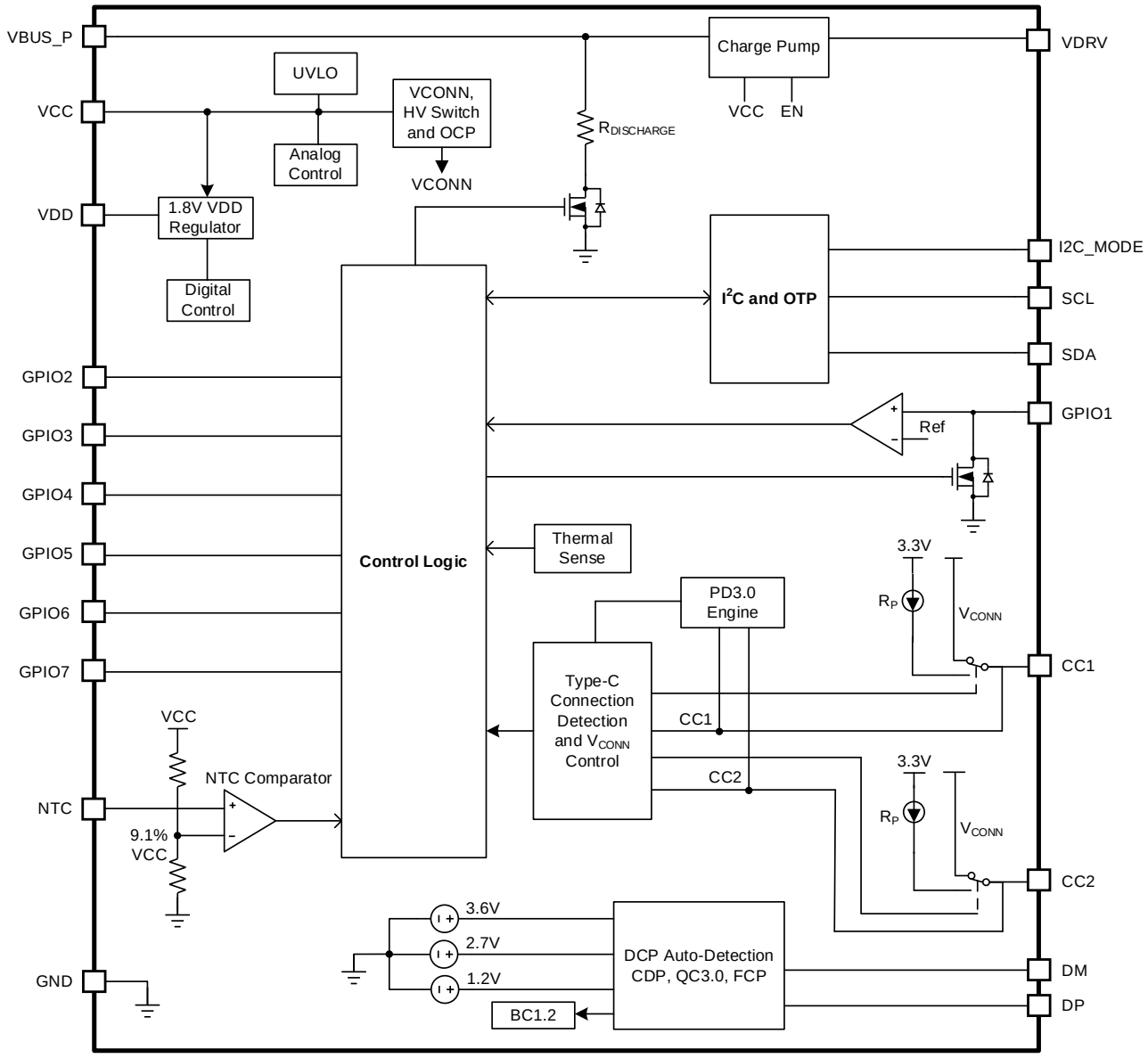


Figure 2: Functional Block Diagram

OPERATION

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MPQ5031's UVLO comparator monitors the VCC input voltage.

VCC and VDD Regulator

The VCC pin is biased by an external 5V supply (e.g. the DC/DC converter's VCC pin). The VCC pin must have a decoupling capacitor between 1µF and 10µF.

The 1.8V internal VDD regulator uses VCC as the input. The VDD pin powers most of the digital circuitries, and requires a 0.47µF decoupling capacitor.

Charging Mode Auto-Detection

Legacy USB 2.0 Mode

The MPQ5031 integrates a USB dedicated charging port auto-detection function that can recognize most mainstream portable devices. It supports the following charging schemes:

- USB Battery Charging Specification BC1.2/ Chinese Telecommunications Industry Standard YD/T 1591-2009
- Apple 3A divider mode
- 1.2V/1.2V mode
- QC3.0 Class A (3.3V to 12V)
- Huawei FCP Class A

The auto-detection function is a state machine that supports all of the above DCP charging schemes, starting in divider mode. If a device compliant with divider mode is attached, the MPQ5031 remains in divider mode. Then 3.6V is applied to the DM pin, and 2.7V is applied to the DP pin.

If a device compliant with BC1.2 or YD/T 1591-2009 is attached, the MPQ5031 operates in 1.2V/1.2V and BC1.2 DCP mode. DM and DP are shorted together with a resistance below 40Ω. The MPQ5031 remains in that mode until the device releases the data line. Then the device returns to divider mode.

When a QC3.0 or FCP device (without PD protocol) is attached, the MPQ5031 automatically enters high-voltage quick charge mode.

The MPQ5031 supports BC1.2 charging data port (CDP) handshaking as well, which can be enabled by the I^2C. DCP mode should be disabled (LEGACY_CHARGING_MODE_SEL = 11b) when the CDP function is selected.

If a USB PD contract is established once the sink is attached, QC3.0 functionality is disabled, but BC1.2 short mode is still enabled.

USB Type-C Port

The USB Type-C receptacle, plug, and cable solution incorporates a configuration process to detect a downstream-facing port (DFP) to upstream-facing port (UFP) connection for V_{BUS} management, and to determine the host-to-device relationship.

Initially, DFP-to-UFP attachment is detected by a host (DFP) when one of the CC pins at its USB Type-C receptacle senses a specified resistance to GND. Subsequently, UFP-to-DFP detachment is detected when the CC pin that was terminated at its USB Type-C receptacle is no longer connected to GND.

Power is not applied to the USB Type-C host or hub receptacle (V_{BUS} or V_{CONN}) until the DFP detects the presence of an attached device (UFP) port. When a DFP-to-UFP attachment is detected, the DFP enables power to the receptacle and begins normal USB operation with the attached device. When a DFP-to-UFP detachment is detected, the port sourcing V_{BUS} removes power.

The MPQ5031 is a DFP (provider only), and its power supply capability is rated at 5V/3.0A by default. V_{CONN} is provided by the DFP to power the cables and electronics in the plug. V_{CONN} is provided instead of the CC pin if the CC pin is not connected to the cable's configuration channel (CC) wire. V_{CONN} has a maximum power output of 100mW.

V_{CONN} is disabled until R_A is detected. R_A is a pull-down resistor connected from the CC pin to GND, and its resistance should be below 1.2kΩ.

USB Power Delivery

In USB power delivery (PD), pairs of directly attached ports negotiate voltage, current, and/or direction of power flow over the USB cable by

using the CC wire as the communication channel. The mechanisms that are implemented operate independently of other USB methods that are used to negotiate power.

Type-C connectors can support the CC wire as the communication channel. The USB PD engine is disabled until a valid Type-C connection is established. Figure 3 shows a USB PD communication stack.

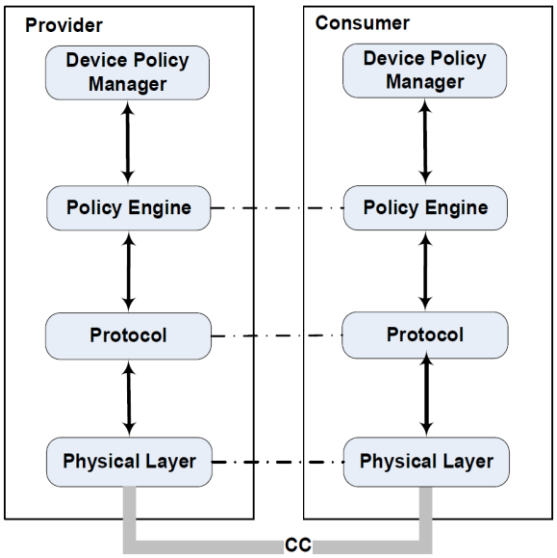


Figure 3: USB PD Communication Stack

DFP Commands

Table 1, Table 2, and Table 3 list the MPQ5031's supported commands. Table 1 lists the control messages.

Table 1: Control Message

Transmitted Message	Received Message
Accept	Get_PPS_Status
Get_Sink_Cap	Get_Source_Cap
Get_Sink_Cap_ Extended	Get_Source_Cap_ Extended
Get_Status	Get_Status
GoodCRC	GoodCRC
GotoMin	Not_Supported
Not_Supported	Reject
PS_RDY	Soft_Reset
Reject	VCONN_Swap
Soft_Reset	

Table 2 lists the different data messages.

Table 2: Data Messages

Transmitted Message	Received Message
Source_Capabilities	Sink_Capabilities
BIST	Request
Alert	BIST
	Alert

Table 3 lists the extended messages.

Table 3: Extended Messages

Transmitted Message	Received Message
Status	
PPS_Status	
Source_Capabilities_ Extended	

The MPQ5031 also supports soft reset, hard reset, and cable discovery for VDM signals. Figure 4 shows the device policy manager.

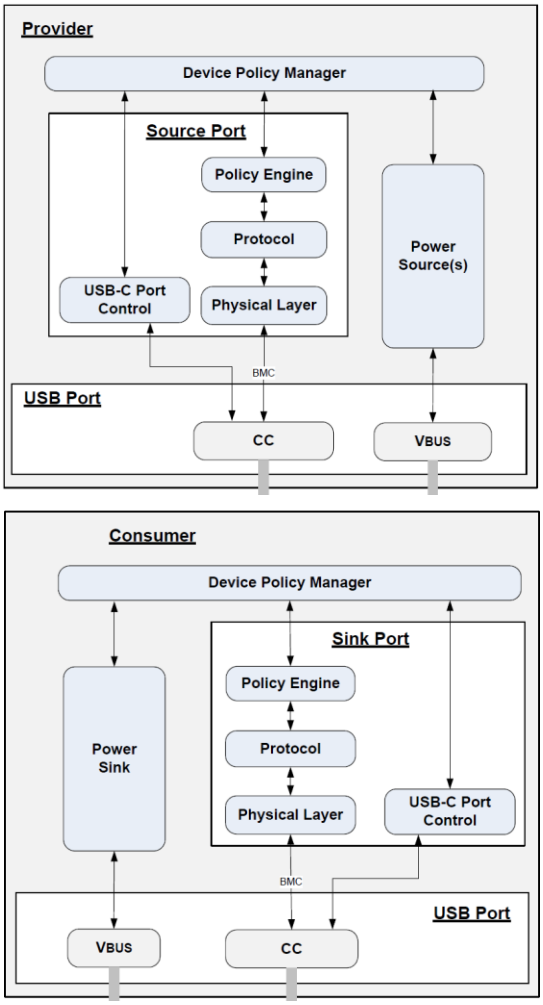


Figure 4: Device Policy Manager

PD Contract Handshake

Figure 5 shows the MPQ5031's PD contract handshake sequence.

#	CH	OS	Power	Data	Cable Plug	Type
0	CC2	SOP'			UFP or DFP	Vendor_Defined
1	CC2	SOP'			Cable Plug	GoodCRC
2	CC2	SOP'			Cable Plug	Vendor_Defined
3	CC2	SOP'			UFP or DFP	GoodCRC
4	CC2	SOP	Source	DFP		Source_Capabilities
5	CC2	SOP	Sink	UFP		GoodCRC
6	CC2	SOP	Sink	UFP		Request
7	CC2	SOP	Source	DFP		GoodCRC
8	CC2	SOP	Source	DFP		Accept
9	CC2	SOP	Sink	UFP		GoodCRC
10	CC2	SOP	Source	DFP		PS_RDY
11	CC2	SOP	Sink	UFP		GoodCRC

Figure 5: PD Contract Handshake

VBUS and VCONN Discharge

When the sink is detached or a hard reset occurs, the MPQ5031 sends a command to turn off the DC/DC regulator's output voltage, and VBUS_P's 200Ω discharge resistor turns on for 200ms. The GPIO7 pin can also be used to control an external MOSFET to discharge the output voltage for 200ms. Meanwhile, the VCONN voltage is discharged with a 1kΩ resistor for 30ms.

VBUS Under-Voltage (UV) Detection

When a DC/DC converter with an I²C interface is selected, the VBUS under-voltage (UV) detection function is enabled by monitoring PG_STATUS. If the VBUS_P voltage is <2.97V (or <4.5V) during PPS operation, the VBUS_UV bit is set to 1 internally, and a hard reset is triggered.

When a DC/DC converter without an I²C interface is selected, PPS functionality is disabled. In fixed PDO operation, GPIO5 can be configured to VBUS_UV_FIXPDO. For this function, connect GPIO5 to VBUS with a 1/5 resistor divider to detect the VBUS voltage. Table 4 lists how to set the VBUS UV threshold in a fixed PDO state. When the VBUS voltage is below the threshold, VBUS_UV_FIXPDO is set to 1 internally, and a hard reset is triggered.

Table 4: VBUS UV Threshold (Only Valid for DC/DC Converters without I²C)

Sink Requested	VBUS_UV_ FIXPDO Threshold (V)	VBUS UV threshold (V)
Default, V_{OUT} = 5V	0.96	4.8
V_{OUT} = 9V	1.743	8.715
V_{OUT} = 15V	2.938	14.69
V_{OUT} = 20V	3.88	19.4

Figure 6 shows a VBUS UV example.

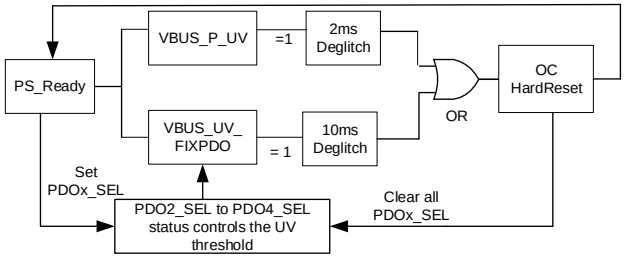


Figure 6: VBUS UV Detection for Non-I²C DC/DC ApplicationsStart-Up and Shutdown Timing

The GPIO3, GPIO4, and GPIO6 pins can be configured to be the EN input function that controls when the MPQ5031 is on or off.

If the MPQ5031's VCC exceeds 4.3V and the GPIOx_EN pin is pulled high, the PD engine can be enabled. The MPQ5031's start-up time should begin after the DC/DC converter start-up time, and its shutdown time should be before the converter's shutdown time (see Figure 7).

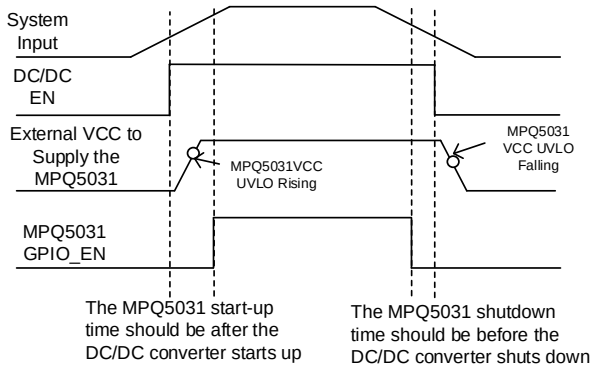


Figure 7: MPQ5031 Start-Up and Shutdown Timing

When the MPQ421x, MPQ423x, MPQ426x or MPQ4272 is used as the DC/DC converter, the converter's 5V LDO output can power the MPQ5031's VCC. If the MP28167-A is selected as the DC/DC converter, an external 5V LDO should be added to power the MPQ5031. The

external 5V LDO's start-up timing should be later than the MP281671-A's timing.

In the MPQ421x, MPQ4272, or MP28167-A PD solution, the MPQ5031's GPIOx_EN pin should be added to control the PD engine's start-up/shutdown time.

If connecting the MPQ5031 GPIOx_EN pin to VIN, the input voltage (V_{IN}) of the PD's start-up and shutdown sequence can be calculated with Equation (1) and Equation (2), respectively:

$$V_{IN\_ON}\ (V) = 1.43V \times (R_{DN2} + R_{UP2}) / R_{DN2} \quad (1)$$

$$V_{IN\_OFF}\ (V) = 1.21V \times (R_{DN2} + R_{UP2}) / R_{DN2} \quad (2)$$

Figure 8 shows the MPQ5031's start-up time schematic.

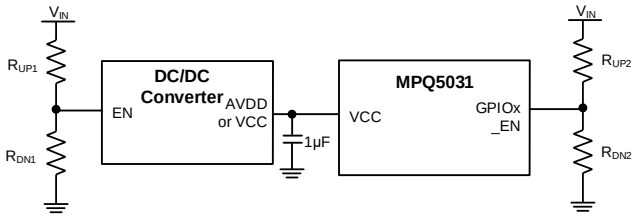


Figure 8: MPQ5031 Start-Up Time Schematic

Table 5 lists the V_{IN} start-up and shutdown thresholds.

Table 5: V_{IN} Start-Up/Shutdown Threshold

	DC/DC EN Divider (kΩ)	MPQ5031 EN Divider (kΩ)	DC/DC Start-Up/ Shutdown (V)	MPQ5031 Start-Up/ Shutdown (V)
MPQ5031 + MPQ4214	100/30	100/28.4	5.85/5.07	6.47/5.47
MPQ5031 + MPQ4272	100/39	100/28.4	5.7/4.9	6.47/5.47

EN Off Delay Timer

The GPIO3 pin can be configured for EN_OFF_DELAY_OUT functionality. When EN is high, the IC is enabled immediately. When the external EN off signal is received, EN_OFF_DELAY_OUT (GPIO3) remains high for 22min (EN_OFF_TIMER = 010b) to enable the upstream DC/DC converter. Once the 22min delay time completes, the USB PD engine is disabled immediately and CLK is disabled after a 200ms delay (see Figure 9). Figure 10 on page 20 shows the timing sequence.

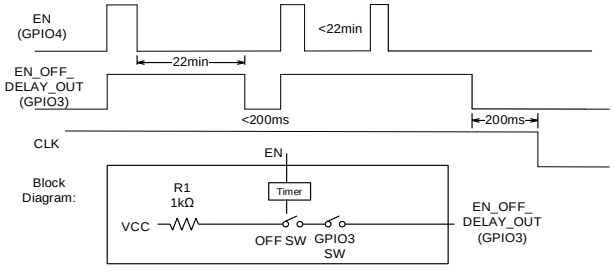


Figure 9: EN Off Timer

If EN_OFF_DELAY functionality is not required, configure the GPIO3 for a function that is not EN_OFF_DELAY_OUT.

State Machine and Timing Sequence

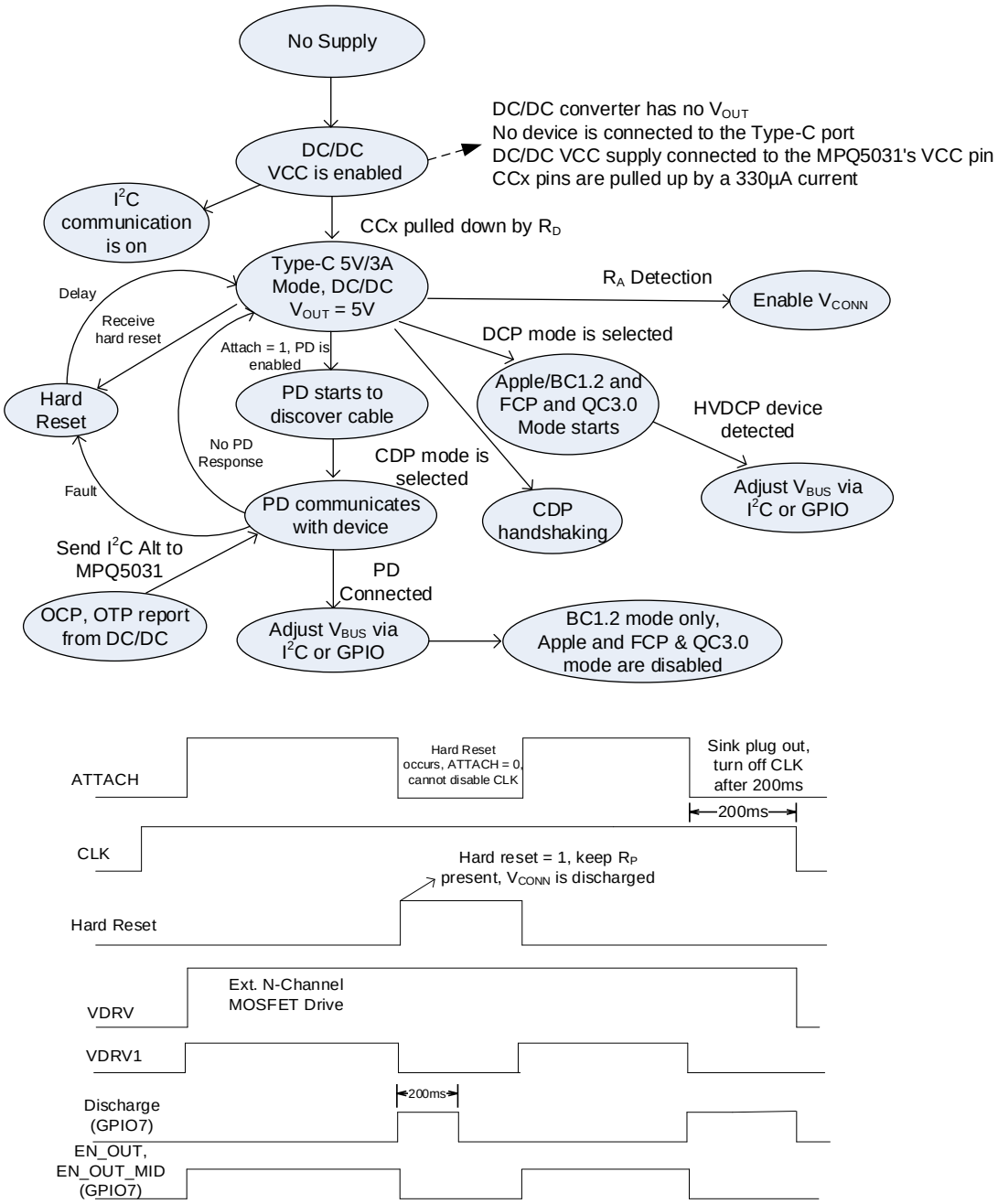


Figure 10: State Machine and Attached Timing Sequence

V_{CONN} Over-Current Protection (OCP)

The VCC to V_{CONN} switch has a 20Ω resistance and a 50mA over-current protection (OCP) threshold. When V_{CONN} OCP is triggered, the V_{CONN} output latches off. The following actions can re-enable V_{CONN} :

- Cycling power on VIN and EN
- A hard reset
- Detaching and reattaching the USB Type-C device

Bidirectional I²C Interface

The MPQ5031's SDA and SCL pins support both I²C master and I²C slave functions. When cooperating with an external buck-boost converter (e.g. the MPQ4230), the MPQ5031 should operate in I²C master mode. When a user wants to configure the MPQ5031's I²C register, I²C slave mode should be selected.

Float I2C_MODE or pull it to GND to set the MPQ5031 to I²C master mode. Pull I2C_MODE to VCC to set the MPQ5031 to I²C slave mode. In I²C slave mode (I2C_MODE = VCC), the digital CLK is always on. The I²C register and I²C functionality are active once VCC is ready. The user does not need to wait for a Type-C sink to be attached.

The GPIO5 and GPIO6 pins can be configured as a second I²C slave entrance, but an internal clock must be turned on to access full I²C functionality. SDA, SCL, GPIO5, and GPIO6 cannot simultaneously work in I²C slave mode (see Table 6).

Table 6: I²C Function on Pin 1, Pin 2 and GPIO5, GPIO6

I2C_MODE Input	Pin 1, Pin 2 (SDA, SCL) Function	GPIO5, GPIO6 I²C Function	Internal Clock
VCC	In I²C slave mode	I²C functionality is disabled	Always on
GND	In I²C master mode	In I²C slave mode. Must turn on internal clock to access full I²C function	Either USB Type-C attachment or writing 0x55AA to register 0x14 can enable the internal clock

Battery Low Detection

The GPIO4 and GPIO2 pins can be configured as an input battery voltage sense pin. If the battery voltage drops below a certain level (this level is configurable), then the USB PD engine updates the source capability based on the I²C control bits VBATT_LOW_PULL_PS_EN and VBATT_LOW_PULL_NTC_EN (see Table 7). When the battery voltage recovers, the USB PD engine changes the source capabilities to normal. If VBATT_LOW_PULL_NTC_EN = 1, the source capability returns to normal after a 16-second delay.

This function can also be disabled via I²C control bits VBATT_LOW_PULL_PS_EN and VBATT_LOW_PULL_NTC_EN.

The recommended resistor divider ratio on VBATT_SENSE pin is 1/10. The internal comparator falling threshold is 1.12V, and the rising threshold is 1.18V with a 20μs deglitch time.

Table 7: Battery Low Update Source Capability

VBATT_LOW_PULL_PS_EN	0	0	1
VBATT_LOW_PULL_NTC_EN	0	1	0
Battery Voltage Low	PDO list is based on the PDO_TYPE register setting	Update PDO1 to 5V/2A, other PDOs are disabled	Disable the PDO with a power rating ≥ PWR_SHARE_TO_PDP

The battery voltage can be calculated with Equation (3):

$$V_{BATT\_LOW}\ (V) = 1.12V \times (R_{DN} + R_{UP}) / R_{DN} \quad (3)$$

Figure 11 shows the resistor divider.

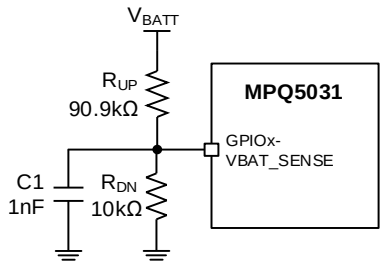


Figure 11: VBATT_SENSE Divider Resistor

Load-Shedding Entry and Recovery

When the NTC or NTC2 (NTC2_PS_EN = 0) falling threshold is triggered (NTC_MODE = 0), the Type-C resistor (R_P) pull-up current changes from 330µA to 180µA, regardless of whether there is a PD contract.

When MPQ423x or MPQ426x device is selected (SLAVE_DEVICE_SEL = 001b), and it sends an OT_WARNING signal and a PD contract exists, the Type-C pull-up current (R_P) changes from 330µA to 180µA. The Type-C detection threshold then changes accordingly. If a PD contract exists, the USB PD PDO is updated to 5V/2A, and all other PDOs are disabled.

If the NTC or NTC2 voltage recovers to a normal value, and the external DC/DC converter OT_WARNING = 0 (after a 16-second delay), R_P changes back to 330µA. If there was originally a PD contract, the MPQ5031 USB PD engine sends the default PDOs again. When NTC2_PS_EN = 1 and the NTC2 falling threshold is triggered, the MPQ5031 updates the PDO list based on the PWR_SHARE_TO_PDP setting.

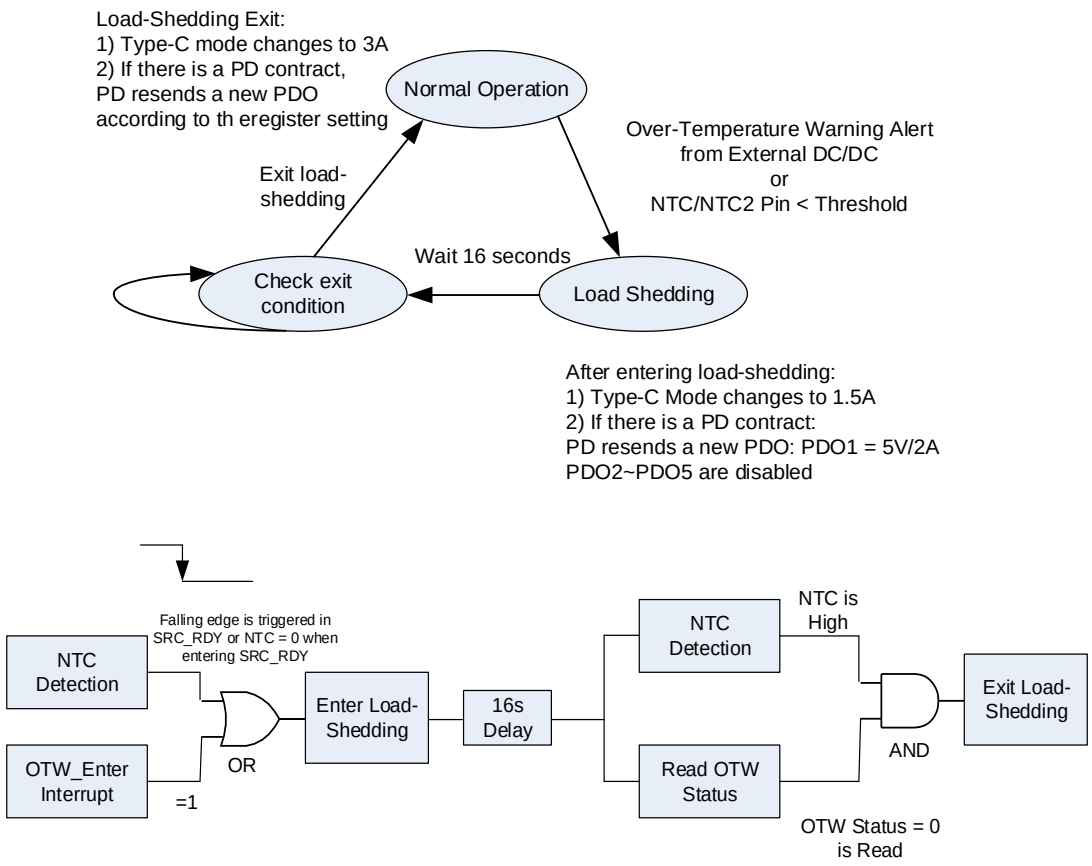


Figure 12: Load-Shedding Logic and State Machine (NTC2_PS_EN = 0)

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C or the NTC/NTC2 falling threshold is triggered (NTC_MODE = 1), the MPQ5031 resets the USB PD engine and stops the DC/DC converter from switching via I²C communication, or by pulling the converter's EN pin low. When the temperature falls below its lower threshold (about 130°C), the chip is enabled for CCx detection. If the sink is attached, the MPQ5031 starts to enable the USB PD engine again.

The I²C slave is still operational during thermal shutdown.

Power Sharing Function

The GPIO2 pin can be configured for power share input functions. When GPIO2 (POWER_SHARE) is pulled low, the USB PD engine disables the PDO if the power rating meets or exceeds PWR_SHARE_TO_PDP, and all PPS APDOs are disabled.

The GPIO3, GPIO5, or GPIO7 pins can be configured for ATTACH indication. If using multiple devices, and the first MPQ5031 (MPQ5031 #1) detects that a sink is attached, it pulls GPIO3 low. Then the second MPQ5031's (MPQ5031 #2) GPIO2 is pulled low at the same time. MPQ5031 #2 disables the PDO with a power rating that is ≥PWR_SHARE_TO_PDP, and all PPS APDOs are disabled.

The GPIO2 pin can also be used for power share output functions. When the MPQ5031's sink-requested PDO power rating is ≥PWR_SHARE_OUTPUT_THLD, GPIO2 is pulled low.

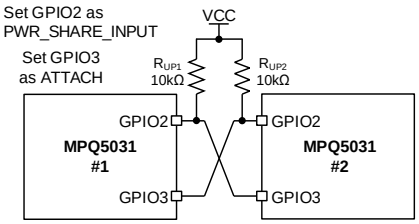


Figure 13: Power-Share Connection between Two MPQ5031s (Cut Total Power to 50%/50%)

I²C Arbitration

The GPIO3 pin can be configured for I²C arbitration (I2C_ARB) functions. When MPQ5031 #1 sends an I²C command, it pulls down GPIO3 first. GPIO3 is pulled high again after MPQ5031 #1's I²C command is finished. MPQ5031 #2 always checks the GPIO3 status, and starts to send an I²C command until GPIO3 is released to high (see Figure 14). It is can be used in MPQ4272 reference design.

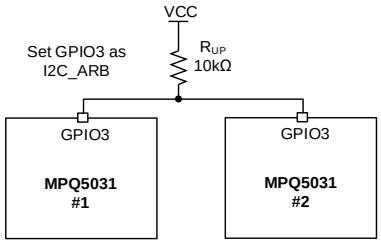


Figure 14: I²C Arbitration Connection

CDP Mode

The MPQ5031 integrates CDP mode handshaking. Set CDP_EN = 1 to enable CDP mode handshaking, and disable Apple divider mode, FCP, 1.2V/1.2V mode and other DCP schemes on DP and DM (LEGACY_CHARGING_MODE_SEL = 11b) (see Figure 15).

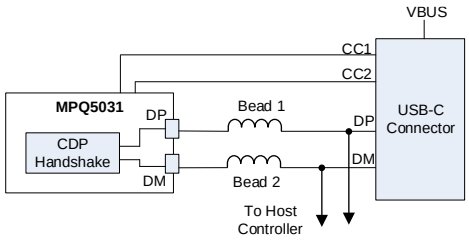


Figure 15: CDP Mode Set-Up

Smart Line Drop Compensation

The MPQ5031 has smart line drop compensation when the MPQ423x, MPQ426x or MPQ421x DC/DC converter is attached. Line drop compensation is active in fixed PDO or non-PD conditions. After entering a PPS condition, line drop compensation is disabled. If the other DC/DC converter is selected, the line drop compensation value is determined by the converter's set-up. The MPQ5031 does not disable line drop compensation in a PPS state.

When an MPQ423x or MPQ426x device is selected (SLAVE_DEVICE_SEL = 001b), the line drop compensation value is determined by the MPQ423x or MPQ426x's set-up. The MPQ5031 disables MPQ423x or MPQ426x line drop compensation after entering PPS.

When an MPQ421x device is selected (SLAVE_DEVICE_SEL = 000b), the MPQ5031 GPIO3 can be configured for ISENS+ functions to sense the MPQ421x's COMP pin voltage. GPIO7 can be configured for ADJ functions to sink the 2μA current on the MPQ421x's FB pin when the COMP voltage exceeds a certain voltage.

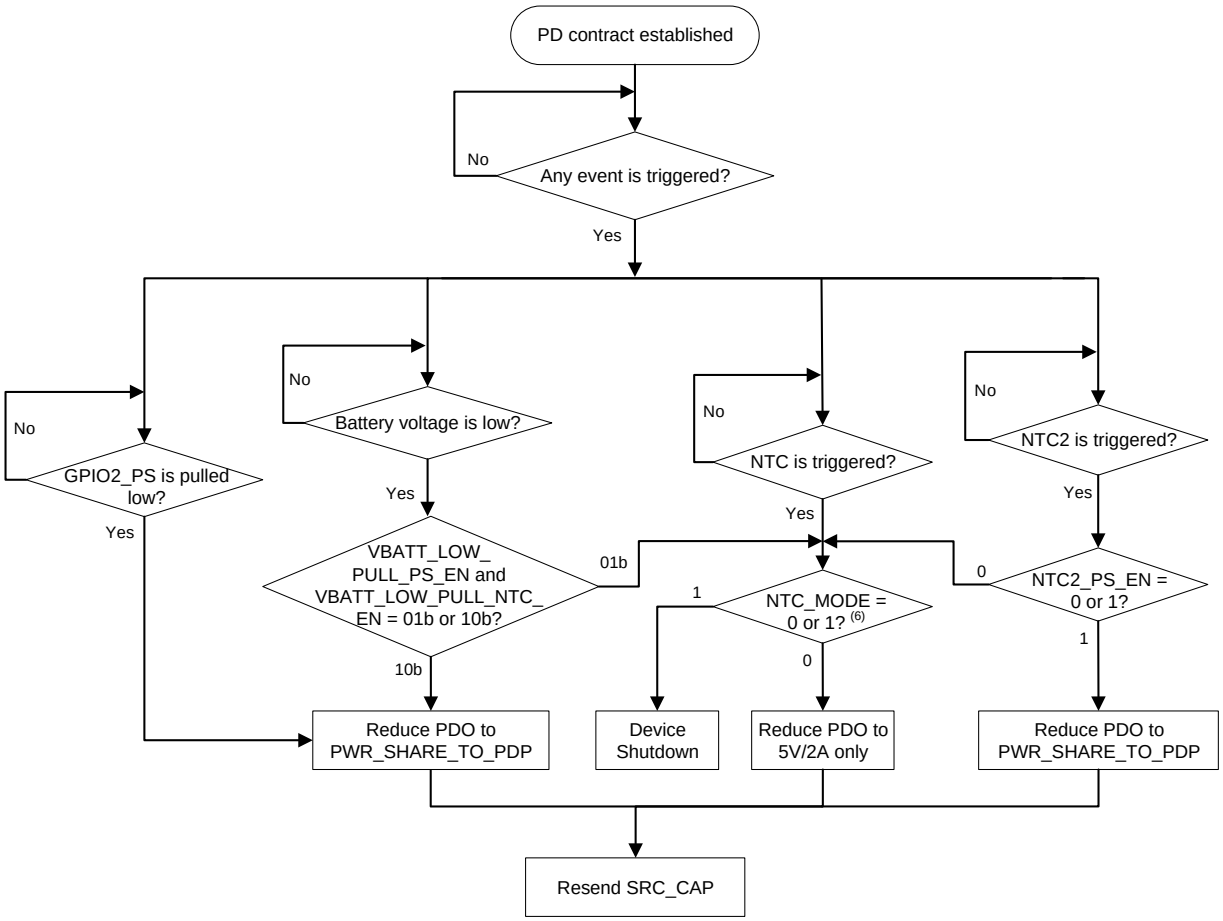


Figure 16: PDO Reduce Logic and State Machine

Note:

6) When NTC and PWR_SHARE_TO_PDP events (GPIO2_PS pulls low, battery voltage low or NTC2) are triggered at the same time, the PDO lists are updated based on the NTC set-up. If NTC_MODE = 1, the device shuts down; if NTC_MODE = 0, the PDO list is updated to 5V/2A.

I²C Transfer Data

Every byte put on the SDA line must be 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. The master generates the acknowledge-related clock pulse. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable (low) during the high period of this clock pulse.

Figure 17 shows the data transfer format. After the start condition (S), a slave address is sent. This address is 7 bits long followed by an 8th data direction bit (R/W). A 0 indicates a transmission (write), while a 1 indicates a request for data (read). A data transfer is always terminated by a stop condition (P) generated by the master. For a master to continue communicating on a bus, it can generate a repeated start condition (Sr) and address another slave without first generating a stop condition.

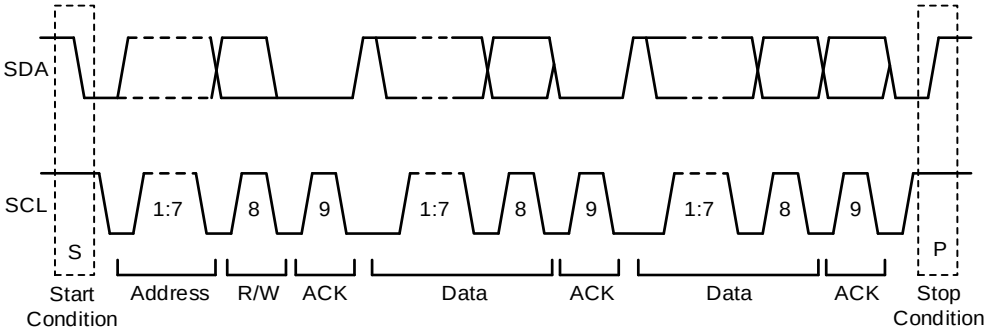


Figure 17: Complete Data Transfer

The MPQ5031 includes a full I²C slave controller. The I²C slave fully complies with the I²C specification requirements. It requires a start condition, valid I²C address, register address byte, and data byte for a single data update. After receiving each byte, the MPQ5031 acknowledges the byte by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address then selects the MPQ5031, and the MPQ5031 performs an update on the falling edge of the LSB byte.

Figure 18 shows an example of an I²C read and write command.

a) I²C Write Word

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	Wr	A	I2C Register Address	A	Data Byte Low	A	Data Byte High	A	P

b) I²C Read Word

1	7	1	1	8	1	1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	I2C Register Address	A	S	Slave Address	Rd	A	Data Byte Low	A	Data Byte High	A	P

Figure 18: I²C Read and Write

I²C REGISTER MAP

I²C Slave, I2C_MODE = VCC

Add (Hex)	Name	R/W	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00	PDO_TYPE	R/W	OTP_SOFTWARE_REVISION_NO (7)						RESERVED		PDO5_EN (7)	PDO4_EN (7)	PDO3_EN (7)	PDO2_EN (7)	PDO5_TYPE (7)	PDO4_TYPE (7)	PDO3_TYPE (7)	PDO2_TYPE (7)
01	PDO_V1	R	RESERVED						PDO1_VOLTAGE_SETTING (5V)									
02	PDO_I1	R/W	OTP_SUFFIX_CODE (7)						PDO1_CURRENT_SETTING (7) (3A default)									
03	PDO_V2	R/W	PDO2_VOLTAGE_SETTING (7) (9V default)															
04	PDO_I2	R/W	RESERVED						PDO2_CURRENT_SETTING (7) (3A default)									
05	PDO_V3	R/W	PDO3_VOLTAGE_SETTING (7) (15V default)															
06	PDO_I3	R/W	RESERVED						PDO3_CURRENT_SETTING (7) (3A default)									
07	PDO_V4	R/W	PDO4_VOLTAGE_SETTING (7) (20V default)															
08	PDO_I4	R/W	RESERVED						PDO4_CURRENT_SETTING (7) (3A default)									
09	PDO_V5	R/W	PDO5_VOLTAGE_SETTING (7) (3.3V to 21V default)															
0A	PDO_I5	R/W	RESERVED						PDO5_CURRENT_SETTING (7) (3A default)									
0B	CTL1	R/W	VBATT_LOW_PULL_PS_EN (7)	LEGACY_CHARGING_MODE_SEL_1 (7)	NTC2_PS_EN (7)	CDP_EN (7)	LEGACY_CHARGING_MODE_SEL_0 (7)	RESERVED	VBATT_LOW_PULL_NTC_EN (7)	I2C_SLAVE_ADDRESS (7)					TYPE-C_MODE (7)	SLAVE_DEVICE_SEL (7)		
0C	CTL2	R/W	HD RST	SEND_SRC_CAP	USB SUSPEND (7)	USB COMMUNICATE (7)	LPS (7)		TOUCH_CURRENT (7)		TOUCH_TEMP (7)				UNCUKEXTMSG (7)	RESERVED	SRC_CAP (7)	VDRV_EN (7)
0D	CTL3	R/W	PFM_PWM (7)	FREQ_DITHER (7)	EN_OFF_TIMER (7)			GPIO4 (7)	GPIO3 (7)		GPIO2 (7)					GPIO1 (7)		
0E	CTL4	R/W	NTC_MODE (7)	VBUS_UV_THD (7)	RESERVED			VDRV (7)	GPIO7 (7)		GPIO6 (7)					GPO5 (7)		
0F	PWR SHA	R/W	PWR_SHARE_OUTPUT_THLD (7)								POWER_SHARE_TO_PDP_THLD (7)							
10	STATUS 1	R	PPS_OUTPUT_VOLTAGE											BATTERY_SHORT	ANALOG_DETECTED_TYPEC	ANA_OTP	PREVIOUSLY_PD_CONNECTED	LOAD_SHED DING
11	STATUS 2	R	RESERVED	CABLE_CAP	CAPABILITY_MISMATCH	OBJECT_POSITION			SINK_REQUEST_CURRENT_APDO								RESERVED	
12	ID	R	VENDER ID:1000				RESERVED											
14	CLK_ON	R/W	Enable control of the digital CLK: 0x55AA to enable the digital clock, 0x0000 to disable the clock															

Note:

7) These registers are OTP-configurable. When the MPQ5031 VCC voltage rises above the UVLO rising threshold, the OTP contents are loaded to the I²C register.

REGISTER DESCRIPTION

PDO_TYPE

PDO1 is always enabled, and is fixed as a 5V fixed-power data object (PDO).

Address: 0x00
Type: Read/Write

Bits	Name	Description
D[15:10]	OTP_SOFTWARE_REVISION_NO	Determined by MPS.
D[7]	PDO5_EN	Enables PDO5's power object. The bit is set to 1b by default. 0b: Disabled 1b: Enabled
D[6]	PDO4_EN	Enables PDO4's power object. The bit is set to 1b by default. 0b: Disabled 1b: Enabled
D[5]	PDO3_EN	Enables PDO3's power object. The bit is set to 1b by default. 0b: Disabled 1b: Enabled
D[4]	PDO2_EN	Enables PDO2's power object. The bit is set to 1b by default. 0b: Disabled 1b: Enabled
D[3]	PDO5_TYPE	Sets PDO5's power object. The bit is set to 1b by default. 0b: Fixed PDO 1b: APDO
D[2]	PDO4_TYPE	Sets PDO4's power object. The bit is set to 0b by default. 0b: Fixed PDO 1b: APDO
D[1]	PDO3_TYPE	Sets PDO3's power object. The bit is set to 0b by default. 0b: Fixed PDO 1b: APDO
D[0]	PDO2_TYPE	Sets PDO2's power object. The bit is set to 0b by default. 0b: Fixed PDO 1b: APDO

PDO_V1

Address: 0x01
Type: Read-Only

Bits	Name	Description
D[9:0]	PDO1_VOLTAGE_SETTING	This bit sets PDO1's output voltage in 50mV units. Fixed to 0001 1001 00b (5V).

PDO_I1

Address: 0x02
Type: Read/Write

Bits	Name	Description
D[15:10]	OTP_SUFFIX_CODE	Determined by MPS.
D[9:0]	PDO1_CURRENT_SETTING	Sets PDO1's maximum output current in 10mA units. The default is 3A. When these bits are set >3A, the MPQ5031 first checks the cable current rating. If set to 5A, send a >3A setting. If the cable capability is 3A, only send a 3A maximum current capability.

PDO_V2

Address: 0x03
Type: Read/Write
Default PDO TYPE: Fixed PDO

If PDO2_TYPE is set to 0b (fixed PDO):

Bits	Name	Description
D[15:10]	RESERVED	Reserved. Set to 0b.
D[9:0]	PDO2_VOLTAGE_SETTING	Sets PDO2's output voltage in 50mV units. The default is 9V.

If PDO2_TYPE is set to 1b (APDO):

Bits	Name	Description
D[15:8]	PDO2_MAXIMUM_VOLTAGE	Sets PDO2's maximum voltage in 100mV increments. The absolute maximum value is 21V.
D[7:0]	PDO2_MINIMUM_VOLTAGE	Sets PDO2's minimum voltage in 100mV increments.

PDO_I2

Address: 0x04
Type: Read/Write
Default PDO TYPE: Fixed PDO

If PDO2_TYPE is set to 0b (fixed PDO):

Bits	Name	Description
D[15:10]	RESERVED	Reserved. Set to 0b.
D[9:0]	PDO2_CURRENT_SETTING	Sets PDO2's maximum output current setting in 10mA units. The default is 3A. When these bits are set >3A, the MPQ5031 first checks the cable current rating. If set to 5A, send a >3A setting. If the cable capability is 3A, only send a 3A maximum current capability.

If PDO2_TYPE is set to 1b (APDO):

Bits	Name	Description
D[15:7]	RESERVED	Reserved. Set to 0b.
D[6:0]	PDO2_CURRENT_SETTING	Sets PDO2's maximum current in 50mA increments. When these bits are set >3A, the MPQ5031 first checks the cable current rating. If set to 5A, send a >3A setting. If the cable capability is 3A, only send a 3A maximum current capability.

PDO_V3

Address: 0x05
Type: Read/Write
Default PDO TYPE: Fixed PDO

If PDO3_TYPE is set to 0b (fixed PDO):

Bits	Name	Description
D[15:10]	RESERVED	Reserved. Set to 0b.
D[9:0]	PDO3_VOLTAGE_SETTING	Sets PDO3's output voltage in 50mV units. The default is 15V.

If PDO3_TYPE is set to 1b (APDO):

Bits	Name	Description
D[15:8]	PDO3_MAXIMUM_VOLTAGE	Sets PDO3's maximum voltage in 100mV increments. The absolute maximum value is 21V.
D[7:0]	PDO3_MINIMUM_VOLTAGE	Sets PDO3's minimum voltage in 100mV increments.

PDO_I3

Address: 0x06
Type: Read/Write
Default PDO TYPE: Fixed PDO

If PDO3_TYPE is set to 0b (fixed PDO):

Bits	Name	Description
D[15:10]	RESERVED	Reserved. Set to 0b.
D[9:0]	PDO3_CURRENT_SETTING	Sets PDO3's maximum output current in 10mA units. The default is 3A. When these bits are set >3A, the MPQ5031 first checks the cable current rating. If set to 5A, send a >3A setting. If the cable capability is 3A, only send a 3A maximum current capability.

If PDO3_TYPE is set to 1b (APDO):

Bits	Name	Description
D[15:7]	RESERVED	Reserved. Set to 0b.
D[6:0]	PDO3_CURRENT_SETTING	Sets PDO3's maximum current in 50mA increments. When these bits are set >3A, the MPQ5031 first checks the cable current rating. If it is set to 5A, send a >3A setting. If the cable capability is 3A, only send a 3A maximum current capability.

PDO_V4

Address: 0x07
Type: Read/Write
Default PDO TYPE: Fixed PDO

If PDO4_TYPE is set to 0b (fixed PDO):

Bits	Name	Description
D[15:10]	RESERVED	Reserved. Set to 0b.
D[9:0]	PDO4_VOLTAGE_SETTING	Sets PDO4's output voltage in 50mV units. The default is 20V.

If PDO4_TYPE is set to 1b (APDO):

Bits	Name	Description
D[15:8]	PDO4_MAXIMUM_VOLTAGE	Sets PDO4's maximum voltage in 100mV increments. The absolute maximum value is 21V.
D[7:0]	PDO4_MINIMUM_ VOLTAGE	Sets PDO4's minimum voltage in 100mV increments.

PDO_I4

Address: 0x08
Type: Read/Write
Default PDO TYPE: Fixed PDO

If PDO4_TYPE is set to 0b (fixed PDO):

Bits	Name	Description
D[15:10]	RESERVED	Reserved. Set to 0b.
D[9:0]	PDO4_CURRENT_ SETTING	Sets PDO4's maximum output current in 10mA units. The default is 3A. When these bits are set >3A, the MPQ5031 first checks the cable current rating. If set to 5A, send a >3A setting. If the cable capability is 3A, only send a 3A maximum current capability.

If PDO4_TYPE is set to 1b (APDO):

Bits	Name	Description
D[15:7]	RESERVED	Reserved. Set to 0b.
D[6:0]	PDO4_CURRENT_ SETTING	Sets PDO4's maximum current in 50mA increments. When these bits are set >3A, the MPQ5031 first checks the cable current rating. If set to 5A, send a >3A setting. If the cable capability is 3A, only send a 3A maximum current capability.

PDO_V5

Address: 0x09
Type: Read/Write
Default PDO TYPE: APDO

If PDO5_TYPE is set to 0b (fixed PDO):

Bits	Name	Description
D[15:10]	RESERVED	Reserved. Set to 0b.
D[9:0]	PDO5_VOLTAGE_ SETTING	Sets PDO5's output voltage in 50mV units.

If PDO5_TYPE is set to 1b (APDO):

Bits	Name	Description
D[15:8]	PDO5_MAXIMUM_ VOLTAGE	Sets PDO5's maximum voltage in 100mV increments. The default is 21V.
D[7:0]	PDO5_MINIMUM_ VOLTAGE	Sets PDO5's minimum voltage in 100mV increments. The default is 3.3V.

PDO_I5

Address: 0x0A
Type: Read/Write
Default PDO TYPE: APDO

If PDO5_TYPE is set to 0b (fixed PDO):

Bits	Name	Description
D[15:10]	RESERVED	Reserved. Set to 0b.
D[9:0]	PDO5_CURRENT_SETTING	Sets PDO5's maximum output current in 10mA units. When these bits are set >3A, the MPQ5031 first checks the cable current rating. If set to 5A, send a >3A setting. If the cable capability is 3A, only send a 3A maximum current capability.

If PDO5_TYPE is set to 1b (APDO) (default):

Bits	Name	Description
D[15:7]	RESERVED	Reserved. Set to 0b.
D[6:0]	PDO5_CURRENT_SETTING	Sets PDO5's maximum current in 50mA increments. The default is 3A. When these bits are set >3A, the MPQ5031 first checks the cable current rating. If set to 5A, send a >3A setting. If the cable capability is 3A, only send a 3A maximum current capability.

CTL1

Address: 0x0B
Type: Read/Write

<table>
<tr><th>Bits</th><th>Name</th><th>Description</th></tr>
<tr><td>D[15]
D[8]</td><td>VBATT_LOW_PULL_PS_EN
VBATT_LOW_PULL_NTC_EN</td><td>Controls battery voltage low detection if GPIO2 or GPIO4 is set to VBATT_SENSE. These bits are set to 01b by default. These bits cannot be set to 11b. The table below lists the configurations.
<table>
<tr><td>D[15]: VBATT_LOW_PULL_PS_EN</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>D[8]: VBATT_LOW_PULL_NTC_EN</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>PDO List when Battery Voltage Low Condition Occurs</td><td>PDO list is based on register PDO_TYPE setting.</td><td>Update PDO1 to 5V/2A, other PDOs are disabled.</td><td>Disable the PDO with a power rating equal to or exceeding PWR_SHARE_TO_PDP</td></tr>
</table></td></tr>
<tr><td>D[14]
D[11]</td><td>LEGACY_CHARGING_MODE_SEL1
LEGACY_CHARGING_MODE_SEL0</td><td>The MPQ5031 supports different legacy charging modes, such as QC3.0, HUAWEI FCP, BC1.2 DCP and Apple divider mode. The table below lists different charging mode selections. These bits are set to 01b by default.
<table>
<tr><td>D[14]: LEGACY_CHARGING_MODE_SEL_1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>D[11]: LEGACY_CHARGING_MODE_SEL_0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>DP/DM Charging Mode</td><td>All modes are active</td><td>Only DCP is active. No Apple divider mode or QC mode. Short the DP and DM pins.</td><td>Apple divider mode/DCP mode is active.</td><td>Only DCP is active. No Apple divider mode or QC mode. Short the DP and DM pins.</td></tr>
</table></td></tr>
<tr><td>D[13]</td><td>NTC2_PS_EN</td><td>Enables the NTC2 power share function. This bit is set to 0b by default.

0: Disabled
1: Enabled</td></tr>
<tr><td>D[12]</td><td>CDP_EN</td><td>Enables CDP mode. This bit is set to 0b by default.

0b: Non-CDP mode, charging-only protocol on DP and DM pins
1b: CDP mode enabled. The CDP protocol is enabled on the DP and DM pins. QC, Apple divider, and DCP modes are disabled (set LEGACY_CHARGING_MODE_SEL = 11b)</td></tr>
<tr><td>D[10:9]</td><td>RESERVED</td><td>Reserved. Always write 00b to these bits.</td></tr>
<tr><td>D[7:4]</td><td>I2C_SLAVE_ADDRESS</td><td>Sets the slave I²C address. This bit is set to 1000b by default.</td></tr>
</table>

D[3]	TYPE-C_MODE	Selection bit for 3A or 1.5A Type-C mode. This bit is set to 0b by default. In 5V/3A Type-C mode, the pull-up current (R_P) is 330μA, and the detection range (Rd) is between 0.8V and 2.6V. 0: 3A Type-C mode 1: 1.5A Type-C mode
D[2:0]	SLAVE_DEVICE_SEL	Selects the power device that is incorporated with the MPQ5031. These bits are set to 001b by default. 000b: MPQ421x 001b: MPQ423x, MPQ426x 010b: MP28167-A 011b: MPQ4272-Page 0 100b: MPQ4272-Page 1 101b: For Non-I^2C DC/DC converters. PDO2_SEL is pulled low when PDO2 is selected. PDO2_SEL and PDO3_SEL both pull low when PDO3 is selected. PDO2_SEL, PDO3_SEL, and PDO4_SEL all pull low when PDO4 is selected. EN_OUT = low, EN_OUT_MID = low during hard reset and detach events. For more details, see Figure 10 on page 20. Others values are reserved.

CTL2

The message bits/bytes referenced in bits D[13:3] are defined in the USB Power Delivery Specification Revision 3.0, Version 2.0, which can be downloaded from the official USB website at https://usb.org/.

Address: 0x0C
Type: Read/Write

Bits	Name	Description
D[15]	HDRST	Sends the hard reset command. This bit is set to 0b by default. 0b: Normal state 1b: Send a hard reset command to the sink. After the HDRST message is sent, this bit auto-resets to 0b
D[14]	SEND_SRC_CAP	Sends the source capability command. The PD engine only sends a SOURCE_CAP message while in the ready state. This bit is set to 0b by default. 0b: Normal state 1b: Send source capability. After SOURCE_CAP is sent, this bit auto-resets to 0b When there is a PDO configuration change in I^2C registers 0x01~0x09, SEND_SRC_CAP should be set to make the new PDO take effect. After sending a new source capability, the MPQ5031 clears this bit. Change the 0x00 register for the new PDO to take effect immediately.
D[13]	USB SUSPEND	Sets whether USB suspend functions are supported. This bit is set to 0b by default. This bit is defined in Fixed Supply PDO message bit[28]. 0b: USB suspend is not supported 1b: USB suspend is supported
D[12]	USBCOMMUNICATE	Sets whether USB communication capabilities are supported. This bit is set to 0b by default. This bit is defined in Fixed Supply PDO message bit[26]. 0b: USB communication capabilities are not supported 1b: USB communication capabilities are supported
D[11:9]	LPS	LPS compliant when set. These bits are defined in SOURCE_CAPABILITIES_EXTENDED Message byte 12, bits[2:0]. These bits are set to 101b by default. D[11] = LPS bit D[10] = PS1 bit D[9] = PS2 bit

D[8:6]	TOUCH_CURRENT	Sets the touch current, bits[2:0]. These bits are defined in SOURCE_CAPABILITIES_EXTENDED Message byte 13, bits[2:0]. These bits are set to 000b by default. D[8] indicates touch current bit[2].
D[5:4]	TOUCH_TEMP	Sets the touch temperature default value to 0, 1, or 2. These bits are defined in SOURCE_CAPABILITIES_EXTENDED Message byte 20, bits[1:0]. These bits are set to 00b by default.
D[3]	UNCUKEXTMSG	Sets the unchunked extend message bit. This bit is defined in Fixed Supply PDO message bit[24]. This bit is set to 1b by default.
D[2]	RESERVED	Reserved. Always write 0b to this bit.
D[1]	SRC_CAP	Send source capability twice control bit when a PD2.0 device is attached. This bit is set to 0b by default. 0: Send source capability twice 1: Send source capability once
D[0]	VDRV_EN	Enables VDRV functions. This bit is set to 0b by default. 0b: Disable the VDRV output. VDRV has 5.1kΩ pull-down resistor when it is disabled 1b: Enable VDRV functions

CTL3

Address: 0x0D
Type: Read/Write

Bits	Name	Description
D[15]	PFM_PWM	Sets the MP28167-A and MPQ421x operation modes. This bit is set to 1b by default. 0b: PFM mode. If the MP28167-A is selected as the I^2C slave, the MP28167-A's 0x04 register D[4] = 0. If the MPQ421x is selected as the I^2C slave, the MPQ421x's 0x02 register D[2] = 0. 1b: PWM mode. If the MP28167-A is selected as the I^2C slave, then 0x04 register D[4] = 1. If the MPQ421x is selected as the I^2C slave, then the its 0x02 register D[2] = 1
D[14]	FREQ_DITHER	Enables frequency dithering for the MPQ421x. This bit is set to 0b by default. 0b: Disabled (fixed-frequency mode). If the MPQ421x is selected as the I^2C slave, the MPQ421x's 0x02 register D[4] = 0 1b: Enabled. If the MPQ421x is selected as the I^2C slave, the MPQ421x's 0x02 register D[4] = 1. For other devices like the MPQ4230, ignore this bit
D[13:11]	EN_OFF_TIMER	Sets the EN off time delay. Only valid when GPIO4 is set for EN functions. These bits are set to 010b by default. 000b: No delay 001b: 10 minutes 010b: 22 minutes 011b: 40 minutes 100b: 80 minutes 101b: 120 minutes
D[10:9]	GPIO4	Configures the function of the GPIO4 pin. These bits are set to 00b by default. 00b: Reserved. This pin can be floated or tied to ground 01b: EN function. When the external input is >1.4V, the MPQ5031 is enabled. When the external input is <1.2V, the MPQ5031 is disabled in a low I_Q state. EN_OFF_TIMER can configure the off delay 10b: NTC2 function. Refer to the NTC2 description on page 22. 11b: The GPIO4 pin functions as the VBATT_SENSE pin, and monitors the battery voltage. If the battery voltage is low (resistor divider ratio is 1/10), then the PD updates the source capability. The internal comparator falling threshold is 1.1V, and the rising threshold is 1.15V with a 20µs deglitch time. This comparator operates when VCC exceeds the under-voltage lockout (UVLO) threshold after a 5s delay time

D[8:6]	GPIO3	Configures the function of GPIO3 pin. This low-voltage pin supports 5.5V operation and has an internal ESD Zener diode. These bits are set to 000b by default. 000b: I2C_ARB function. Tri-state input or output to avoid having two I^2C masters. This function has a similar structure to GPIO2 when it is set to PWE_SHARE. See the I^2C Arbitration section on page 23 for more details 001b: EN function. When the external input is >1.4V, the MPQ5031 is enabled. When the external input is <1.2V, the MPQ5031 is disabled in a low I_Q state 010b: ATTACH function. GPIO3 is pulled low once a Type-C port is attached. Open-drain structure 011b: EN_OFF_DELAY_OUT function. When EN goes low, this pin still outputs high. It changes to a floating state after 22 minutes. This signal can be used to control the upstream DC/DC converter's enable pin 100b: POL output 101b: PDO3_SEL_OUT. This is an open-drain output. When PDO3 is selected, this pin pulls low. The pull-down speed is very slow (typically 1ms to drop from 100kΩ to 2Ω) 110b: ISENS+ function. This pin is used for line drop compensation when the MPQ4214 is selected. Connect ISENS+ to the MPQ4214's COMP pin to sense current information 111b: IPWM function. The PWM output sets the external buck-boost's PPS CC current limit. This pin must be pulled up externally. The PWM signal frequency is 10kHz
D[5:3]	GPIO2	Configures the function of the GPIO2 pin. This is a low-voltage pin. These bits are set to 110b by default. 000b: QC_12 function. For QC2.0 mode, this pin is used to enable QC $12V_{OUT}$ 001b: POL output. This is an open-drain output to indicate the plug orientation. When CC1 is selected as the CC line, the POL is pulled low. When CC2 is selected as the CC line, the POL is an open drain 010b: GPIO2 is pulled low 110b: PWR_SHARE function. See the Power Sharing Function section on page 23 for more details 111b: VBATT_SENSE pin
D[2:0]	GPIO1	Configures the function of the GPIO1 pin. It is a low-voltage pin that supports 5.5V operation. These bits are set to 001b by default. 000b: PDO2_SEL_OUT. This pin is an open-drain output. When PDO2 is selected, this pin is pulled low. The pull-down speed is very slow (typically 1ms to drop from 100kΩ to 2Ω). For QC2.0 mode, this pin is used to enable $9V_{OUT}$ (QC logic adds this output signal as well) 001b: Interrupt input pin. This is a high-impedance pin that monitors the input signal. In real applications, it should be connected to the external DC/DC converter's ALT pin to get interruption information from the I^2C slave 010b: GPIO1 is pulled low 011b: GPIO1 is an open drain 100b: VSEL1. Output voltage selection pin. See the GPIO Summary section on page 38 for more details 100b~111b: Reserved

CTL4

Address: 0x0E
Type: Read/Write

Bits	Name	Description
D[15]	NTC_MODE	Sets the NTC behavior. This bit is set to 0b by default. 0b: If NTC is triggered, the MPQ5031 initiates load-shedding 1b: If NTC is triggered, the MPQ5031 shuts down. This process is similar to internal thermal shutdown, and the ENO_MID output is set

D[14]	VBUS_UV_THD	Sets the VBUS_P under-voltage (UV) threshold. Set the threshold to 2.97V when the minimum APDO voltage is 3.3V, and to 4.5V when the minimum APDO voltage is 5V. This bit is set to 0b by default. 0b: The VBUS_P falling threshold is 2.97V 1b: The VBUS_P falling threshold is 4.5V
D[10:9]	VDRV	Sets the VDRV pin function. These bits are set to 00b by default. 00b: VDRV function. This pin is the external N-channel MOSFET gate driver signal. When the sink is attached, VDRV drives the external N-channel MOSFET to turn on. Then power will flow from the DC/DC output to the sink. When the sink is detached, VDRV drives the external N-channel MOSFET to turn off to isolate the power path 01b: VDRV1 function. See Figure 10 on page 20 for the timing sequence
D[8:6]	GPIO7	Configures the GPIO7 pin. It is a low-voltage pin. These bits are set to 011b by default. 000b: DISCHG pin. Output discharge function. The discharge function only turns on for 200ms, then turns off. DISCHG only outputs a control signal. An external N-channel MOSFET should be added between VBUS and GND for this function 001b: ATTACH function. This pin is pulled low once a Type-C port is attached. Open-drain structure 011b: EN_OUT_MID function. If there is a hard reset or a detach event, this pin clamps the voltage to 1V 100b: EN_OUT. This output controls the upstream DC/DC output. If a hard reset occurs, the PD engine pulls this pin to GND. In normal operation, this pin is an open drain output 101b: ADJ function. This function is used for MPQ421x line drop compensation. It sinks a 2μA current when the COMP voltage >1.2V
D[5:3]	GPIO6	Configures the GPIO6 pin. These bits are set to 110b by default. 000b: PDO4_SEL_OUT. When PDO4 is selected, this bit is an open drain output 001b: VSEL2. Output voltage selection pin 010b: POL output. Open-drain output to indicate the plug orientation. If CC1 is selected as the CC line, then the POL is pulled low. If CC2 is selected as the CC line, then the POL is an open drain 011b: EN function. When the external input is >1.4V, the MPQ5031 is enabled. When the external input is <1.2V, the MPQ5031 is disabled in a low I_Q state 100b: SYNC_OUT2. PWM output to sync external buck-boost's switching frequency. It is an open-drain output with a 25% duty cycle, 450kHz frequency, and 180° phase delay based on GPIO5 101b: NTC2 function. See the NTC2 description on page 22 for more details 110b: I2C_SLV_SDA. This pin is an I^2C slave data pin
D[2:0]	GPIO5	Configures the GPIO5 pin. These bits are set to 000b by default. 000b: I2C_SLV_SCL. This pin is the I^2C slave's clock pin 001b: IPWM. The PWM output sets the external buck-boost's PPS CC current limit. It should be internally pulled up to 1.8V with a 2kΩ resistor. The PWM signal frequency is 10kHz 010b: SYNC_OUT1. This is the PWM output to sync the external buck-boost's switching frequency. It is an open-drain output with a 25% duty cycle, 250kHz frequency, and 0° phase delay 011b: This is the PWM output to sync the external buck-boost's switching frequency. It is an open-drain output with a 25% duty cycle, 350kHz frequency, and 0° phase delay 100b: SYNC_OUT1. This is the PWM output to sync the external buck-boost's switching frequency. It is an open-drain output with a 25% duty cycle, 450kHz frequency, and 0° phase delay 101b: ATTACH function. This pin is pulled low once a Type-C port is attached. It has an open drain structure 111b: VBUS_UV_FIXPDO. This pin is a VBUS voltage detection input. Connect a 1/5 resistor divider to VBUS

PWRSHA

Address: 0x0F
Type: Read/Write

Bits	Name	Description
D[15:8]	PWR_SHARE_ OUTPUT_THLD	Sets the threshold of the sink-requested PDO power rating. If the sink-requested PDO power rating is equal to or higher than this threshold, the GPIO2 pin (if GPIO2 is set to PWR_SHARE) pulls low. The default value is 0x3C (60W). 0x01: 1W 0xFF: 255W
D[7:0]	PWR_SHARE_ INPUT_TO_PDP_ THLD	Sets the port's PD power rating. If the GPIO2 pin (if GPIO2 is set to PWR_SHARE) is pulled low, the battery voltage is low (VBATT_LOW_PULL_PS_EN = 1b), or NTC2 is triggered (NTC2_PS_EN = 1b), all PDOs with a power rating equal to or higher than this threshold are disabled. The default value is 0x3C (60W). 0x01: 1W 0xFF: 255W

STATUS1

Address: 0x10
Type: Read-Only
This register is read clear.

Bits	Name	Description
D[15:5]	PPS_OUTPUT_ VOLTAGE	Records the sink requested for PPS VOUT. In 20mV. This bit is only valid when the selected PDO is APDO.
D[4]	BATTERY_ SHORT	This bit is set if CCx, DP, or DM is shorted to the input battery.
D[3]	ANALOG_ DETECTED_ TYPEC	Detects if a Type-C device is attached or unattached.
D[2]	ANA_OTP	Indicates if the MPQ5031 enters over-temperature protection (OTP), excluding thermal shutdowns caused by NTC or NTC2. It also indicates if the external power device enters OTP (the digital side provides the OTP information for the external device).
D[1]	PREVIOUSLY_ PD_ CONNECTED	Indicates whether the MPQ5031 has a PD contract.
D[0]	LOAD_ SHEDDING	Indicates if the device has entered load-shedding (see Figure 12 on page 22 for more details).

STATUS2

Address: 0x11
Type: Read-Only
Read clear.

Bits	Name	Description
D[15]	RESERVED	Reserved.
D[14]	CABLE_CAP	1b: The cable can handle 5A 0b: The cable can only handle 3A
D[13]	CAPABILITY_ MISMATCH	A sink request sets the "Capability Mismatch" bit.

D[12:10]	OBJECT_ POSITION	When a sink is attached, these bits indicate the sink-requested PDO position. 000b: Non-PD device is attached 001b: Sink requested PDO1 (5V PDO) 010b: Sink requested PDO2 011b: Sink requested PDO3 100b: Sink requested PDO4 101b: Sink requested PDO5
D[9:2]	SINK_REQUEST _CURRENT_ APDO	Sink-requested APDO current in 50mA units.
D[1:0]	RESERVED	Reserved.

ID

Address: 0x12
Type: Read-Only

Bits	Name	Description
D[15:12]	VENDOR_ID	Vendor ID. The default is 1000b.
D[11:0]	RESERVED	Reserved.

CLK_ON

Address: 0x14
Type: Read/Write

Bits	Name	Description
D[15:0]	CLK_ON	Enables the digital CLK. Set these bits to 0x55AA to enable the digital clock; set them to 0x0000 to disable the clock. When GPIO5 and GPIO6 are configured as I2C_SLV_SCL and I2C_SLV_SDA, the digital CLK should be enabled when sending I^2C write commands via GPIO5/GPIO6, then the digital CLK should be disabled after the I^2C command ends. A digital CLK does not need to be enabled when only reading the I^2C register via GPIO5 and GPIO6.

I²C Bus Slave Address

The slave address is a 7-bit address followed by an 8th data direction bit (read or write). The A4 to A1 bits are configurable via the OTP.

	A7	A6	A5	A4	A3	A2	A1
Setting Value	0	1	0	1 (8)	0 (8)	0 (8)	0 (8)

Note:

8) By default, the slave address is 0x28, A[7:1] = 0101 000.

GPIO Summary

For more details on the GPIO functions, see the CTL3 register on page 33 and the CTL4 register on page 34.

Name	Function Options							
GPIO1	INT	PDO2_ SEL_OUT	VSEL1	-	-	-	-	-
GPIO2	PWR_ SHARE	QC_12	POL	VBATT_ SENSE	-	-	-	-
GPIO3	I2C_ARB	PDO3_ SEL_OUT	POL	EN_OFF_ DELAY_ OUT	ISENS+	IPWM (9)	ATTACH	EN
GPIO4	EN	NTC2	VBATT_ SENSE	-	-	-	-	-
GPIO5	SYNC_ OUT1	IPWM (9)	VBUS_ UV_ FIXPDO	I2C_SLV_ SCL	ATTACH	-	-	-
GPIO6	SYNC_ OUT2	PDO4_ SEL_OUT	VSEL2	I2C_SLV_ SDA	NTC2	POL	EN	-
GPIO7	DISCHG	EN_OUT	EN_OUT_ MID	ADJ	ATTACH	-	-	-
VDRV	VDRV	VDRV1	-	-	-	-	-	-

Note:

9) IPWM on GPIO3 must be pulled up externally. IPWM on GPIO5 is pulled up internally.

Table 8: V_{OUT} Voltage vs. GPIO Output for Non-I²C DC/DC Converter Use Case

V_{OUT}	PDO2_SEL_OUT (or QC_9)	QC_12	PDO3_SEL_OUT	PDO4_SEL_OUT
5V	Open drain	Open drain	Open drain	Open drain
9V	0	Open drain	Open drain	Open drain
12V	0	0	Open drain	Open drain
15V	0	Open drain	0	Open drain
20V	0	Open drain	0	0

Table 9: V_{OUT} Voltage vs. VSEL1, VSEL2 Output Status (10)

V_{OUT}	VSEL1	VSEL2
5V	Open drain	Open drain
9V	0	Open drain
15V	Open drain	0
20V	0	0
12V	100kΩ to GND	0

Notes:

10) VSEL1 and VSEL2 can be used to control the MP2491C's output voltage.

APPLICATION INFORMATION

PCB Layout Guidelines (11)

Efficient PCB layout is critical for stable operation and better ESD performance. A 2-layer or 4-layer layout is recommended. For the best results, refer to Figure 19 and follow the guidelines below:

1. Place the VCC and VDD decoupling capacitor as close to the VCC and VDD pins as possible.
2. Put 9 vias on the exposed pad of the IC. Connect the exposed pad to ground.
3. Place the ESD diodes as close to the IC as possible. Use short, direct, and wide traces to connect CC1, CC2, DP, and DM to the cathode of ESD diodes. Connect the anode of ESD diode to ground with multiple vias.
4. Use short, direct, and wide traces to connect CC1 and CC2 to the USB Type-C receptacle.

Notes:

11) The recommended layout is based on Figure 20 on page 41.

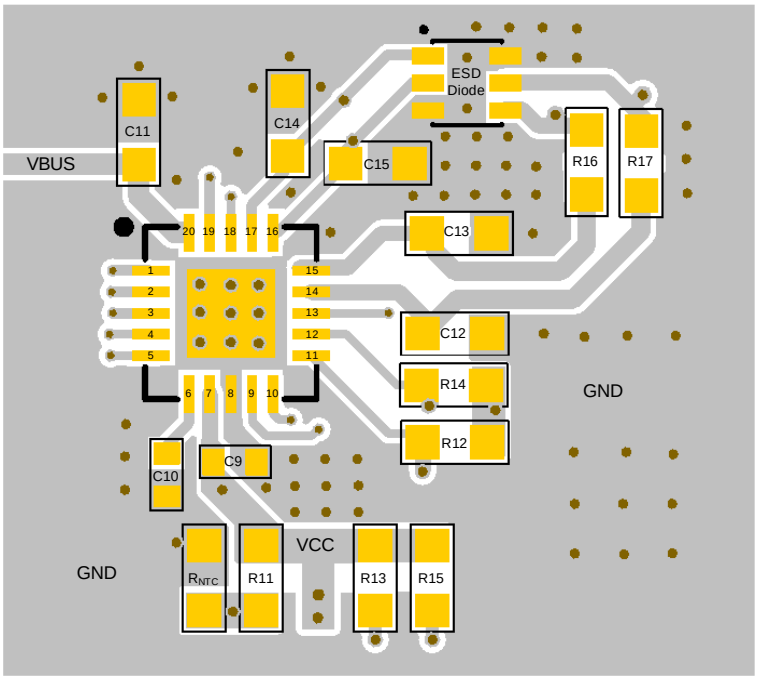


Figure 19: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

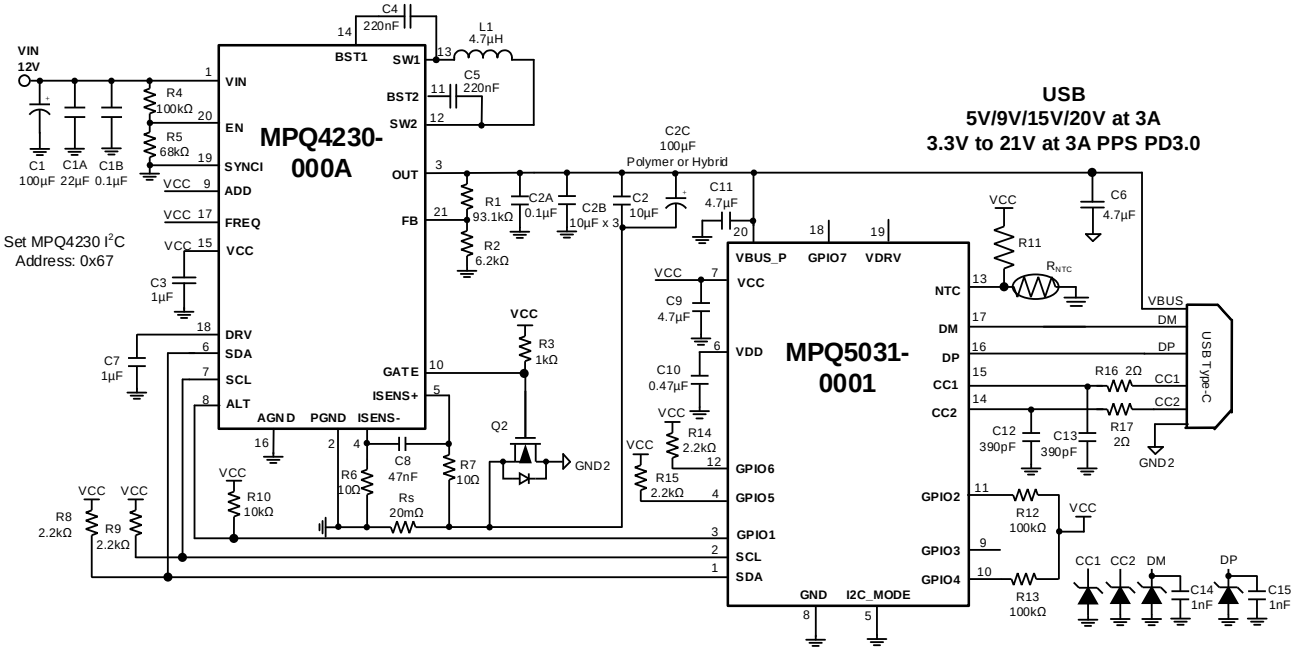


Figure 20: MPQ4230 + MPQ5031 for 60W PD Application (12)

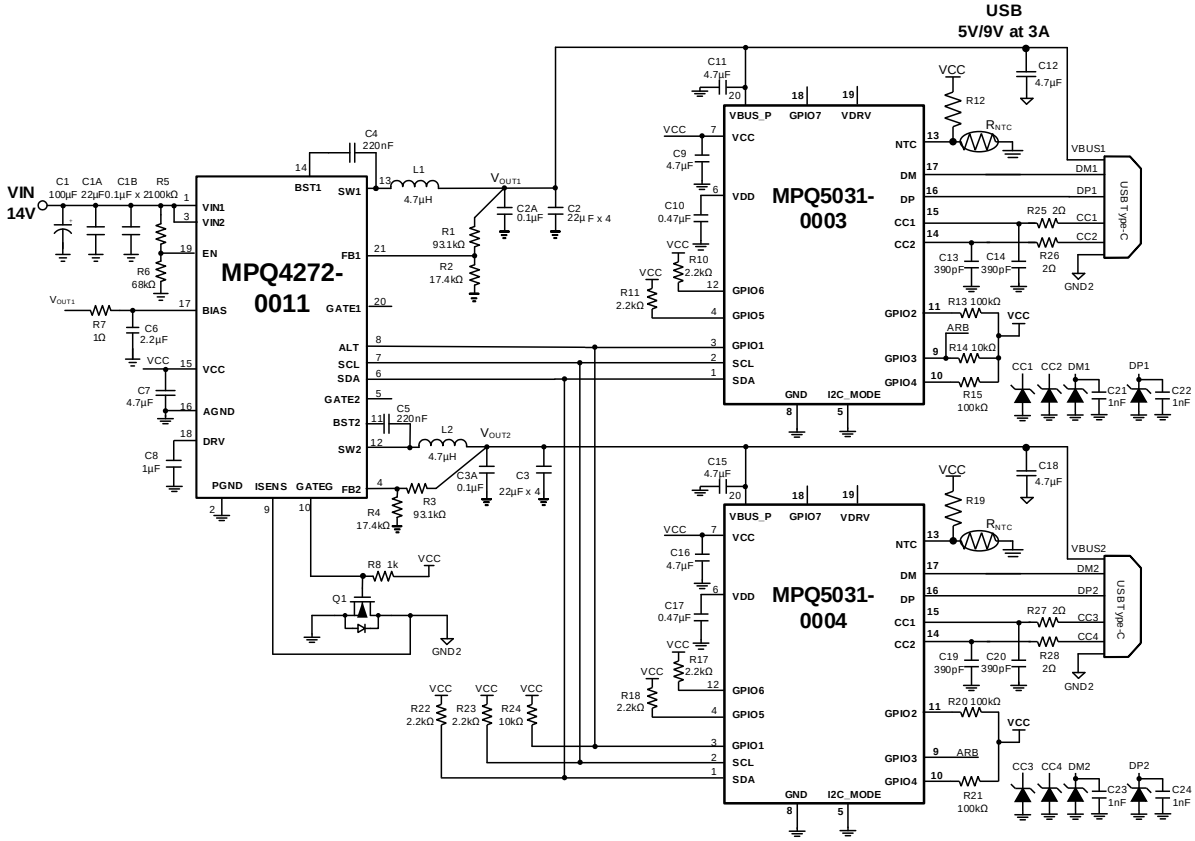


Figure 21: MPQ4272 + MPQ5031 for Dual-Port 27W PD Application (12)

Note:

12) A TVS and RC filter should be added to the DP/DM/CCx pins to ensure that they pass ±8kV/±15kV IEC Contact/Air Discharge ESD.

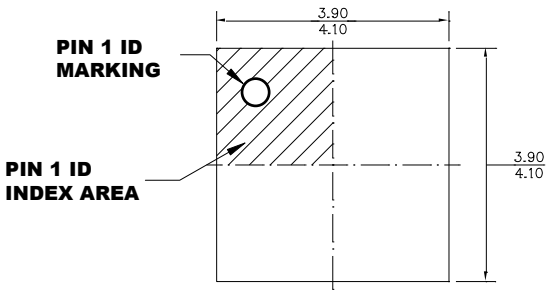
MPQ5031GRE-0001 CONFIGURATION TABLE

OTP Items	Enabled/Disabled	PDO Type	Voltage	Current
PDO1	Enabled	Fixed PDO	5V	3A
PDO2	1b: Enabled (default)	0b: Fixed PDO (default)	9V (default)	3A
PDO3	1b: Enabled (default)	0b: Fixed PDO (default)	15V (default)	3A
PDO4	1b: Enabled (default)	0b: Fixed PDO (default)	20V (default)	3A
PDO5	1b: Enabled (default)	1b: APDO (default)	3.3V to 21V (default)	3A

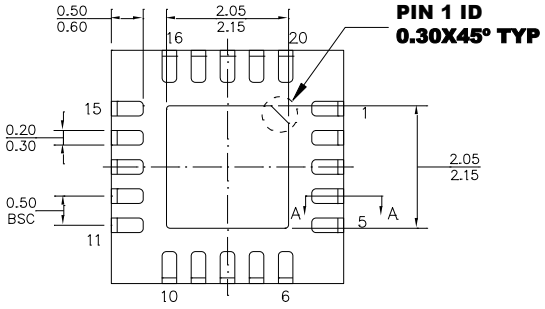
OTP Items	Description	Value
GPIO1	Configures the function of the GPIO1 pin.	001b: Interrupt input pin (default)
GPIO2	Configures the function of the GPIO2 pin.	110b: PWR_SHARE function (default)
GPIO3	Configures the function of the GPIO3 pin.	000b: I2C_ARB function (default)
GPIO4	Configures the function of the GPIO4 pin.	00b: Reserved (default)
GPIO5	Configures the function of the GPIO5 pin.	000b: I2C_SLV_SCL (default)
GPIO6	Configures the function of the GPIO6 pin.	110b: I2C_SLV_SDA (default)
GPIO7	Configures the function of the GPIO7 pin.	011b: EN_OUT_MID function (default)
VBATT_LOW_PULL_PS_EN	The PDO list is reduced based on PWR_SHARE_TO_PDP_THLD when a battery voltage low condition is triggered.	0b: Disabled (default)
VBATT_LOW_PULL_NTC_EN	Update the PDO list to 5V/2A. Other PDOs are disabled when a battery voltage low condition is triggered.	0b: Disabled
NTC2_PS_EN	Connect NTC2 to power share control.	0b: Disabled (default)
LEGACY_CHARGING_MODE_SEL	QC3.0/DCP short mode/Apple divider mode selection.	00b: All modes are active
CDP_EN	Enables for CDP mode.	0b: Non-CDP mode, charging only protocol on DP, DM pins (default)
I2C_SLAVE_ADDRESS	Sets the MPQ5031's I^2C slave address.	28H (default)
TYPE-C_MODE	Selects 3A or 1.5A Type-C mode.	0b: 3A Type-C mode (default)
SLAVE_DEVICE_SEL	Selects the power device incorporated with MPQ5031.	001b: MPQ423x, MPQ426x (default)
VDRV	Sets the VDRV pin function.	00b: VDRV function (default)
VDRV_EN	Enables the VDRV function.	0b: Disabled (default)
PFM_PWM	Sets the MP28167A and MPQ421x operation mode.	1b: PWM mode (default)
FREQ_DITHER	Enables frequency dithering for the MPQ421x.	0b: Fixed frequency mode (default)
EN_OFF_TIMER	Sets different EN off timers. Only valid when GPIO4 is set for EN functions.	010b: 20 minutes (default)
NTC_MODE	Sets the MPQ5031 behavior when NTC is triggered.	1b: The MPQ5031 shuts down
VBUS_UV_THD	Set the VBUS_P UV threshold.	0b: VBUS_P falling threshold is 2.97V (default)
PWR_SHARE_OUTPUT_THLD	Sets the sink-requested PDO power rating threshold.	60W (default)
PWR_SHARE_TO_PDP_THLD	Sets the threshold for PDO power rating.	60W (default)
USB SUSPEND	USB Suspend supported or not.	0b: Not supported (default)
USBCOMMUNICATE	USB Communication Capable or not.	0b: Not supported (default)
LPS	LPS compliant when set.	101b (default)
TOUCH_CURRENT	Sets the touch current bits[2:0].	000b (default)
TOUCH_TEMP	Sets the touch temperature default value to 0, 1, or 2.	00b (default)
UNCUKEXTMSG	Sets unchunked extend message bit.	1b (default)
OTP_SUFFIX_CODE	OTP suffix code.	0x0001

PACKAGE INFORMATION

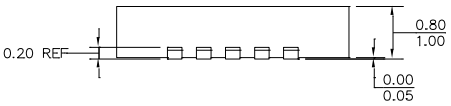
QFN-20 (4mmx4mm)



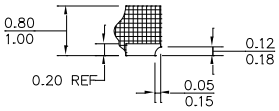
TOP VIEW



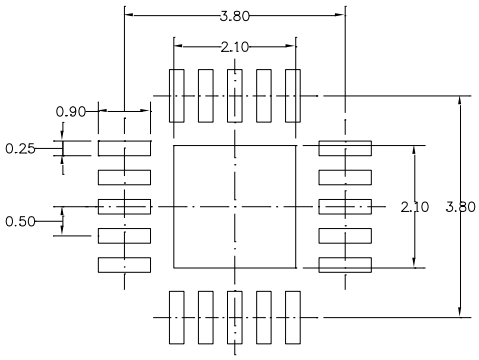
BOTTOM VIEW



SIDE VIEW



SECTION A-A

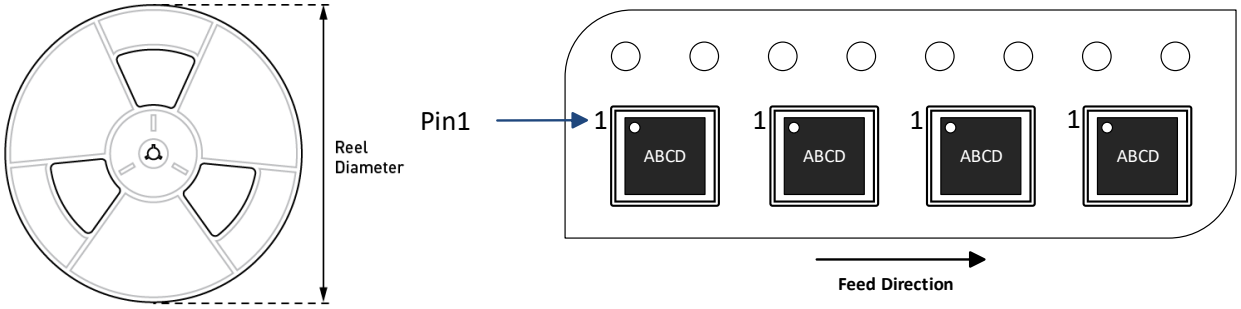


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ5031GRE-xxxx-AEC1–Z	QFN-20 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/15/2020	Initial Release	-