MPQ6612A/MPQ6612A-D

40V, 5A, H-Bridge DC Motor Driver with Current Sense, AEC-Q100

DESCRIPTION

The MPQ6612A and MPQ6612A-D are H-bridge motor drivers used for driving reversible motors, which can drive one DC motor, one winding of a stepper motor, or other loads. The H-bridge consists of four N-channel power MOSFET, and an internal charge pump that generates the required gate-drive voltages.

For the MPQ6612A, control of the outputs is accomplished through the IN1 and IN2 pins. For the MPQ6612A-D, control of the outputs is accomplished through the DIR and ENBL pins. Otherwise, both parts are identical. References to the MPQ6612A in this document also apply to the MPQ6612A-D unless otherwise noted.

The MPQ6612A operates on a motor power-supply voltage from 4V to 40V, which can supply an output current (I_{OUT}) of up to 5A according to the logic control. Very low standby quiescent current (I_Q) can be achieved when the device is disabled.

An internal current-sense (CS) circuit provides a voltage proportional to the output current (I_{OUT}). In addition, it integrates cycle-by-cycle current regulation and limiting. These features do not require the use of a low-ohmic shunt resistor.

There are internal shutdown functions for over-current protection (OCP), over-voltage protection (OVP), under-voltage lockout (UVLO) and over-temperature protection (OTP).

The MPQ6612A and MPQ6612A-D require a minimal number of readily available, standard external components. Both are available in a QFN-18 (3mmx4mm) package, and are AEC-Q100 qualified.

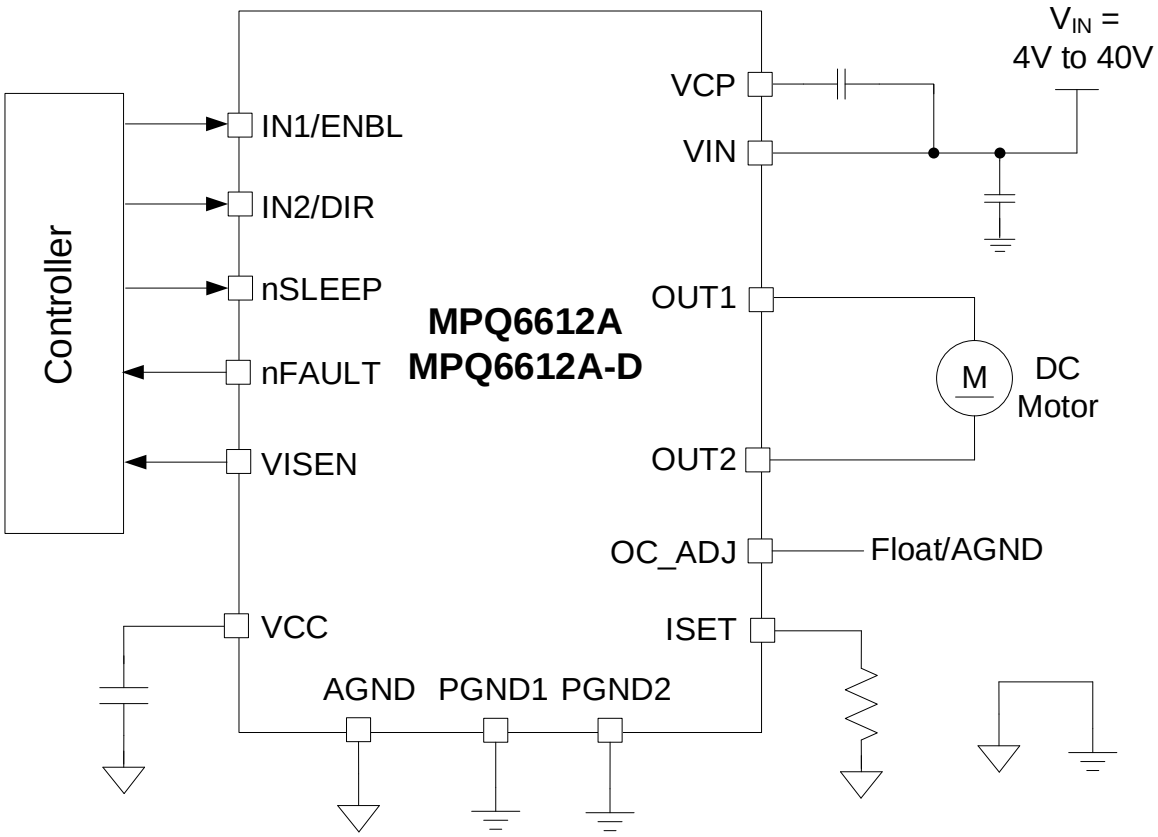
FEATURES

- Wide 4V to 40V Operating Input Voltage (V_{IN}) Range
- Internal Full H-Bridge Driver Supports Up to 100% Duty Cycle with Internal Charge Pump
- Current Sense with 10% Accuracy
- 5A Continuous Driver Current
- Low On Resistance ($R_{DS(ON)}$):
  - 63mΩ High-Side MOSFET (HS-FET)
  - 40mΩ Low-Side MOSFET (LS-FET)
- Cycle-by-Cycle Current Regulation and Limiting
- MPQ6612A: IN1 and IN2 Logic Inputs
- MPQ6612A-D: ENBL and DIR Logic Inputs
- Low Quiescent Current (I_Q) Brake Mode when Two LS-FETs Are On
- Configurable Current Limit
- Fault Indication for Over-Current Protection (OCP), Over-Voltage Protection (OVP), and Over-Temperature Protection (OTP)
- Available in a QFN-18 (3mmx4mm) Package with Wettable Flanks
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Brushed DC Motor Drivers
- Solenoid Drivers
- Door Locks and Latches

TYPICAL APPLICATION



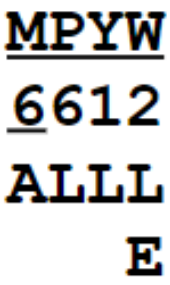
ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MPQ6612AGLE-AEC1*	QFN-18 (3mmx4mm)	*See Below*	1
MPQ6612AGLE-D-AEC1**			

* For Tape & Reel, add suffix -Z (e.g. MPQ6612AGLE-AEC1-Z).

** For Tape & Reel, add suffix -Z (e.g. MPQ6612AGLE-D-AEC1-Z).

TOP MARKING (MPQ6612AGLE-AEC1)

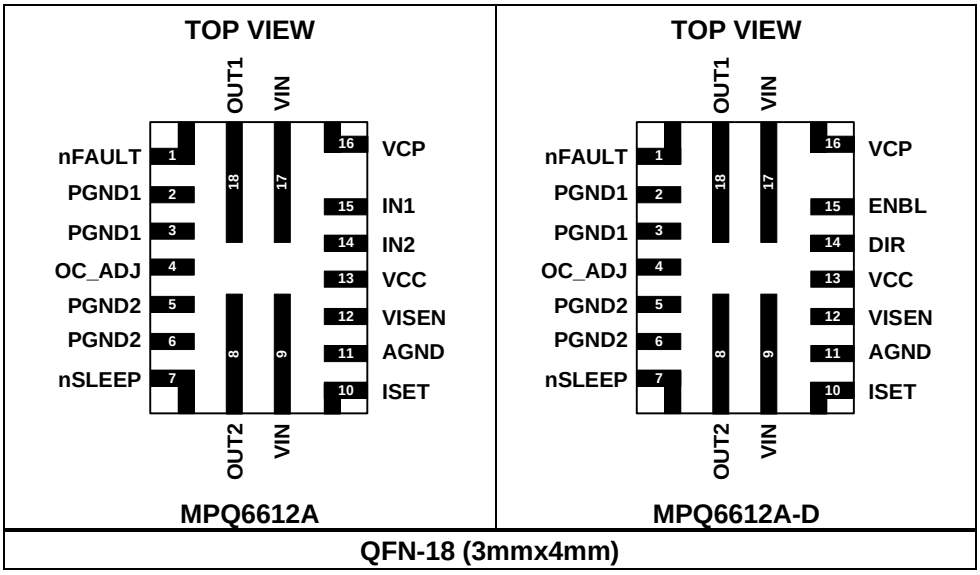


MP: MPS prefix
Y: Year code
W: Week code
6612A: Part number
LLL: Lot number
E: Wettable flank

TOP MARKING (MPQ6612AGLE-D-AEC1)

MP: MPS prefix
Y: Year code
W: Week code
6612A: Part number
LLL: Lot number
D: Part number suffix
E: Wettable flank

PACKAGE REFERENCE



QFN-18 (3mmx4mm)

PIN FUNCTIONS

Pin #	MPQ6612A	MPQ6612A-D	Description
1	nFAULT		**Fault indication.** Open-drain output. This pin is pulled logic low if a fault occurs.
2, 3	PGND1		**Power ground for half-bridge 1.** Connect PGND1 to PGND2.
4	OC_ADJ		**Over-current (OC) threshold programming pin.** Float this pin or connect to AGND.
5, 6	PGND2		**Power ground for half-bridge 2.** Connect PGND2 to PGND1.
7	nSLEEP		**Sleep mode input.** Pull this pin logic high to enable the device; pull it logic low to put the device in low-power sleep mode. nSLEEP is pulled down via an internal resistor.
8	OUT2		**Output terminal for half-bridge 2.** Connect OUT2 to the motor winding.
9, 17	VIN		**Supply voltage.** Place an input capacitor from VIN to ground to prevent large voltage spikes from appearing at the input.
10	ISET		**Current configuration resistor.** Connect a resistor to AGND to set the current limit and the VISEN output voltage. If current limiting is not desired, connect the ISET pin directly to AGND.
11	AGND		**Analog ground.** Connect the AGND pin to PGND1 and PGND2.
12	VISEN		**Current-sense output terminal.**
13	VCC		**5V LDO output for internal driver and logic.**
14	IN2	-	**Input 2.** IN2 is pulled down via an internal resistor.
	-	DIR	**H-bridge phase input (motor direction).** DIR is pulled down via an internal resistor.
15	IN1	-	**Input 1.** IN1 is pulled down via an internal resistor.
	-	ENBL	**H-bridge enable input.** ENBL is pulled down via an internal resistor.
16	VCP		**Charge pump output.** Connect a 1µF, 16V, X7R ceramic capacitor from VCP to VIN.
18	OUT1		**Output terminal for half-bridge 1.** Connect OUT1 to the motor winding.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to +45V
VCP voltage (V_{CP}).....V_{IN} to V_{IN} + 6.5V
V_{OUTx} .....-0.3V to V_{IN} + 0.3V
PGND1, PGND2 to AGND.....-0.3V to +0.3V
All other pins to AGND.....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
..... 2.6W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) 2kV
Charged-device model (CDM)..... 1.5kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....4V to 40V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Metrics (4)

θ_{JA} (junction-to-ambient)……..44.3°C/W
θ_{JC_TOP} (junction-to-case top)……..…..37.5°C/W
θ_{JC_BOTTOM} (junction-to-case bottom)…..2.6°C/W
θ_{JB} (junction-to-board)……5.3°C/W
Ψ_{JT} (junction-to-top)……....1.1°C/W
Ψ_{JB} (junction-to-board)…….....5.1°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) According to JEDEC JESD51-2/-5/-7/-8/-14.

ELECTRICAL CHARACTERISTICS

4V < V_{IN} < 40V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage						
VIN pin operating range	V_{IN}		4		40	V
Turn-on threshold	V_{IN_ON}	V_{IN} rising edge		3	3.5	V
Turn-on hysteretic voltage	V_{IN_HY}			0.3		V
IC Supply						
Shutdown current	I_{IN_SD}	nSLEEP = low			2.8	µA
Quiescent current	I_Q	Low-I_Q brake mode, OC_ADJ = floating		30	145	µA
		Low-I_Q brake mode, OC_ADJ = GND		48	185	µA
VCC regulator voltage	V_{VCC}	V_{IN} > 5.2V, 10mA load	4.8	5	5.2	V
VCC regulator dropout voltage	V_{VCCD}	V_{IN} ≤ 5.2V, 10mA load		200		mV
Input Logic (IN1, IN2, nSLEEP)						
Input high voltage	V_{IN_H}		1.5			V
Input low voltage	V_{IN_L}				0.4	V
Input high current	I_{IN_H}	V_{IN} = 5V			50	µA
Input low current	I_{IN_L}	V_{IN} = 0V	-5		+5	µA
Input pull-down resistance	$R_{PD(IN1, IN2)}$			200		kΩ
	$R_{PD(nSLEEP)}$			500		kΩ
nFault Output (Open-Drain Output)						
Output low voltage	V_{OUT_L}	I_{OUT} = 5mA			0.6	V
Output high leakage current	I_{OUT_H}	V_{OUT} = 3.3V			1	µA
Switching Frequency						
Externally applied PWM frequency	f_{PWM}				200	kHz
Power MOSFET						
Output on resistance	$R_{DS(ON)\_HS}$	I_{OUT} = 1A, T_A = 25°C	50	63	75	mΩ
		I_{OUT} = 1A, T_J = -40°C to +125°C			130	mΩ
	$R_{DS(ON)\_LS}$	I_{OUT} = 1A, T_A = 25°C	30	40	50	mΩ
		I_{OUT} = 1A, T_J = -40 to +125°C			80	mΩ
Minimum on time	t_{MON}			200		ns
Output enable time	t1				250	ns
Output disable time	t2				250	ns
Delay time	t3				420	ns
	t4				420	ns
Output rise time	t_{RISE}	R_L = 40Ω		40	120	ns
Output fall time	t_{FALL}	R_L = 40Ω		10	165	ns
IC start-up delay	t_{DELAY}	Enable to switching			500	µs

ELECTRICAL CHARACTERISTICS *(continued)*

4V < V_{IN} < 40V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Protection Features						
Over-current protection (OCP) threshold	I_{OC}	OC_ADJ = floating	9	13	19	A
		OC_ADJ = GND	13	19	25	A
Input over-voltage (OV) threshold	V_{INOVP}		43	46	48	V
Thermal shutdown	T_{SD}			165		°C
Thermal shutdown hysteresis	T_{SD_HY}			20		°C
Current Control						
Off time	t_{ITRIP}	After $V_{ITRIP-R}$ is reached		11		µs
ISET current	I_{ISET}		95	100	105	µA/A
Current trip voltage (rising)	$V_{ITRIP-R}$	At the ISET pin	1.44	1.5	1.56	V
Current trip voltage (falling)	$V_{ITRIP-F}$	At the ISET pin	1.15	1.2	1.25	V
VISEN Output						
VISEN output voltage (V_{VISEN}) accuracy	ΔV_{VISEN}	V_{ISET} > 0.4V	-5		+5	%

TIMING DIAGRAM

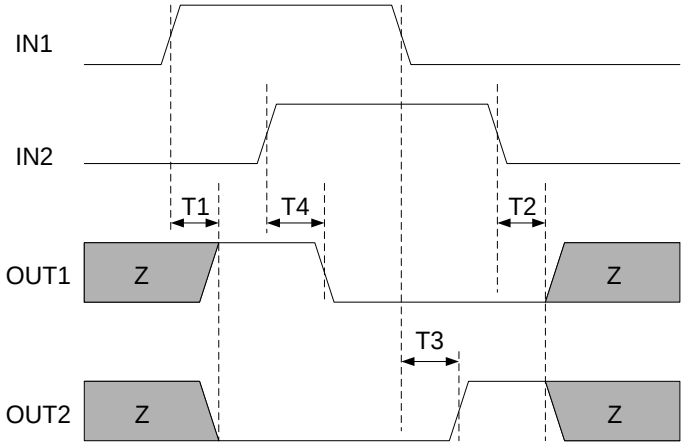
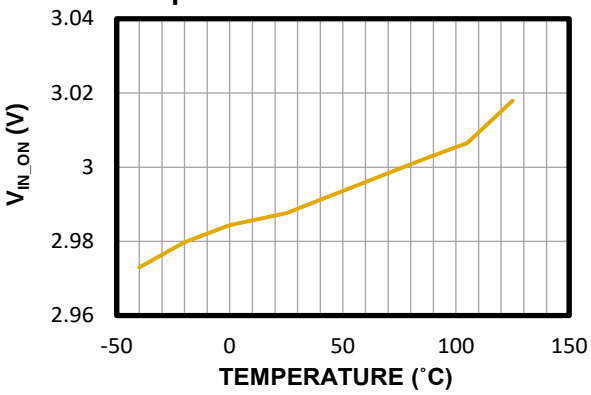


Figure 1: Input/Output Timing

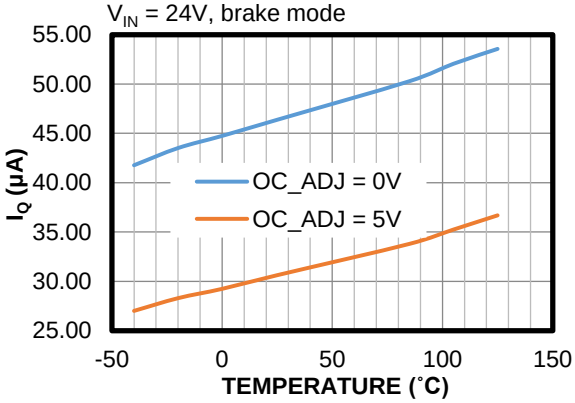
TYPICAL CHARACTERISTICS

Turn-On Threshold vs. Temperature



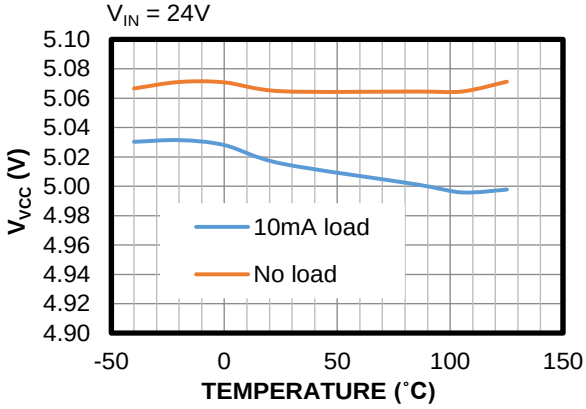
Quiescent Current vs. Temperature

V_{IN} = 24V, brake mode



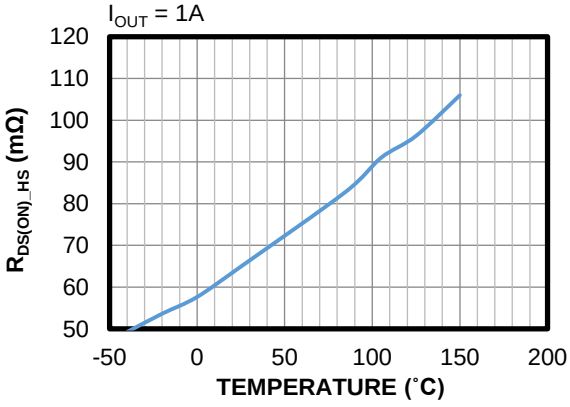
VCC Voltage vs. Temperature

V_{IN} = 24V



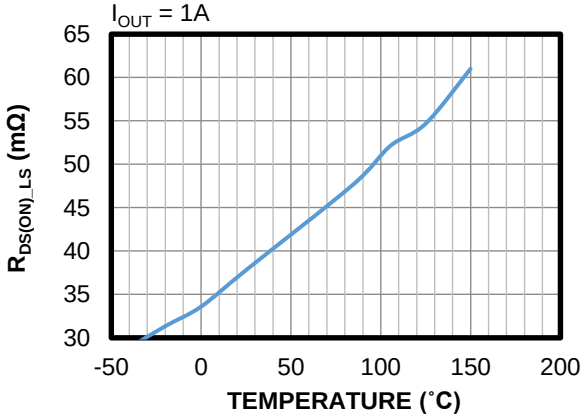
HS-FET On Resistance vs. Temperature

I_{OUT} = 1A

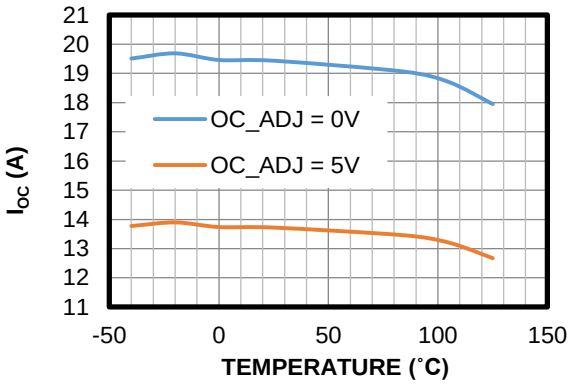


LS-FET On Resistance vs. Temperature

I_{OUT} = 1A



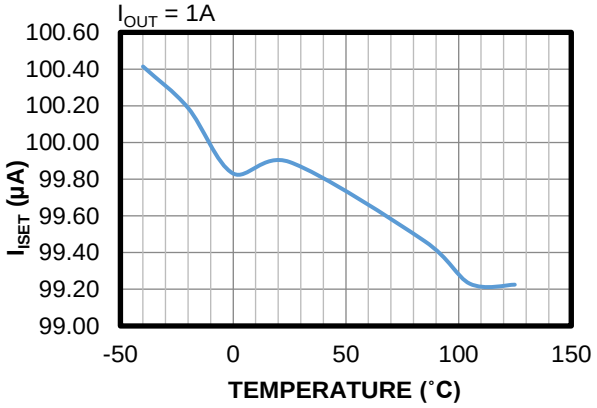
OCP Threshold vs. Temperature



TYPICAL CHARACTERISTICS *(continued)*

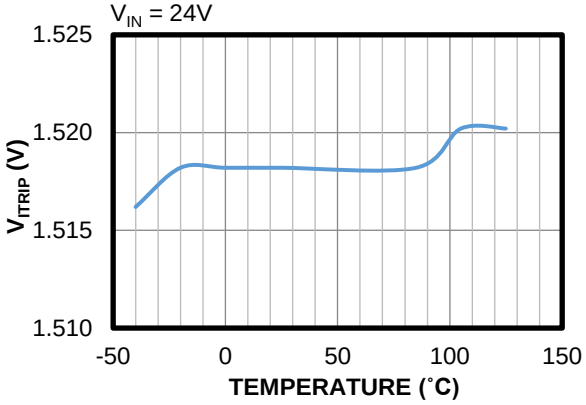
ISET Current vs. Temperature

I_{OUT} = 1A



Current Trip Voltage vs. Temperature

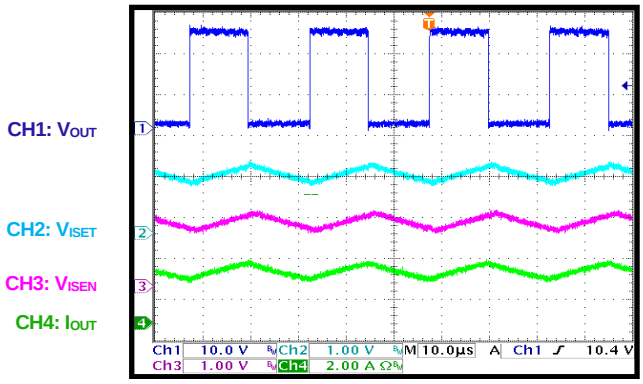
V_{IN} = 24V



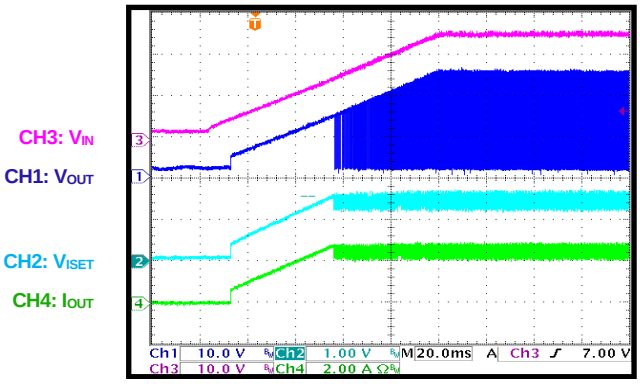
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, IN1 = 5V, IN2 = 0V, I_{OUT} = 3A, T_A = 25°C, resistor + inductor load: 4Ω + 0.2mH between OUT1 and OUT2, unless otherwise noted.

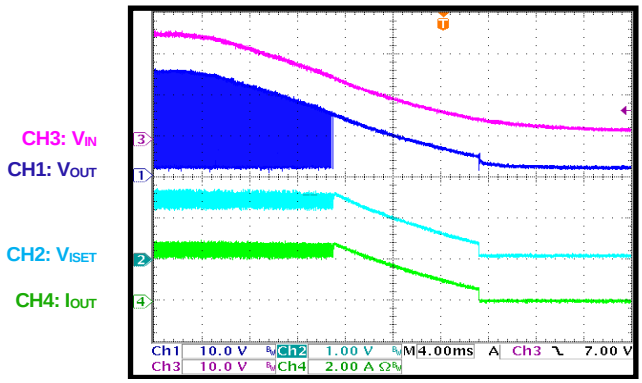
Steady State



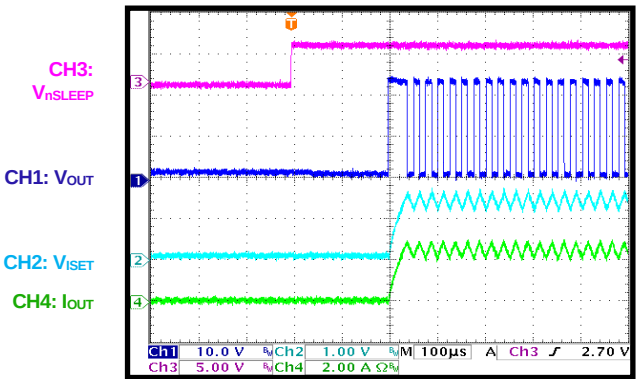
Input Power Start-Up



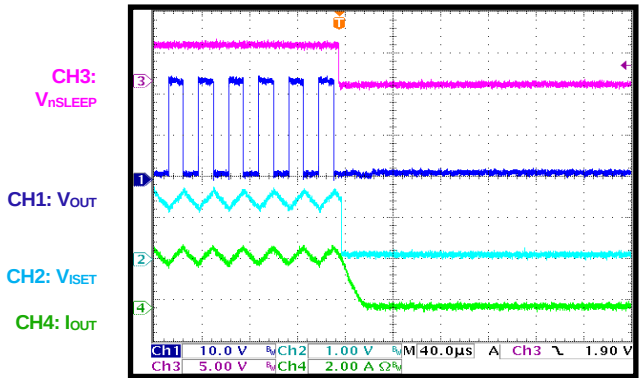
Input Power Shutdown



Sleep Start-Up



Sleep Shutdown



FUNCTIONAL BLOCK DIAGRAM

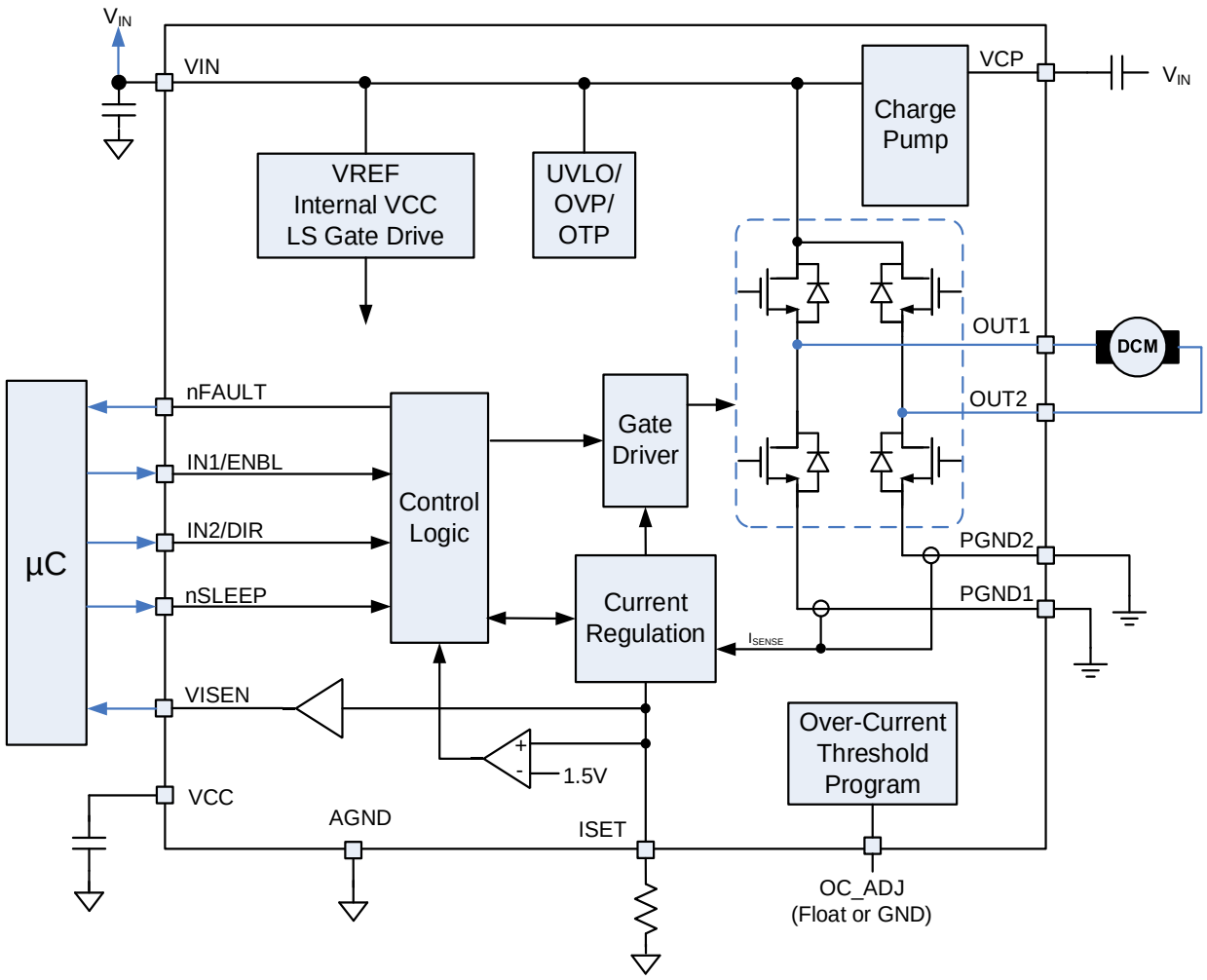


Figure 2: Functional Block Diagram (1 Amp Channel)

OPERATION

Bridge Control

The MPQ6612A is controlled using a pulse-width modulation (PWM) input interface that is compatible with industry-standard devices.

For the MPQ6612A, control of the outputs is accomplished through the IN1 and IN2 pins. Drive both IN1 and IN2 high for about 1ms to put the part into low quiescent current (I_Q) brake mode. In this mode, only a few internal circuits continue operating to maintain the load brake. Current sense, current limiting and regulation functionality, and most diagnostic and protection functions are disabled. Only output short to input voltage (V_{IN}) protection is remains enabled, so the part consumes a very small current. Table 1 shows the logic for the MPQ6612A.

Table 1: MPQ6612A Input Logic Truth Table

IN1	IN2	OUT1	OUT2	Function (DC Motor)
L	L	Z	Z	Coast
L	H	L	H	Reverse
H	L	H	L	Forward
H	H	L	L	Brake

For the MPQ6612A-D, control of the outputs is accomplished through the DIR and ENBL pins. Drive ENBL low for about 1ms to put the part into low-I_Q brake mode. Table 2 shows the logic for the MPQ6612A-D.

Table 2: MPQ6612A-D Input Logic Truth Table

ENBL	DIR	OUT1	OUT2	Function (DC Motor)
H	L	L	H	Reverse
H	H	H	L	Forward
L	X	L	L	Brake

Current Sensing (CS)

The current flowing into the two low-side MOSFETs (LS-FETs) is sensed with an internal current-sense (CS) circuit. A voltage proportional to the output current (I_{OUT}) is sourced on the VISEN pin.

VISEN output voltage (V_{VISEN}) scaling is set via a resistor connected between the ISET pin and ground. For a 1A I_{OUT}, 100μA of current is sourced into the resistor connected to ISET. For example, if a 5kΩ resistor is connected between ISET and ground, V_{VISEN} is 0.5V/A of I_{OUT}.

Current is sensed any time one of the low-side MOSFETs are turned on, including during slow decay (brake) mode.

The load current ($I_{VISEN-LOAD}$) applied to the VISEN pin should be kept below 2mA, with no more than 500pF of capacitance.

Current Limiting and Regulation

The current in the outputs is regulated using constant-off-time PWM control circuitry. This operates as follows:

1. Initially, a diagonal pair of MOSFETs turns on and drives current through the load.
2. The current increases in the load, which is sensed by the internal CS circuit.
3. If I_{OUT} reaches the current trip voltage threshold ($V_{ITRIP-R}$), the H-bridge switches to slow decay mode, with the two LS-FETs turned on.
4. If I_{OUT} drops to below 80% of $V_{ITRIP-R}$ after a fixed off time (t_{ITRIP}), then the diagonal pair of MOSFETs are re-enabled and the cycle repeats.

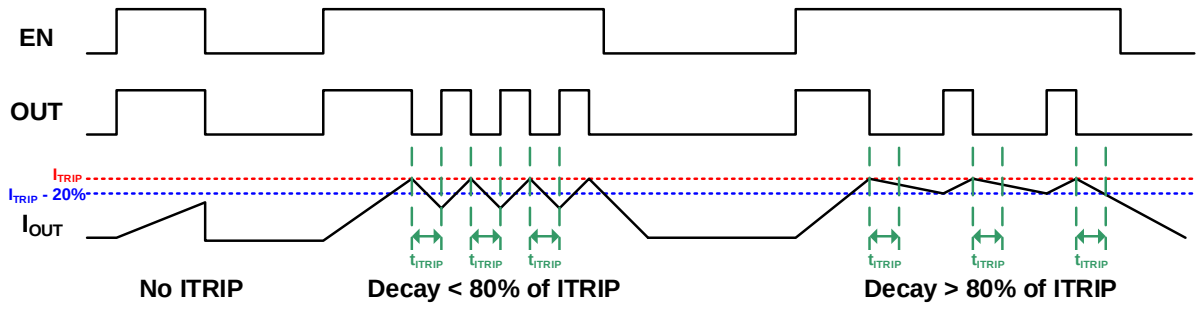


Figure 3: Current Limit Operation

5. If the current remains above 80%, the off time is extended until the current drops to 80% of $V_{ITRIP-R}$.

$V_{ITRIP-R}$ is reached when the ISET pin reaches 1.5V. For example, with a 5kΩ resistor from ISET to ground, the ISET voltage (V_{ISET}) is 0.5V/A of I_{OUT}. When I_{OUT} reaches 3A, the ISET pin voltage reaches 1.5V, and a current trip occurs.

For DC motors, current regulation is used to limit the motor's start-up and stall current. Speed control is typically performed by providing an external PWM signal to the input pins.

If current regulation is not needed, it can be disabled by connecting the ISET pin directly to ground.

During current regulation, the nFAULT pin is not active.

Blanking Time

There is often a current spike when the MOSFET turns on due to the body diode's reverse-recovery current or the load's shunt capacitance. This current spike requires filtering to prevent the MOSFET from erroneously shutting down. An internal fixed blanking time (t_{MON}) blanks the CS comparator's output when the MOSFET turns on. This blanking time also sets the MOSFET's minimum on time.

nSLEEP Operation

Driving nSLEEP low puts the device into a low-power sleep state. In this state, the H-bridge outputs are turned off, all related internal circuits — including the gate drive charge pump — are disabled, and all inputs are ignored. When waking up from sleep mode, there is a set delay time (t_{DELAY}) before the outputs begin operating.

Protection Circuits

The MPQ6612A is offers protection against under-voltage (UV), over-current (OC), over-voltage (OV), and over-temperature (OT) conditions.

Over-Current Protection (OCP)

The MPQ6612A includes internal short-circuit protection (SCP). The currents in both the high-side MOSFETs (HS-FETs) and LS-FETs are measured. If the current exceeds the OC threshold (I_{OC}), then all MOSFETs in the H-bridge turn off. After approximately 4ms, the bridge is re-enabled automatically.

I_{OCP} is specified by OC_ADJ (see Table 3).

Table 3: OCP Threshold

OC_ADJ	Min OCP Threshold (A)
Float	9
GND	13

Over-Temperature Protection (OTP)

The MPQ6612A also integrates thermal monitoring. If the die temperature exceeds safe limits (T_{SD}), all MOSFETs turn off and the nFAULT pin is pulled low. Once the die temperature returns to a safe level (T_{SD} - T_{SD_HY}), the device automatically resumes normal operation.

Under-Voltage Lockout (UVLO)

If at any time the voltage on the VIN pin falls below the under-voltage lockout (UVLO) threshold voltage, all circuitry in the device is disabled and the internal logic is reset. Once V_{IN} exceeds the UVLO threshold, the device restarts and resumes normal operation.

Over-Voltage Protection (OVP)

If the voltage on the VIN pin exceeds the input over-voltage threshold (V_{INOVP}), the device is disabled. Once V_{IN} drops to a safe level (about 2V below V_{INOVP}), the device restarts and resumes normal operation.

Fault Indication Output (nFAULT)

If any protection circuits are activated, the nFAULT pin is pulled active low. These fault conditions include OC, OT, and OV. nFAULT is an open-drain output, and requires an external pull-up resistor. Once any fault conditions removed and the device resumes normal operation, nFAULT is pulled inactive high by the pull-up resistor.

APPLICATION INFORMATION

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 4 and follow the guidelines below:

1. Place the supply bypass capacitor and charge pump capacitor as close to the IC as possible. Each VIN pin should have a bypass capacitor.
2. Use large copper areas for PGND, VIN, and OUT to improve thermal performance.
3. Use thermal vias to transfer heat to other layers of the PCB. Use as many vias as possible to improve thermal dissipation.

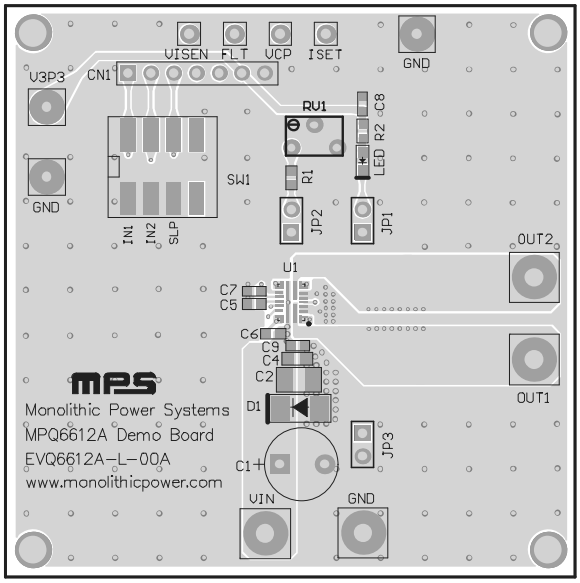


Figure 4: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

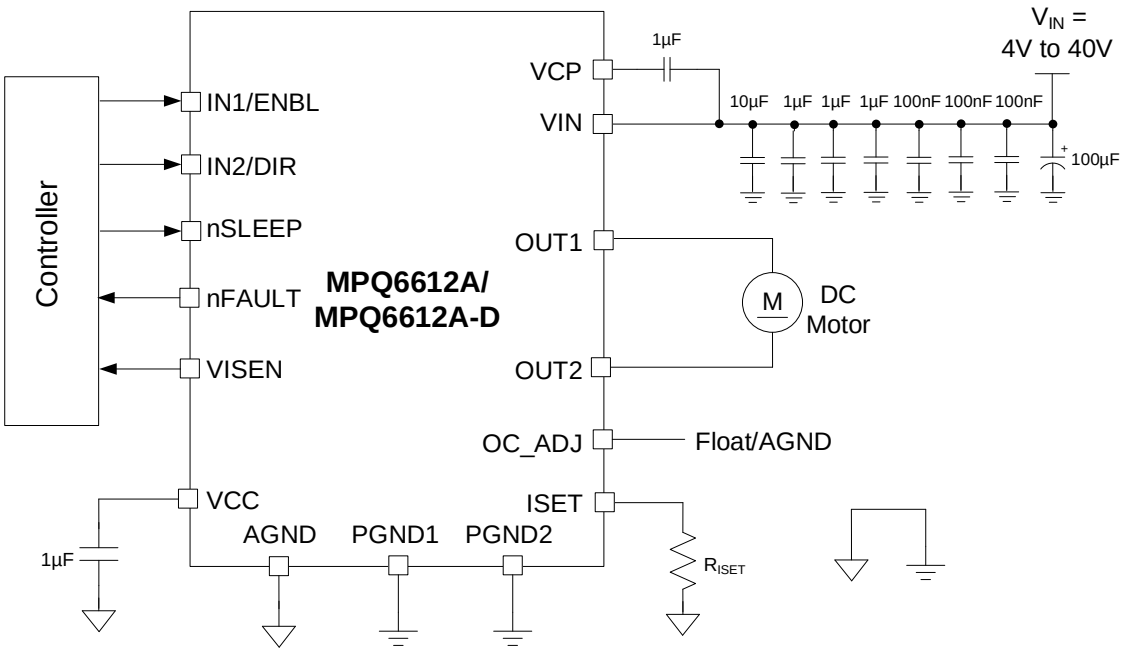
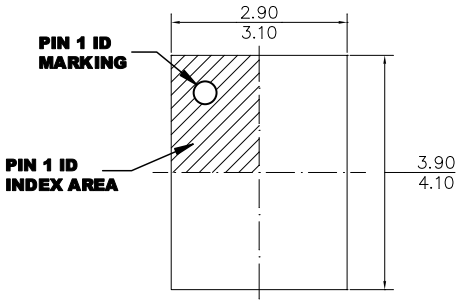


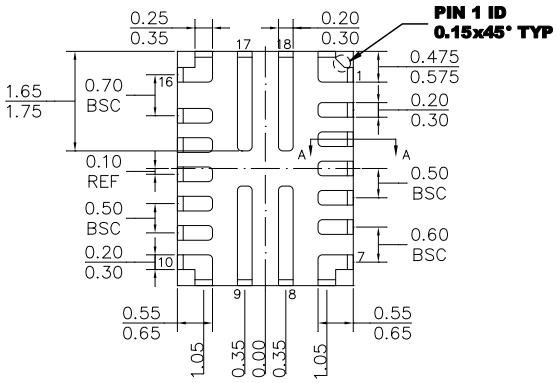
Figure 5: Typical Application Circuit

PACKAGE INFORMATION

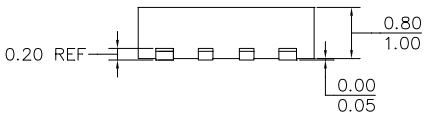
QFN-18 (3mmx4mm)
Wettable Flank



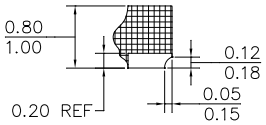
TOP VIEW



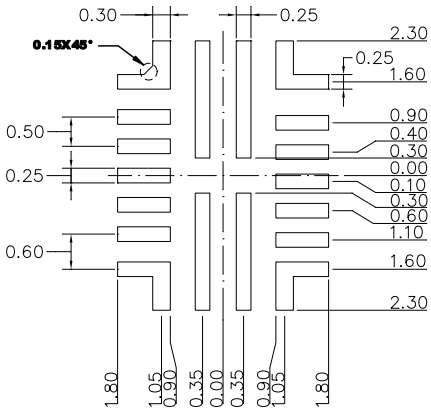
BOTTOM VIEW



SIDE VIEW



SECTION A-A

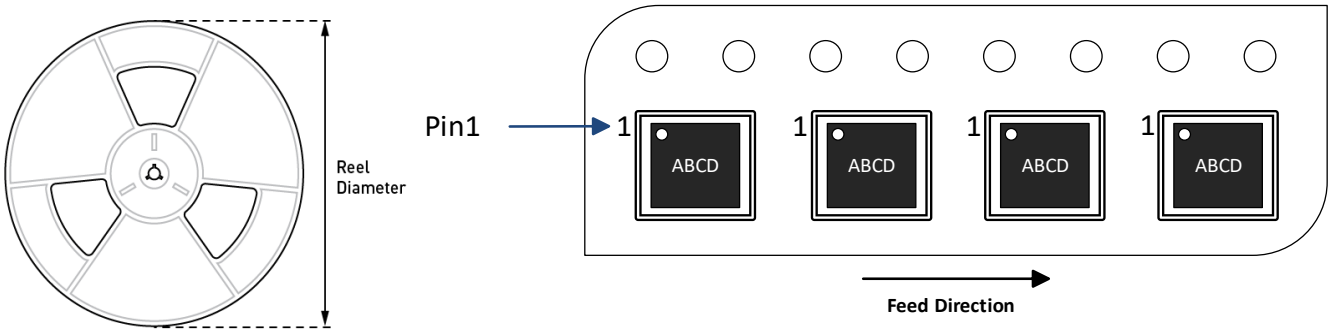


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tray	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ6612AGLE-AEC1-Z	QFN-18 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ6612AGLE-D-AEC1-Z							

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/26/2024	Initial Release	-