MPQ6619

2.7V to 28V, 5A,
H-Bridge Motor Driver
AEC-Q100 Qualified

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MPQ6619 is an H-bridge motor driver that operates from a supply voltage up to 28V and delivers a motor current up to 5A. The MPQ6619 is ideally suited to drive a brushed DC motor.

The MPQ6619 also has programmable current limit function.

Full protection features include over-current protection (OCP), input over-voltage protection (OVP), under-voltage lockout (UVLO), and over-temperature protection (OTP).

The MPQ6619 is available in a QFN-19 (4mmx4mm) package.

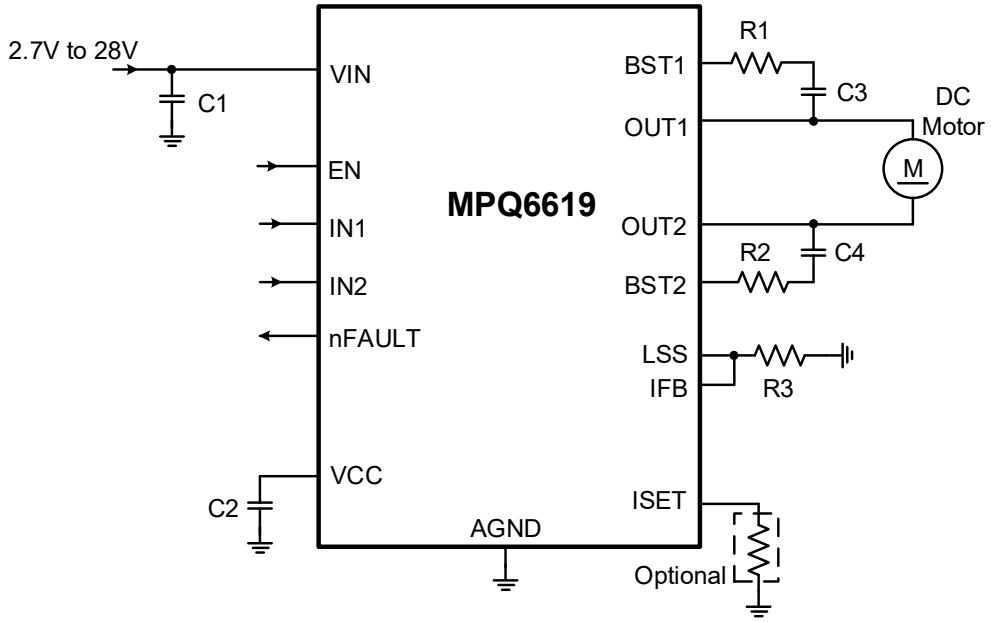
FEATURES

- Wide 2.7V to 28V Operating Input Range
- Up to 5A Peak Output Current
- Internal H-Bridge Driver
- Programmable Current Limiting
- 65mΩ $R_{DS(ON)}$ for Each Half-Bridge MOSFET
- 100% Duty Cycle Operation of H-Bridge
- 1μA Shutdown Mode
- Over-Current Protection (OCP)
- Input Over-Voltage Protection (OVP)
- Under-Voltage Lockout (UVLO)
- Over-Temperature Protection (OTP)
- Fault Indication Output
- Available in a QFN-19 (4mmx4mm) Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- DC Motors
- Solenoid/Actuators

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ6619GRE-AEC1	QFN-19 (4mmx4mm)	*See Below*	1

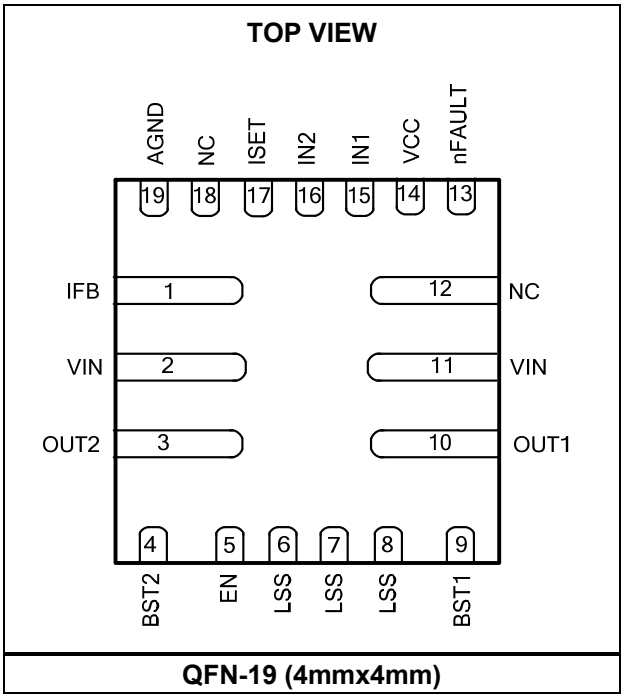
* For Tape & Reel, add suffix -Z (e.g. MPQ6619GRE-AEC1-Z).

TOP MARKING

MPSYWW
MP6619
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
MP6619: Part number
LLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-19 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	IFB	**Current-sense signal feedback.** Connect the IFB and LSS pins together.
2, 11	VIN	**Input supply.**
3	OUT2	**Output terminal 2.**
4	BST2	**Bootstrap (BST) pin for the OUT2 high-side MOSFET (HS-FET) gate driver.** Connect a capacitor between the BST2 and OUT2 pins.
5	EN	**IC enable.**Pull the EN pin down internally.
6, 7, 8	LSS	**Low-side (LS) source connection.** For current sense, connect a current-sense resistor between the LSS pin and power ground.
9	BST1	**BST pin for the OUT1 HS-FET gate driver.** Connect a capacitor between BST1 and OUT1.
10	OUT1	**Output terminal 1.**
12, 18	NC	**No connection.** Float this pin or connect it to AGND.
13	nFAULT	**Fault indication output.** Pull the nFAULT active low for fault conditions.
14	VCC	**5V LDO output for internal driver and logic.**
15	IN1	**Output 1 control input.** Pull the IN1 pin down internally.
16	IN2	**Output 2 control input.** Pull the IN2 pin down internally.
17	ISET	**Current trip voltage setting.** Connect a resistor from the ISET pin to GND.
19	AGND	**Ground for internal logic.**

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 35V
V_{OUTx} ..... -0.3V to V_{IN} + 0.3V
V_{BST1} ..... V_{OUT1} + 6V
V_{BST2} ..... V_{OUT2} + 6V
LSS ..... -0.3V to +0.3V
All other pins ..... -0.3V to +6V
Continuous power dissipation (T_A = 25°C) (2)
QFN-19 (4mmx4mm) 2.8W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged device model (CDM) ..... ±1.25kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 2.7V to 28V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4)	θ_{JA}	θ_{JC}
QFN-19 (4mmx4mm)	44	9 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which can cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operation conditions.
4) Measured on a JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 13.5V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage						
VIN operating range	V_{IN}		2.7		28	V
Turn-on threshold	V_{IN_ON}	VIN rising edge		2.5	2.65	V
Turn-on hysteretic voltage	V_{IN_HY}			0.15		V
IC Supply						
Shutdown current	I_{IN_SD}	EN = 0			1	µA
Quiescent current	I_{IN_SBY}	EN = 1, no load current		1.6	2.2	mA
VCC regulator voltage	V_{VCC}	V_{IN} > 5.2V	4.5	5	5.5	V
VCC regulator drop output voltage		V_{IN} < 5V, 20mA load		100		mV
Logic						
Logic high threshold	V_{IH}				1.5	V
Logic low threshold	V_{IL}		0.4			V
IC start-up delay	t_{DELAY}	EN active to switching		230	350	µs
Current Control						
Current trip voltage	V_{ITRIP}	V_{ITRIP} = 200mV	180	200	225	mV
		V_{ITRIP} = 100mV	85	100	120	mV
Off time	t_{ITRIP}	After I_{TRIP}		1		ms
Switching Frequency						
PWM frequency on IN1/IN2	f_{PWM}				200	kHz
Power MOSFET						
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	T_A = 25°C	42	65	93	mΩ
		T_A = -40°C to +125°C			135	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	T_A = 25°C	42	65	93	mΩ
		T_A = -40°C to +125°C			140	mΩ
Minimum on time	t_{MIN_ON}			200		ns
Bootstrap for High-Side Driver						
Forward voltage for BST charge	V_{FBST}			0.5		V
BST UVLO	$V_{BST-UVLO}$	Rising edge		2		V
Protection						
Over-current (OC) retry time	t_{OCP}		0.8	1		ms
OC threshold	I_{OCP}		6.5	10		A
Input over-voltage (OV) threshold	V_{INOVP}		29	31	33	V
Thermal shutdown (5)	T_{SD}			150		°C
Thermal shutdown hysteresis(5)	T_{SD_HY}			20		°C

Note:

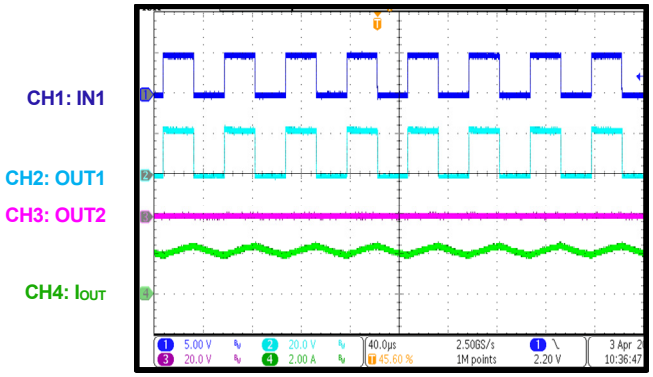
5) Not tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, T_A = 25°C, unless otherwise noted.

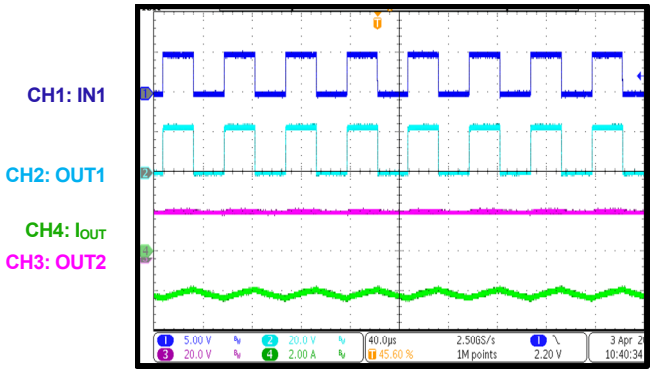
Normal Operation

V_{IN} = 24V, IN1 = 20kHz / 50%, IN2 = low, load = 5Ω + 700μH



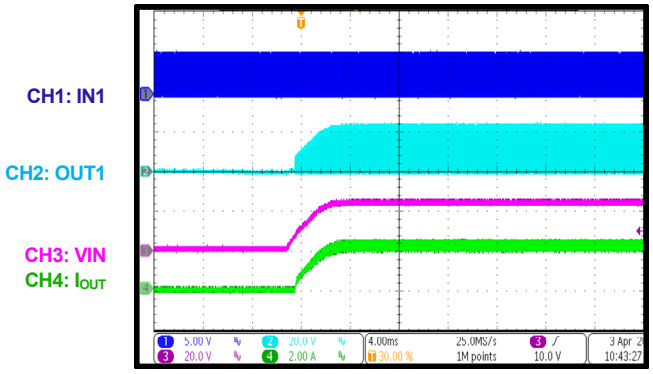
Normal Operation

V_{IN} = 24V, IN1 = 20kHz / 50%, IN2 = high, load = 5Ω + 700μH



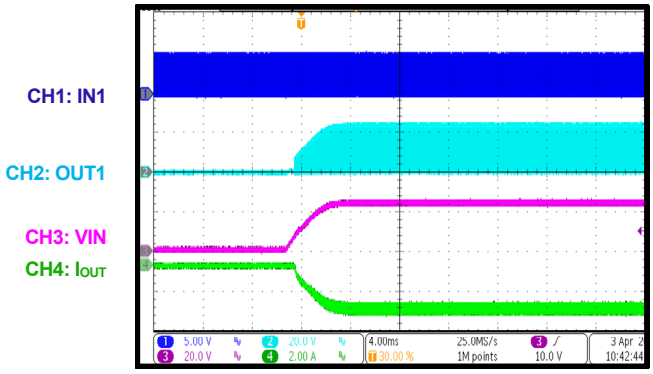
Start-Up through VIN

V_{IN} = 24V, IN1 = 20kHz / 50%, IN2 = low, load = 5Ω + 700μH



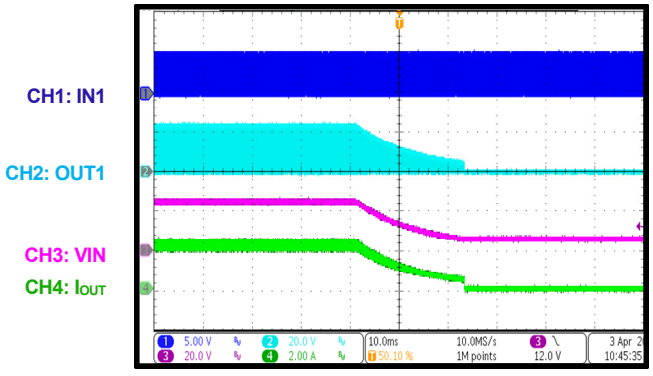
Start-Up through VIN

V_{IN} = 24V, IN1 = 20kHz / 50%, IN2 = high, load = 5Ω + 700μH



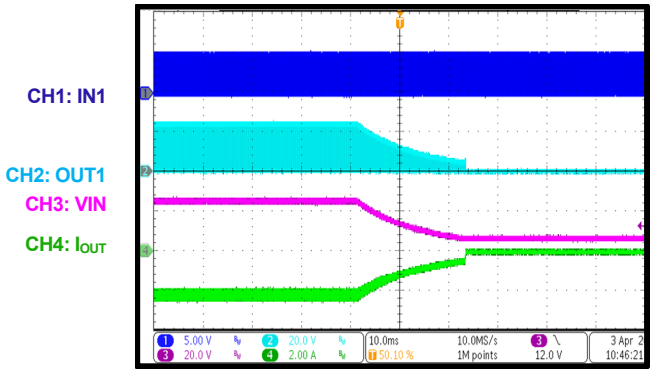
Shutdown through VIN

V_{IN} = 24V, IN1 = 20kHz / 50%, IN2 = low, load = 5Ω + 700μH



Shutdown through VIN

V_{IN} = 24V, IN1 = 20kHz / 50%, IN2 = high, load = 5Ω + 700μH

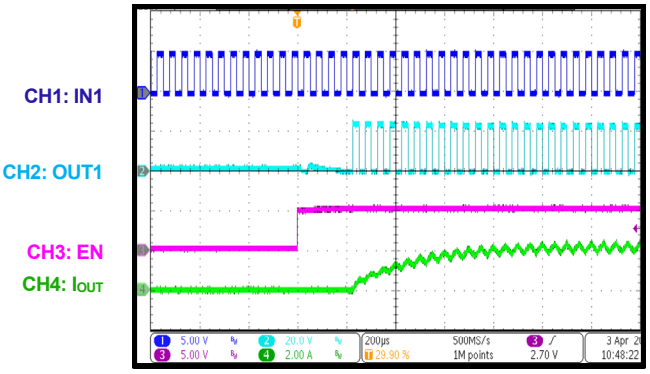


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, T_A = 25°C, unless otherwise noted.

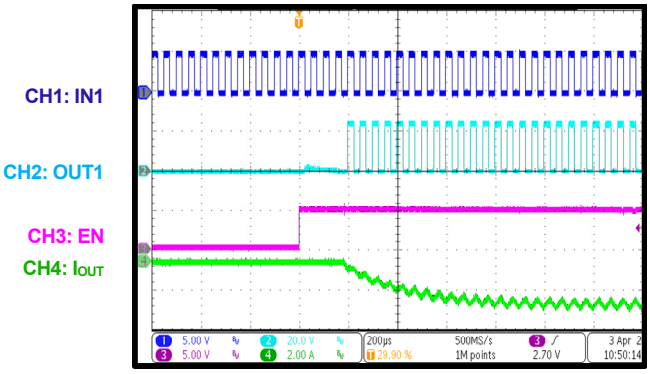
IC Enable

V_{IN} = 24V, IN1 = 20kHz / 50%, IN2 = low, load = 5Ω + 700μH



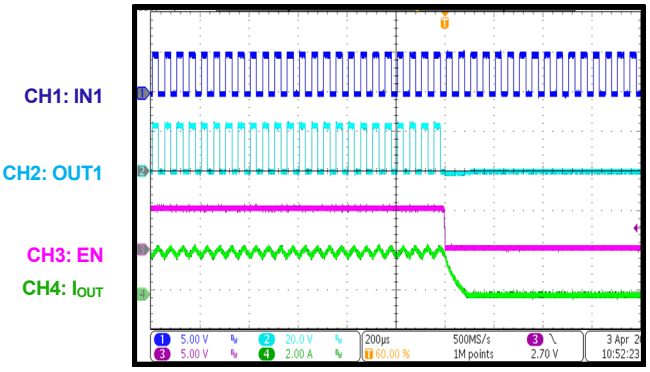
IC Enable

V_{IN} = 24V, IN1 = 20kHz / 50%, IN2 = high, load = 5Ω + 700μH



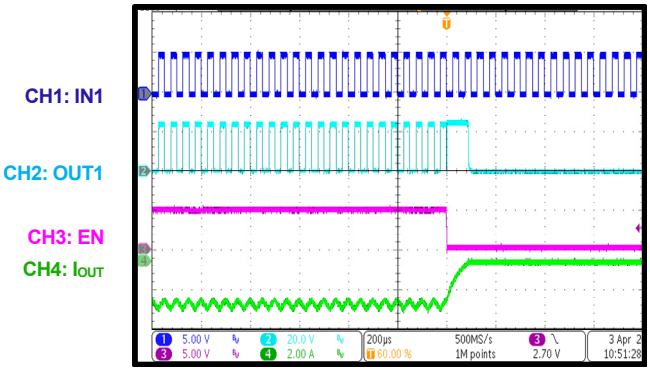
IC Disable

V_{IN} = 24V, IN1 = 20kHz / 50%, IN2 = low, load = 5Ω + 700μH



IC Disable

V_{IN} = 24V, IN1 = 20kHz/50%, IN2 = high, load = 5Ω + 700μH



FUNCTIONAL BLOCK DIAGRAM

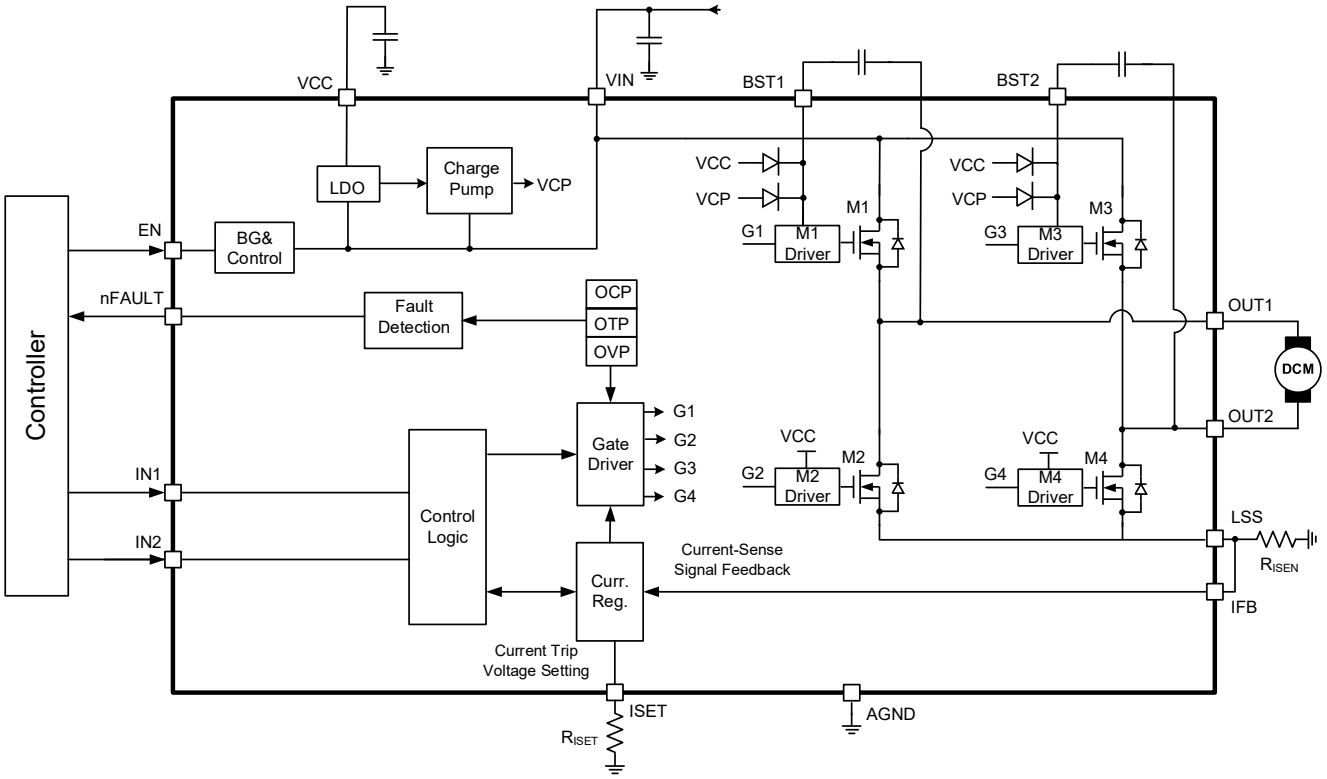


Figure 1: Functional Block Diagram

OPERATION

The MPQ6619 is an H-bridge motor driver that operates from a supply voltage up to 28V and delivers a motor current up to 5A. Typically, the MPQ6619 is used to drive a brushed DC motor.

Input Logic

For the MPQ6619, control of each half-bridge is independent, using EN, IN1, and/or IN2 pins (see Table 1).

Table 1: Truth Table

EN	INx	OUTx
0	x	Z
1	0	L
1	1	H

Shutdown Mode

If the EN signal is pulled low, the MPQ6619 shuts down. In shutdown mode, all circuits and blocks are disabled, and the MPQ6619 consumes less than 1μA of shutdown current. There is about 150ns of deglitch time on EN to avoid mistriggering.

Current Limit

The MPQ6619 has a programmable current limit function. The output current (I_{OUT}) flowing through both two low-side MOSFETs (LS-FETs) is sensed by an external sense resistor. If I_{OUT} reaches the current trip threshold, a current limit condition is triggered. The entire H-bridge switches to a high-impedance state with all the MOSFETs turned off. After a fixed off time (t_{ITRIP}), the MOSFETs are re-enabled, and the cycle repeats.

The current limit is triggered when the IFB pin voltage (V_{IFB}) reaches the current trip voltage (V_{ITRIP}). For example, if a 40mΩ sense resistor is connected from LSS to ground, and the current trip voltage (V_{ITRIP}) is 200mV, when I_{OUT} reaches 5A, V_{IFB} reaches 200mV and a current trip occurs.

Current Trip Voltage Setting

The current control trip value is set by connecting a resistor between ISET and GND. When ISET is floating, the current trip voltage is set to the default (200mV). If a resistor is connected between ISET and GND, the current trip voltage can be reduced below 200mV to reduce power loss on the sense resistor. The IC requires about 0.3ms to detect whether a resistor is available on ISET when the IC starts up for the first time. During this time, the IC is not switching. The relationship of the current trip voltage and ISET resistance (R_{ISET}) can be calculated with Equation (1):

$$V_{ITRIP} = 0.2 \times \frac{40}{R_{ISET}(k\Omega)} \quad (1)$$

For example, if R_{ISET} is 80kΩ, the trip voltage is 100mV. For improved accuracy, a 40kΩ to 80kΩ resistance is recommended to achieve a 200mV to 100mV current trip voltage.

Start-Up Sequence

The IC needs about 0.3ms to detect whether a resistor is available on ISET when the IC starts up for the first time. During this time, the IC is not switching.

VCC LDO Regulator

The IC employs a low-dropout (LDO) regulator to provide a constant voltage (5V) at VCC. The VCC voltage (V_{VCC}) is used for the internal power supply of the logic circuit and driver circuit. When the input voltage drops, V_{VCC} drops together with V_{IN}. If V_{VCC} drops below 4.8V, the IC triggers a power reset sequence and shuts down. The IC resumes normal operation when V_{VCC} exceeds 5.1V.

High-Side MOSFET (HS-FET) Driver

The two high-side MOSFETs (HS-FETs) (M1 and M3) are N-channel MOSFETs. When the HS-FETs turn on, a bootstrap (BST) supply voltage (V_{BSTx}) across BST1 and BST2 is required. V_{BSTx} is generated by a combination of the internal charge pump and a 5V VCC. This allows the IC to operate at 100% duty cycle to provide enough driver voltage for the HS-FETs.

Over-Current Protection (OCP)

The over-current protection (OCP) circuit limits the current through each MOSFET by reducing the gate driver voltage to the MOSFET. If the MOSFET current remains in the over-current (OC) condition (exceed the OCP threshold, I_{OCP}) for longer than the OCP deglitch time, all MOSFETs in the H-bridge are disabled and nFAULT is pulled low. The driver remains disabled during the OCP retry time (t_{OCP}) and then is re-enabled automatically.

Input Over-Voltage Protection (OVP)

During the freewheeling time, the energy stored in the load current is delivered to the input side. If V_{IN} and the output current (I_{OUT}) are high enough, the energy sent back to the input side causes V_{IN} to rise up. To avoid IC damage due to a high voltage spike, the IC employs V_{IN} protection.

If voltage applied to the VIN pin is above the OVP threshold, the H-bridge output is disabled and nFAULT is pulled low. This protection is released when V_{IN} drops to a safe level.

Junction Over-Temperature Protection (OTP)

If the die temperature exceeds safe limits, all H-bridge MOSFETs are disabled and nFAULT is driven low. Once the die temperature drops to a safe level, the MPQ6619 resumes normal operation automatically.

Fault Indication Output (nFAULT)

The MPQ6619 provides an nFAULT pin that is pulled active low if any of the protection circuits are activated. These fault conditions include over-current protection (OCP), over-temperature protection (OTP), and over-voltage protection (OVP). nFAULT is also pulled low when a current-limit trip occurs. nFAULT is an open-drain output, and requires an external pull-up resistor. Once the fault condition is removed, nFAULT is pulled inactive high by the pull-up resistor.

Enable/Disable (EN)

To enable the MPQ6619, apply a logic high signal to EN, and the high-level signal time must exceed about 10μs. Pull EN to logic low, and set the low-level signal above 100ns to shut down the IC.

APPLICATION INFORMATION

Selecting the Input Capacitor

The input capacitor (C_{IN}) reduces the surge current drawn from the input supply and the switching noise from the device. C_{IN} impedance at the switching frequency (f_{SW}) should be less than the input source impedance to prevent the high-frequency switching current from passing through to the input. Ceramic capacitors with X5R or X7R dielectrics are recommended for their low ESR and small temperature coefficients. A higher-value capacitor is helpful for reducing V_{IN} ripple and noise. For most applications, two 22µF ceramic capacitors in parallel are sufficient. It is recommended to connect one capacitor to each VIN pin.

Setting the Output Current limit

If a resistor is connected between ISET and GND, then the output current limit value can be calculated with Equation (2):

$$I_{OUT} = 0.2 \times \frac{40}{R_{ISET}(k\Omega)} \times \frac{1}{R_{ISEN}(\Omega)} \quad (2)$$

If ISET is left floating, then I_{OUT_LIM} can be calculated with Equation (3):

$$I_{OUT} = \frac{0.2}{R_{ISEN}(\Omega)} \quad (3)$$

For example, if R_{ISET} is 80kΩ, then the trip voltage is 100mV. For improved accuracy, a 40kΩ to 80kΩ resistance is recommended to achieve a 200mV to 100mV current trip voltage.

Setting the Sense Resistor

The power loss of the sensing resistor (P_{LOSS_RIFB}) can be calculated with Equation (4):

$$P_{LOSS\_RIFB} = \frac{V_{ITRIP}^{2}}{R_{ISEN}(\Omega)} \quad (4)$$

To guarantee a current reference, the nominated power rating of the sensing resistor is recommended to be twice the calculated power loss with at least a 1% accuracy resistor.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 2 and follow the guidelines below:

1. Place the input capacitor as close as to the VIN, VCC, and GND pins.
2. Use a wide copper plane for the input, output, and GND connection to improve thermal performance.
3. Place as many GND vias near the output and C_{IN} as possible to improve thermal performance.
4. Keep the sense resistor loop as short as possible.
5. Keep the current-sense feedback signal far away from noise sources.

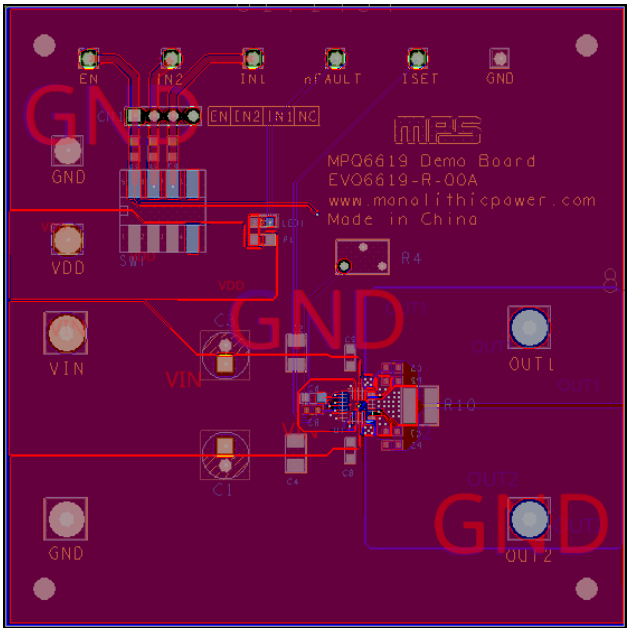


Figure 2: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

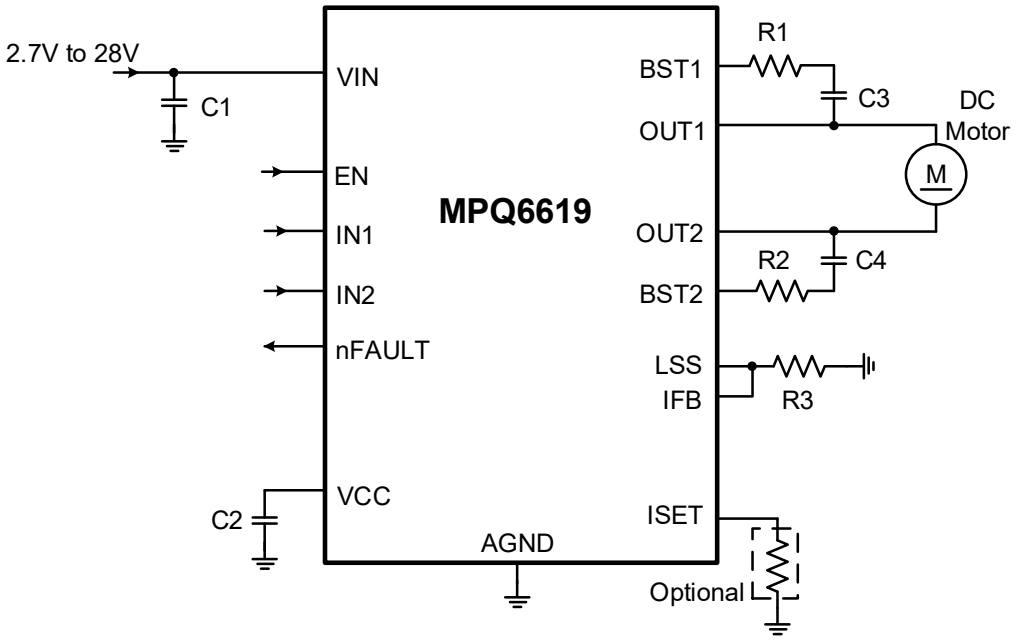
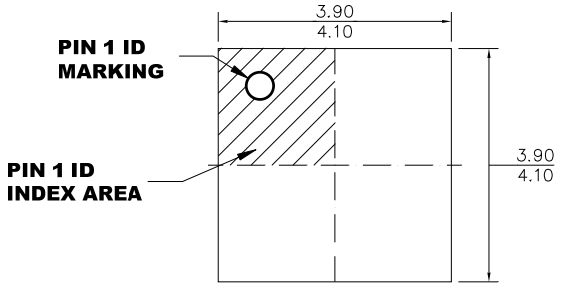


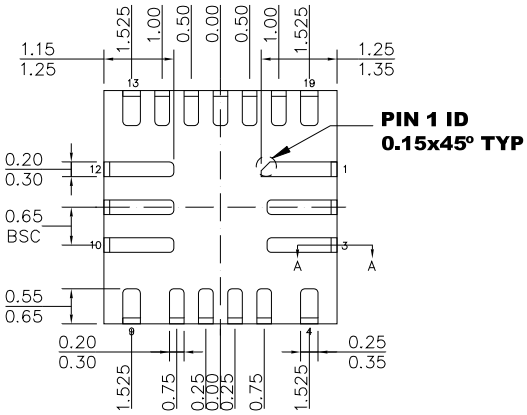
Figure 3: Typical Application Circuit

PACKAGE INFORMATION

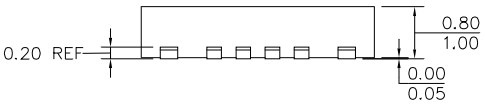
QFN-19 (4mmx4mm)



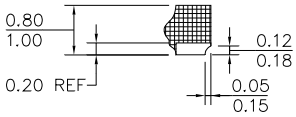
TOP VIEW



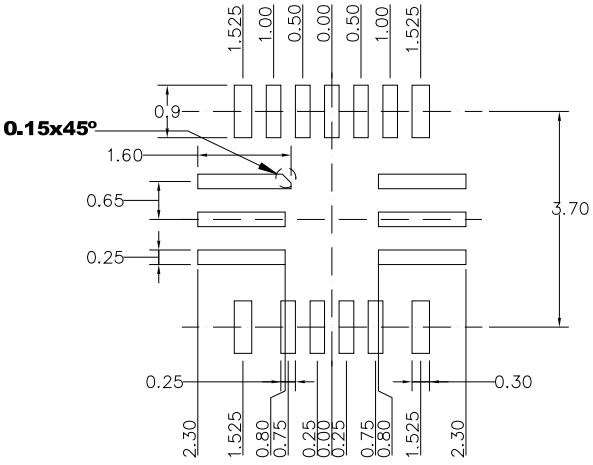
BOTTOM VIEW



SIDE VIEW



SECTION A-A

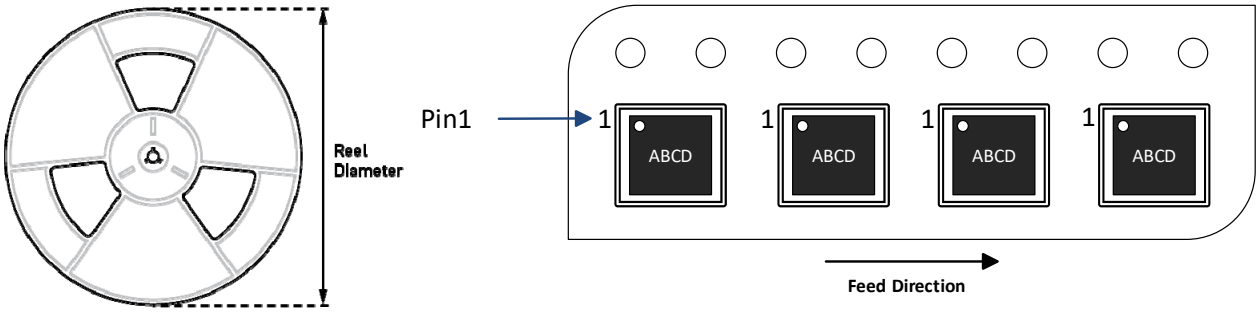


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ6619GRE-AEC1-Z	QFN-19 (4mmx4mm)	5000	N/A	N/A	13 in.	12 mm	8 mm