MPQ7930

MPSafe™ QM, 5.5V, PMIC with 6 Buck Converters, AEC-Q100 Qualified

DESCRIPTION

The MPQ7930 device is a power management IC (PMIC) designed meet the power management requirements of processors used in various safety-relevant automotive systems.

Six integrated synchronous buck converters can be configured as 3 dual-phase or 6 single-phase converters. With dynamic voltage scaling, the output voltage of each converter can be changed during normal operation. The PMBus interface provides packet error checking (PEC) and integrated multi-page one-time programmable (MOTP) memory for a high degree of configurability.

Six enable pins allow each regulator to be sequenced independently for flexible timing control. This allows the device to meet a wide variety of sequencing requirements.

To prevent overshoot during start-up, soft-start functionality is featured on each converter, and the slew rate can be configured via the MOTP.

2MHz, fixed-frequency pulse-width modulation (PWM) control regulates the output voltage (V_{OUT}), offers fast transient performance, and allows for a large reduction in external inductor and capacitor values. In addition, frequency spread spectrum (FSS) reduces EMI noise.

Full protection features include under-voltage lockout (UVLO), over-current protection (OCP), under-voltage protection (UVP), over-voltage protection (OVP), and thermal shutdown.

The MPQ7930 is available in a TQFN-32 (5mmx5mm) package, and is AEC-Q100 qualified.

FEATURES

- Designed for Automotive Applications:
  - 2.7V to 5.5V Input Voltage (V_{IN}) Range
  - -40°C to +150°C Junction Temperature Rating
- Reduced Board Size and BOM:
  - Six Synchronous Buck Converters (Independent or Multi-Phase Operation): Two 4A, Two 3A, and Two 1A
  - Integrated and Adjustable Compensation Network for each Buck Converter
  - Dynamic Voltage Scaling
  - PMBus Interface with Packet Error Checking (PEC)
- Optimized for EMC/EMI:
  - 180° Phase Shift between Bucks 1, 3, and 6, then Bucks 2, 4, and 5
  - 2MHz Switching Frequency (f_{SW})
  - Frequency Spread Spectrum (FSS)
- Additional Features:
  - Multi-Page One-Time Programmable (MOTP) Memory
  - Configurable Sequencing
  - Power Good Output
  - ALERT Indicator
  - Over-Current Protection (OCP), Over-Voltage Protection (OVP), and Under-Voltage Protection (UVP) with Hiccup
  - Available in a TQFN-32 (5mmx5mm) Package with Wettable Flank
  - Available in AEC-Q100 Grade 1

APPLICATIONS

- Advanced Driver Assistance Systems (ADAS)
- Surround View System Electronic Control Units (ECUs)
- ADAS Domain Controllers
- Drive Assist ECUs

TYPICAL APPLICATION

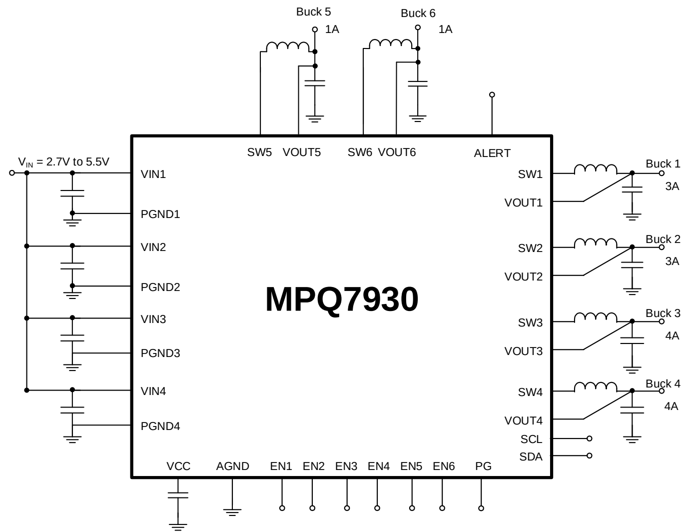
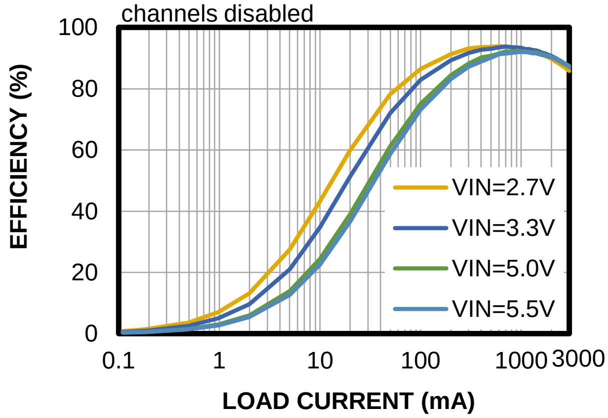


Figure 1: Typical Application

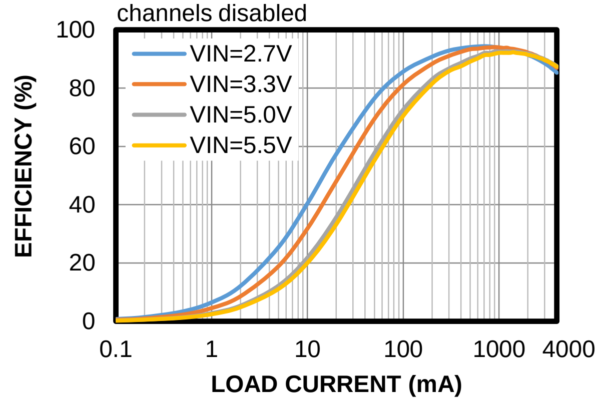
Efficiency vs. Load Current (Buck 1)

V_{OUT1} = 1.8V, f_{SW} = 2MHz, L1 = 1.5µH, DCR = 23.6mΩ, XAL4020-152MEB, other channels disabled



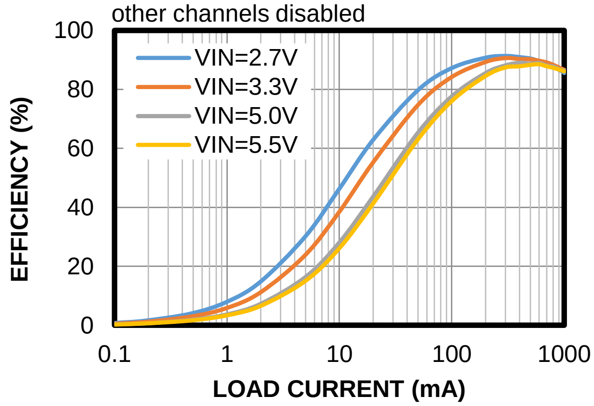
Efficiency vs. Load Current (Buck 3)

V_{OUT3} = 1.8V, f_{SW} = 2MHz, L3 = 1.0µH, DCR = 14.6mΩ, XEL4020-102MEB, other channels disabled



Efficiency vs. Load Current (Buck 5)

V_{OUT5} = 1.8V, f_{SW} = 2MHz, L5 = 3.3µH, DCR = 105mΩ, VCTA32251B-3R3MS6-99, other channels disabled



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating***
MPQ7930GUTE-xxxx-AEC1**	TQFN-32 (5mmx5mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ7930GUTE-xxxx-AEC1-Z).

** "xxxx" is the configuration code identifier for the register settings stored in the OTP register. The first value must be a numerical value (0–9), while the last three values can be a hexadecimal value between 0 and F. The default code is "0000". Contact an MPS FAE to create this unique number.

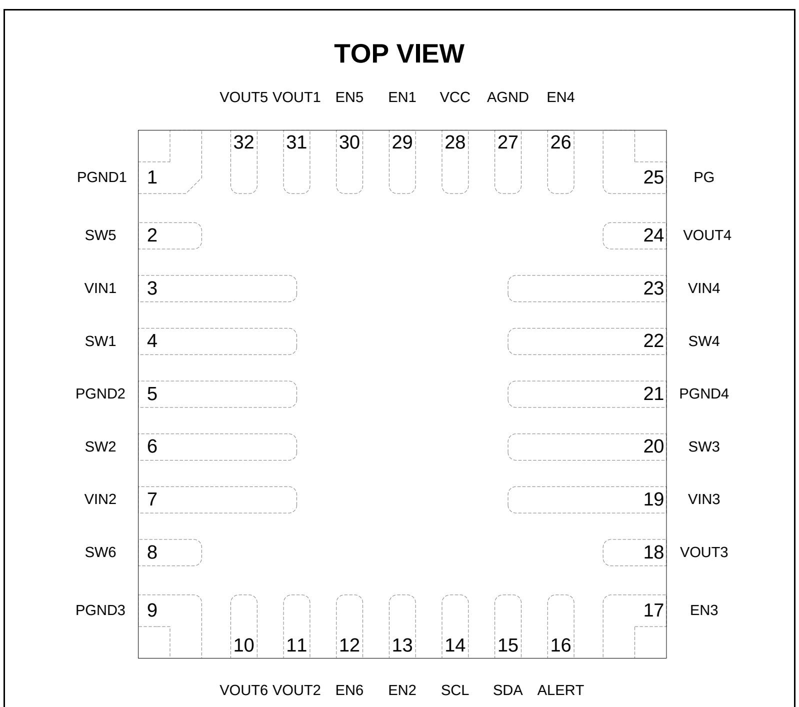
*** Moisture Sensitivity Level Rating

TOP MARKING

MPSYYWW
MP7930
LLLLLLL
E

MPS: MPS prefix
YY: Year code
WW: Week code
MP7930: Part number
LLLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



TQFN-32 (5mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 5, 9, 21	PGNDx	**Power ground.** The PGND pins are internally connected.
2	SW5	**Switch node 5.** The SW5 pin is the switching node of the internal power switches for buck converter 5. Float this pin or connect a 100kΩ resistor between this pin and GND if it is not used.
3, 7, 19, 23	VINx	**Input supply voltage.** VIN supplies power to all the internal control circuitries and the power switches. The decoupling capacitor connected from VIN to ground must be placed close to VIN to minimize switching spikes. The VIN pins are not internally connected. It is not allowed to separate different VIN pins; connect the VIN pins using copper pours and vias.
4	SW1	**Switch node 1.** The SW1 pin is the switching node of the internal power switches for buck converter 1. Float this pin or connect a 100kΩ resistor between this pin and GND if it is not used.
6	SW2	**Switch node 2.** The SW2 pin is the switching node of the internal power switches for buck converter 2. Float this pin or connect a 100kΩ resistor between this pin and GND if it is not used.
8	SW6	**Switch node 6.** The SW6 pin is the switching node of the internal power switches for buck converter 6. Float this pin or connect a 100kΩ resistor between this pin and GND if it is not used.
10	VOUT6	**Feedback input pin 6.** The VOUT6 pin is the feedback voltage input for buck converter 6. Float this pin or connect a 100kΩ resistor between this pin and GND if it is not used.
11	VOUT2	**Feedback input pin 2.** The VOUT2 pin is the feedback voltage input for buck converter 2. Float this pin or connect a 100kΩ resistor between this pin and GND if it is not used.
12	EN6	**Buck 6 enable.** Pull the EN6 pin below the specified threshold (1.3V) to shut down buck 6. Pull this pin up above the specified threshold (1.4V) to enable buck 6. There is an internal pull-down resistor that depends on the pin's voltage. After V_{CC} is on, the pull-down resistor is 1.95MΩ when the pin voltage exceeds 1.4V, or it is 1.05MΩ when the pin voltage is below 1.4V. Connect this pin to GND if it is not used.
13	EN2	**Buck 2 enable.** Pull the EN2 pin below the specified threshold (1.3V) to shut down buck 2. Pull this pin up above the specified threshold (1.4V) to enable buck 2. There is an internal pull-down resistor that depends on the pin's voltage. After V_{CC} is on, the pull-down resistor is 1.95MΩ when the pin voltage exceeds 1.4V, or it is 1.05MΩ when the pin voltage is below 1.4V. Connect this pin to GND if it is not used.
14	SCL	**PMBus serial clock.** The SCL pin is an open-drain port, and it cannot be floated. Use an external pull-up resistor to connect this pin to the PMBus supply rail. Connect this pin to GND if it is not used.
15	SDA	**PMBus serial data.** This pin is an open-drain port, and it cannot be floated. Use an external pull-up resistor to connect this pin to the PMBus supply rail. Connect this pin to GND if it is not used.
16	ALERT	**Open-drain fault output.** The ALERT pin asserts active low if a failure occurs. Use a resistor to pull ALERT up to a power source. Float this pin or connect this pin to GND if not used.
17	EN3	**Buck 3 enable.** Pull the EN3 pin below the specified threshold (1.3V) to shut down buck 3. Pull this pin up above the specified threshold (1.4V) to enable buck 3. There is an internal pull-down resistor that depends on the pin's voltage. After V_{CC} is on, the pull-down resistor is 1.95MΩ when the pin voltage exceeds 1.4V, or it is 1.05MΩ when the pin voltage is below 1.4V. Connect this pin to GND if it is not used.
18	VOUT3	**Feedback input pin 3.** The VOUT3 pin is the feedback voltage input for buck converter 3. Float this pin or connect a 100kΩ resistor between this pin and GND if it is not used.

PIN FUNCTIONS *(continued)*

Pin #	Name	Description
20	SW3	Switch node 3. The SW3 pin is the switching node of the internal power switches for buck converter 3. Float this pin or connect a 100kΩ resistor between this pin and GND if it is not used.
22	SW4	**Switch node 4.** The SW4 pin is the switching node of the internal power switches for buck converter 4. Float this pin or connect a 100kΩ resistor between this pin and GND if it is not used.
24	VOUT4	**Feedback input pin 4.** The VOUT4 pin is the feedback voltage input for buck converter 4. Float this pin or connect a 100kΩ resistor between this pin and GND if it is not used.
25	PG	**Power good indicator.** The output of PG is an open drain of an N-channel MOSFET. PG goes high if all the output voltages are within +4.5%/-3.5% or +6.5%/-5.5% of their nominal voltages. Use a resistor to pull PG up to a power source. Float this pin or connect this pin to GND if not used.
26	EN4	**Buck 4 enable.** Pull the EN4 pin below the specified threshold (1.3V) to shut down buck 4. Pull this pin up above the specified threshold (1.4V) to enable the buck 4. There is an internal pull-down resistor that depends on the pin's voltage. After V_{CC} is on, the pull-down resistor is 1.95MΩ when the pin voltage exceeds 1.4V, or it is 1.05MΩ when the pin voltage is below 1.4V. Connect this pin to GND if it is not used.
27	AGND	**Analog ground.** The AGND pin is the reference GND for the internal logic and signal circuit. AGND is not internally connected to the power ground. Ensure that AGND is connected to power ground in the PCB.
28	VCC	**Internal bias supply.** The internal, 3.35V low-dropout (LDO) regulator supplies power to the control circuit and gate drivers. Connect a 10µF capacitor from VCC to AGND with a trace that is as short as possible.
29	EN1	**Buck 1 enable.** Pull the EN1 pin below the specified threshold (1.3V) to shut down buck 1. Pull this pin up above the specified threshold (1.4V) to enable the buck 1. There is an internal pull-down resistor that depends on the pin's voltage. After V_{CC} is on, the pull-down resistor is 1.95MΩ when the pin voltage exceeds 1.4V, or it is 1.05MΩ when the pin voltage is below 1.4V. Connect this pin to GND if it is not used.
30	EN5	**Buck 5 enable.** Pull the EN5 pin below the specified threshold (1.3V) to shut down buck 5. Pull this pin up above the specified threshold (1.4V) to enable the buck 5. There is an internal pull-down resistor that depends on the pin's voltage. After V_{CC} is on, the pull-down resistor is 1.95MΩ when the pin voltage exceeds 1.4V, or it is 1.05MΩ when the pin voltage is below 1.4V. Connect this pin to GND if it is not used.
31	VOUT1	**Feedback input pin 1.** The VOUT1 pin is the feedback voltage input for buck converter 1. Float this pin or connect a 100kΩ resistor between this pin and GND if it is not used.
32	VOUT5	**Feedback input pin 5.** The VOUT5 pin is the feedback voltage input for buck converter 5. Float this pin or connect a 100kΩ resistor between this pin and GND if it is not used.

ABSOLUTE MAXIMUM RATINGS (1)

VINx, SWx ....-0.3V to +6.5V
EN_X ....-0.3V to +5V
All other pins ....-0.3V to +4V
Continuous power dissipation (T_A = 25°C) (2)(6)
QFN-32 (5mmx5mm) 6.16W
Operating junction temperature ....150°C
Lead temperature ....260°C
Storage temperature .... -65°C to +150°C

ESD Ratings

Human body model (HBM) ....Class 2 (3)
Charged-device model (CDM)........ Class C2b (4)

Recommended Operating Conditions

Supply voltage (V_{IN}) ....2.7V to 5.5V
Output voltage (V_{OUTx})............. 0.20625V to 3.6V
Operating junction temp (T_J) .... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

TQFN-32 (5mmx5mm)
JESD51-7...........................31.7….2.6....°C/W (5)
EVQ7930-UT-00A..............20.3.....0.7…°C/W (6)

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002.
4) Per AEC-Q100-011.
5) Measured on a JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The value of θ_{JC} shows the thermal resistance from junction-to-case bottom.
6) Measured on an MPS standard EVB: EVQ7930-UT-00A, a 9cmx9cm, 2oz. copper, 4-layer PCB. The value of θ_{JC} shows the thermal resistance from junction-to-case top.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply Voltage						
V_{IN} under-voltage lockout (UVLO) rising threshold	V_{IN_UVLO}		2.4		2.8	V
V_{IN} UVLO hysteresis	$V_{IN\_UVLO\_HYS}$			180		mV
V_{IN} quiescent current	I_{Q_ON}	All bucks on, no switching			20	mA
V_{IN} shutdown current	I_{Q_OFF}	All bucks off, all enables low			150	µA
VCC Regulator						
VCC regulation voltage	V_{VCC}	C = 2.2µF, I_{OUT} = 10mA	3.1	3.35	3.6	V
V_{CC} UVLO rising threshold	V_{VCC_UVLO}			2.48		V
Oscillator						
Switching frequency range (7)	f_{SW}			2		MHz
Switching frequency accuracy	f_{SW_ACC}		-10		+10	%
Minimum on time (7)	t_{ON_MIN}			60		ns
Minimum off time (7)	t_{OFF_MIN}			60		ns
Spread spectrum modulation frequency spread (7)	f_{SS_SPREAD}			15		%
Spread spectrum modulation frequency rate (7)	f_{SS_RATE}			9		kHz
Dynamic Output Voltage						
VOUT output range (7)	V_{OUT}	VOUT_SL = 1	0.20625		1.8	V
		VOUT_SL = 2	0.4125		3.6	V
VOUT accuracy	V_{OUT_ACC}	VOUT_SL = 1, V_{OUT} = 600mV, V_{CC} = 3.35V	-1.5		+1.5	%
		VOUT_SL = 1, V_{OUT} = 600mV, V_{CC} = 2.5V	-1.5		+1.5	%
VOUT start-up slew rate range (7)	$V_{OUTSLEW\_ST}$	VOUT_SL = 1	1.25		10	mV/µs
		VOUT_SL = 2	2.5		20	mV/µs
VOUT start-up slew rate accuracy	$V_{OUTSLEW\_ST\_ACC}$		-15		+15	%
VOUT shutdown slew rate range (7)	$V_{OUTSLEW\_SP}$	VOUT_SL = 1	1.25		10	mV/µs
		VOUT_SL = 2	2.5		20	mV/µs
VOUT shutdown slew rate accuracy	$V_{OUTSLEW\_SP\_ACC}$		-15		+15	%
VOUT dynamic slew rate range (7)	$V_{OUTSLEW}$	VOUT_SL = 1	2.5		20	mV/µs
		VOUT_SL = 2	5		40	mV/µs
VOUT dynamic slew rate accuracy	$V_{OUTSLEW\_ACC}$		-15		+15	%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Start-up delay time range (7)	t_{ON_DELAY}		0		7750	µs
Shutdown delay time range (7)	t_{OFF_DELAY}		0		7750	µs
Buck Converter 1 (Buck 1)						
Buck 1 high-side switch on resistance	$R_{DS\_HS\_BUCK1}$			40	90	mΩ
Buck 1 low-side switch on resistance	$R_{DS\_LS\_BUCK1}$			20	45	mΩ
SW1 switch leakage current	I_{ILEAK_BUCK1}				50	µA
SW1 peak current limit (7)	$I_{LIM\_HS\_BUCK1}$	0xCE = ’b00	4	6	7.8	A
SW1 valley current limit (7)	$I_{LIM\_LS\_BUCK1}$	0xCE = ’b00	3	4	5.1	A
SW1 ZCD current (7)	I_{ZCD_BUCK1}				300	mA
SW1 reverse current limit (7)	I_{REV_BUCK1}	0xCE = ’b00	2	3	4	A
VOUT1 feedback leakage	R_{FB1_BUCK1}	VOUT_SL = 1	12			kΩ
	R_{FB2_BUCK1}	VOUT_SL = 2	12			kΩ
VOUT1 output discharge	R_{DIS_BUCK1}			100		Ω
Buck Converter 2 (Buck 2)						
Buck 2 high-side switch on resistance	$R_{DS\_HS\_BUCK2}$			40	90	mΩ
Buck 2 low-side switch on resistance	$R_{DS\_LS\_BUCK2}$			20	45	mΩ
SW2 switch leakage current	I_{ILEAK_BUCK2}				50	µA
SW2 peak current limit (7)	$I_{LIM\_HS\_BUCK2}$	0xCE = ’b00	4	6	7.8	A
SW2 valley current limit (7)	$I_{LIM\_LS\_BUCK2}$	0xCE = ’b00	3	4	5.1	A
SW2 ZCD current (7)	I_{ZCD_BUCK2}				300	mA
SW2 reverse current limit (7)	I_{REV_BUCK2}	0xCE=’b00	2	3	4	A
VOUT2 feedback leakage	R_{FB1_BUCK2}	VOUT_SL = 1	12			kΩ
	R_{FB2_BUCK2}	VOUT_SL = 2	12			kΩ
VOUT2 output discharge	R_{DIS_BUCK2}			100		Ω
Buck Converter 3 (Buck 3)						
Buck 3 high-side switch on resistance	$R_{DS\_HS\_BUCK3}$			30	55	mΩ
Buck 3 low-side switch on resistance	$R_{DS\_LS\_BUCK3}$			16	32	mΩ
SW3 switch leakage current	I_{ILEAK_BUCK3}				60	µA
SW3 peak current limit (7)	$I_{LIM\_HS\_BUCK3}$	0xCE = ’b00	5.5	8	11	A
SW3 valley current limit (7)	$I_{LIM\_LS\_BUCK3}$	0xCE = ’b00	4	4.8	5.8	A
SW3 ZCD current (7)	I_{ZCD_BUCK3}				400	mA
SW3 reverse current limit (7)	I_{REV_BUCK3}	0xCE = ’b00	3.5	4.5	5.5	A
VOUT3 feedback leakage	R_{FB1_BUCK3}	VOUT_SL = 1	12			kΩ
	R_{FB2_BUCK3}	VOUT_SL = 2	12			kΩ
VOUT3 output discharge	R_{DIS_BUCK3}			100		Ω
Buck Converter 4 (Buck 4)						
Buck 4 high-side switch on resistance	$R_{DS\_HS\_BUCK4}$			30	55	mΩ
Buck 4 low-side switch on resistance	$R_{DS\_LS\_BUCK4}$			16	32	mΩ
SW4 switch leakage current	I_{ILEAK_BUCK4}				60	µA
SW4 peak current limit (7)	$I_{LIM\_HS\_BUCK4}$	0xCE = ’b00	5.5	8	11	A
SW4 valley current limit (7)	$I_{LIM\_LS\_BUCK4}$	0xCE = ’b00	4	4.8	5.8	A
SW4 ZCD current (7)	I_{ZCD_BUCK4}				400	mA
SW4 reverse current limit (7)	I_{REV_BUCK4}	0xCE = ’b00	3.5	4.5	5.5	A
VOUT4 feedback leakage	R_{FB1_BUCK4}	VOUT_SL = 1	12			kΩ
	R_{FB2_BUCK4}	VOUT_SL = 2	12			kΩ
VOUT4 output discharge	R_{DIS_BUCK4}			100		Ω

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Buck Converter 5 (Buck 5)						
Buck 5 high-side switch on resistance	$R_{DS\_HS\_BUCK5}$			130	250	mΩ
Buck 5 low-side switch on resistance	$R_{DS\_LS\_BUCK5}$			75	140	mΩ
SW5 switch leakage current	I_{ILEAK_BUCK5}				20	µA
SW5 peak current limit (7)	$I_{LIM\_HS\_BUCK5}$	0xCE = ’b00	1.2	1.8	2.7	A
SW5 valley current limit (7)	$I_{LIM\_LS\_BUCK5}$	0xCE = ’b00	0.9	1.5	2	A
SW5 ZCD current (7)	I_{ZCD_BUCK5}				175	mA
SW5 reverse current limit (7)	I_{REV_BUCK5}	0xCE = ’b00	0.7	1.1	1.4	A
VOUT5 feedback leakage	R_{FB1_BUCK5}	VOUT_SL = 1	12			kΩ
	R_{FB2_BUCK5}	VOUT_SL = 2	12			kΩ
VOUT5 output discharge	R_{DIS_BUCK5}			100		Ω
Buck Converter 6 (Buck 6)						
Buck 6 high-side switch on resistance	$R_{DS\_HS\_BUCK6}$			130	250	mΩ
Buck 6 low-side switch on resistance	$R_{DS\_LS\_BUCK6}$			75	140	mΩ
SW6 switch leakage current	I_{ILEAK_BUCK6}				20	µA
SW6 peak current limit (7)	$I_{LIM\_HS\_BUCK6}$		1.2	1.8	2.7	A
SW6 valley current limit (7)	$I_{LIM\_LS\_BUCK6}$		0.9	1.5	2	A
SW6 ZCD current (7)	I_{ZCD_BUCK6}				175	mA
SW6 reverse current limit (7)	I_{REV_BUCK6}		0.7	1.1	1.4	A
VOUT6 feedback leakage	R_{FB1_BUCK6}	VOUT_SL = 1	12			kΩ
	R_{FB2_BUCK6}	VOUT_SL = 2	12			kΩ
VOUT6 output discharge	R_{DIS_BUCK6}			100		Ω
Thermal Protection						
Thermal warning (7)	T_{TW}		125	140	155	°C
Thermal warning hysteresis (7)	T_{TW_HYS}			20		°C
Thermal shutdown (7)	T_{TSD}		155	170	185	°C
Thermal shutdown hysteresis (7)	T_{TSD_HYS}			20		°C
Output Voltage Protection						
VOUT over-voltage (OV) threshold	V_{OUT_OV}	V_{OUT} = 1.8V	112.5	115	117.5	%
VOUT OV hysteresis	$V_{OUT\_OV\_HYS}$	V_{OUT} = 1.8V		5.5		%
VOUT under-voltage (UV) threshold	V_{OUT_UV}	V_{OUT} = 1.8V	72.5	75	77.5	%
VOUT UV hysteresis	$V_{OUT\_UV\_HYS}$	V_{OUT} = 1.8V		5		%
Hiccup time range (7)	t_{HIC}		2		8	ms
Enable						
ENx logic on threshold	V_{ENx_LOG}		0.25	0.65	1	V
ENx rising threshold	V_{ENx_RISING}		1.25	1.4	1.55	V
ENx falling threshold	$V_{ENx\_FALLING}$		1.15	1.3	1.45	V
ENx voltage hysteresis	V_{ENx_HYS}			100		mV
ENx leakage	I_{ENx}	V_{ENx} = 3.3V			12	µA

ELECTRICAL CHARACTERISTICS *(continued)*

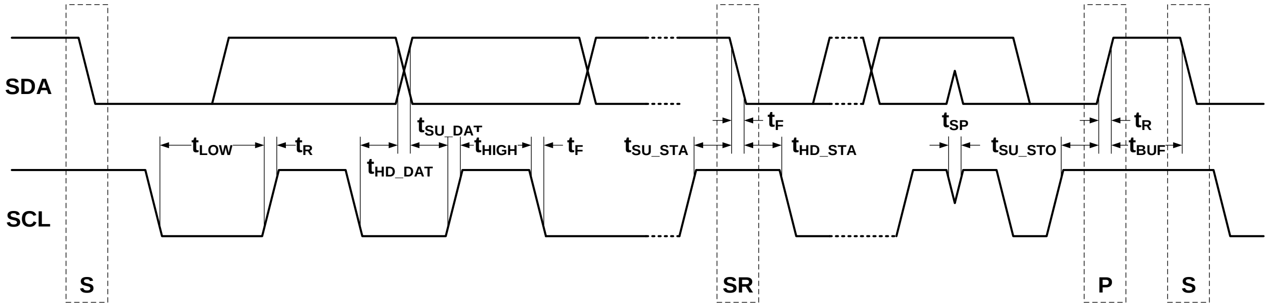
V_{IN} = 5V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Good						
PG OV rising threshold [8]	PG_{OV}	V_{OUT} = 1.8V, percentage of actual V_{REF}, PG_THRESHOLD[0] = 1	102.5	104.5	106.5	%
		V_{OUT} = 1.8V, percentage of actual V_{REF}, PG_THRESHOLD[0] = 0	104.5	106.5	108.5	%
PG OV threshold hysteresis [8]	PG_{OV_HYS}	V_{OUT} = 1.8V		0.5		%
PG UV falling threshold [8]	PG_{UV}	V_{OUT} = 1.8V, percentage of actual V_{REF}, PG_THRESHOLD[0] = 1	94.5	96.5	98.5	%
		V_{OUT} = 1.8V, percentage of actual V_{REF}, PG_THRESHOLD[0] = 0	92.5	94.5	96.5	%
PG UV threshold hysteresis [8]	PG_{UV_HYS}	V_{OUT} = 1.8V		0.5		%
PG sink capability	I_{PG}	I_{PG} = 4mA			300	mV
PG delay range [7]	t_{PG_DELAY}		0		10	ms
ALERT						
ALERT sink capability	I_{RST}	I_{RESET} = 4mA			300	mV
System Clock						
System clock	f_{CLK}			2		MHz
PMBus Logic Interface[7]						
SCL/SDA input logic low	V_{IL}				0.4	V
SCL/SDA input logic high	V_{IH}		1.2			V
SDA output logic low	V_{OL}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency	f_{SCL}				1000	kHz
SCL high time	t_{HIGH}		0.6			µs
SCL low time	t_{LOW}		1.3			µs
Data set-up time	t_{SU_DAT}		100			ns
Data hold time	t_{HD_DAT}		0		0.9	µs
Set-up time for repeated start	t_{SU_STA}		0.6			µs
Hold time for start	t_{HD_STA}		0.6			µs
Bus free time between a start and a stop condition	t_{BUF}		1.3			µs
Set-up time for stop condition	t_{SU_STO}		0.6			µs
Rising time of SCL/SDA	t_R				300	ns
Falling time of SCL/SDA	t_F				300	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance bus for each bus line	C_B				400	pF

Notes:

7) Derived from bench characterization. Not tested in production.
8) Power good threshold is based on the nominal output voltage of each output.

PMBUS-COMPATIBLE INTERFACE TIMING DIAGRAM



S: Start Condition

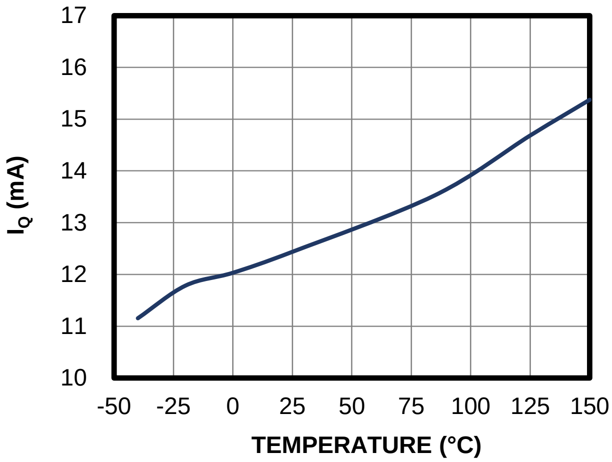
SR: Repeated Start Condition

P: Stop Condition

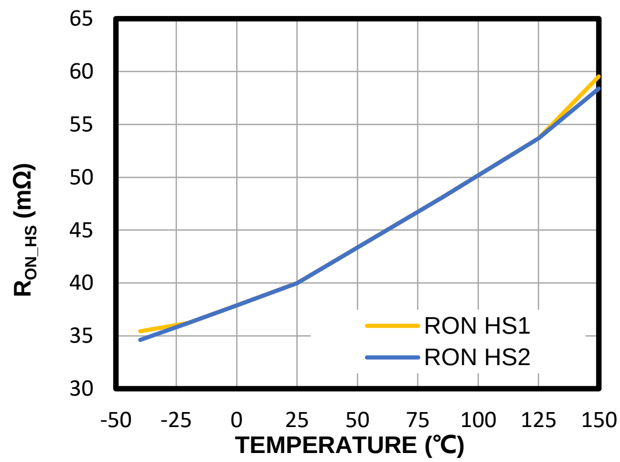
TYPICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40°C to +150°C, unless otherwise noted.

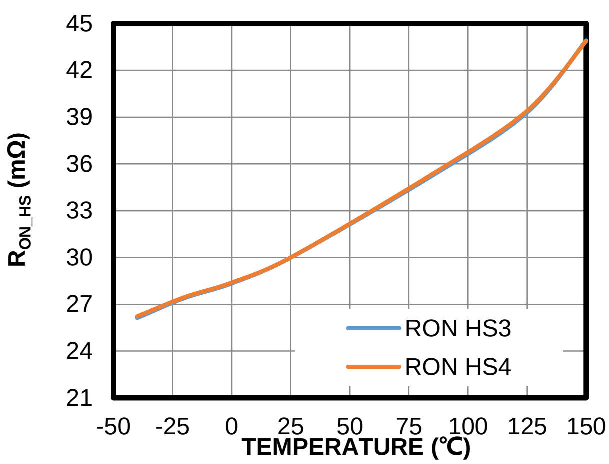
I_Q vs. Temperature



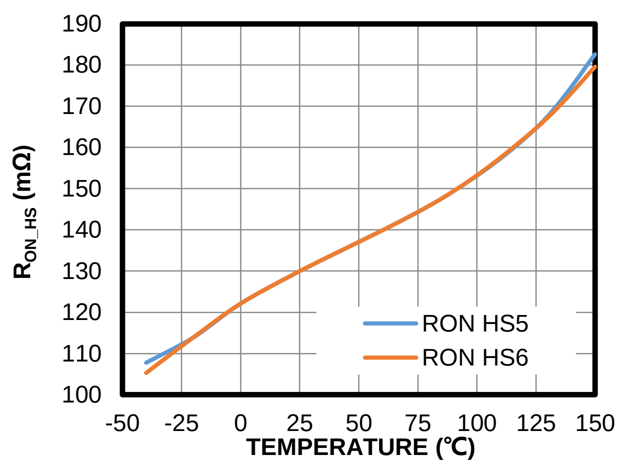
R_{ON_HS} vs. Temperature
Buck 1 and Buck 2



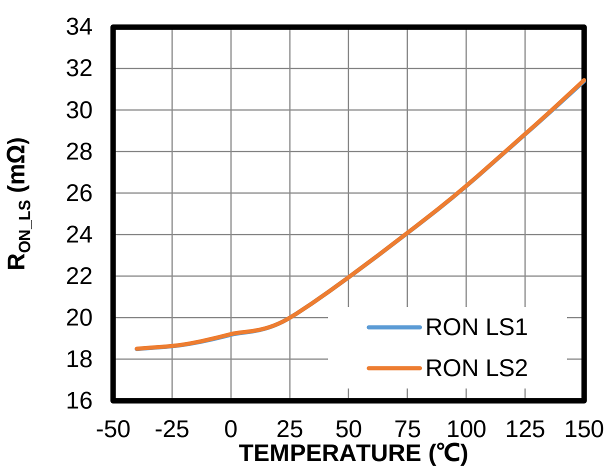
R_{ON_HS} vs. Temperature
Buck 3 and Buck 4



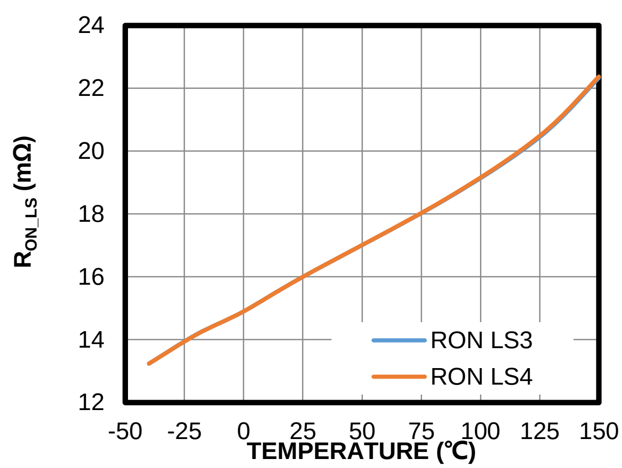
R_{ON_HS} vs. Temperature
Buck 5 and Buck 6



R_{ON_LS} vs. Temperature
Buck 1 and Buck 2



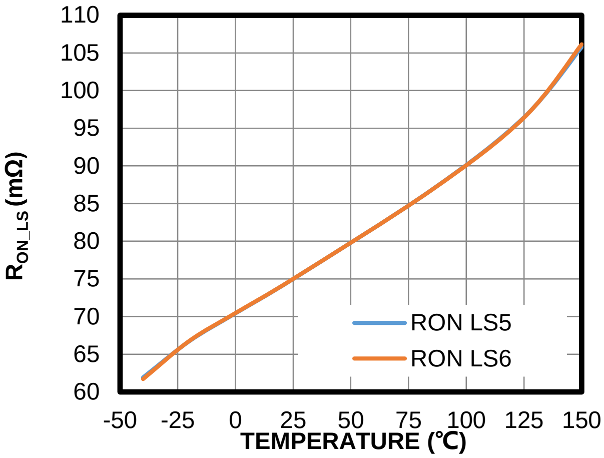
R_{ON_LS} vs. Temperature
Buck 3 and Buck 4



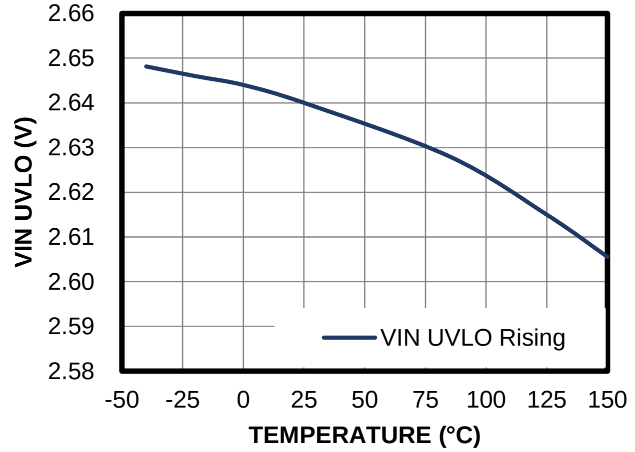
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_J = -40°C to +150°C, unless otherwise noted.

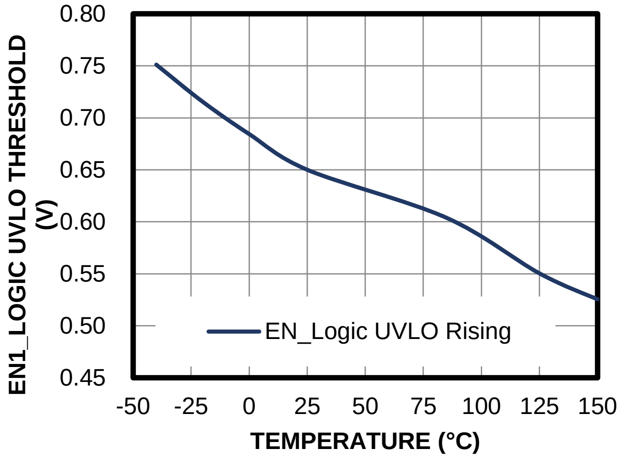
R_{ON_LS} vs. Temperature
Buck 5 and Buck 6



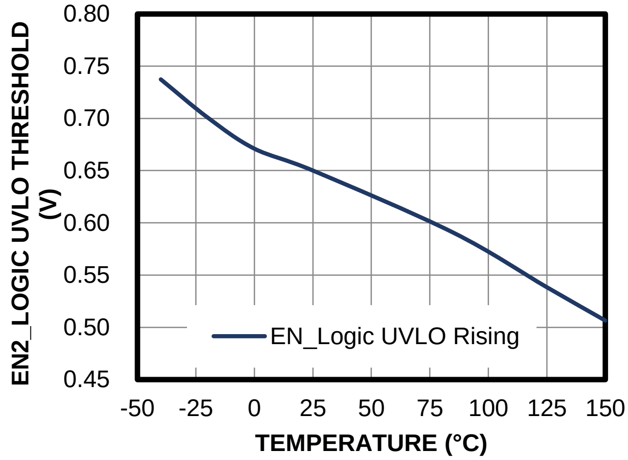
V_{IN} UVLO Threshold vs. Temperature



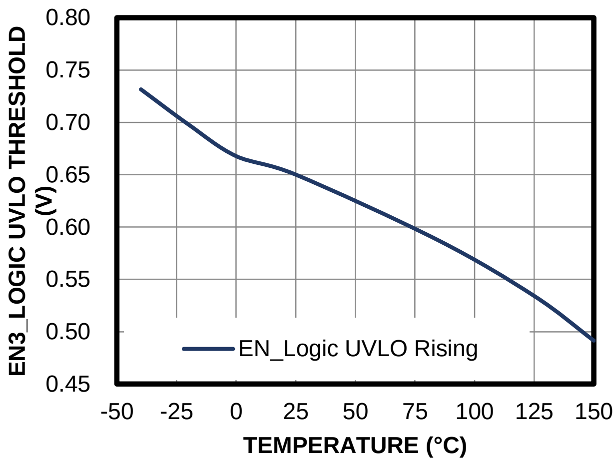
EN1_Logic UVLO Threshold vs. Temperature



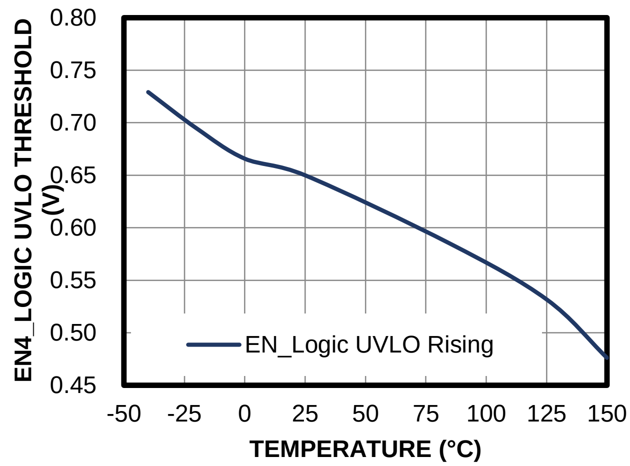
EN2_Logic UVLO Threshold vs. Temperature



EN3_Logic UVLO Threshold vs. Temperature



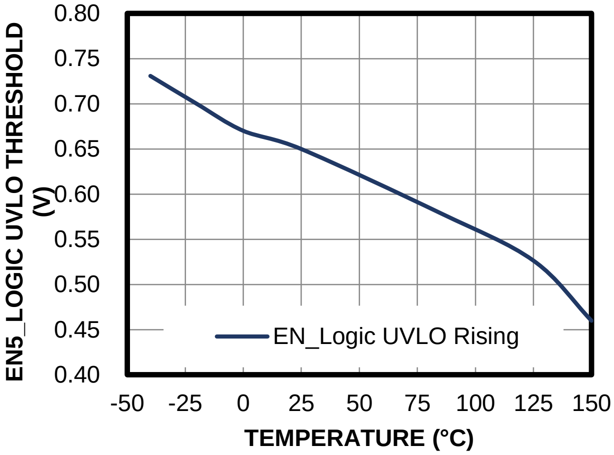
EN4_Logic UVLO Threshold vs. Temperature



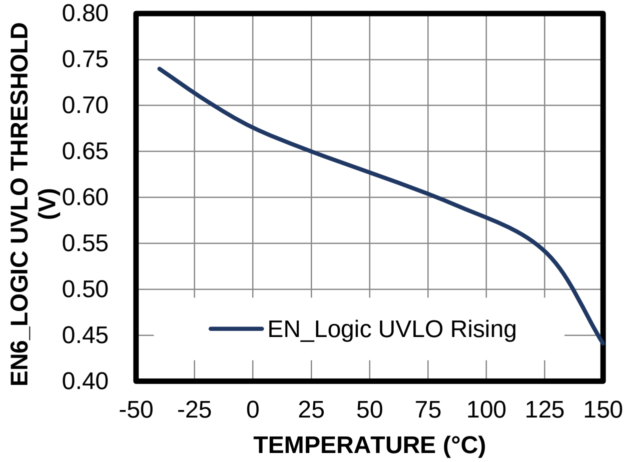
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_J = -40°C to +150°C, unless otherwise noted.

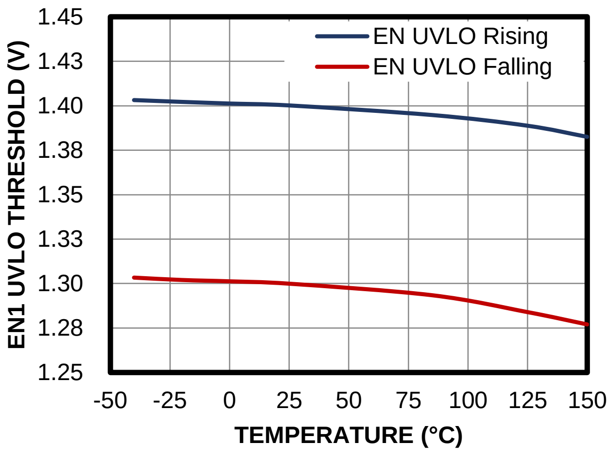
EN5_Logic UVLO Threshold vs. Temperature



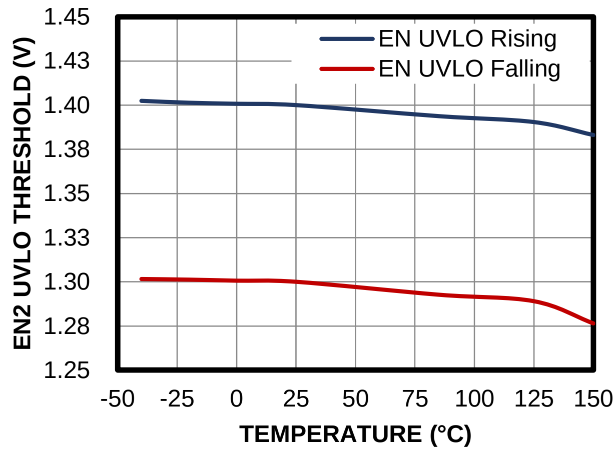
EN6_Logic UVLO Threshold vs. Temperature



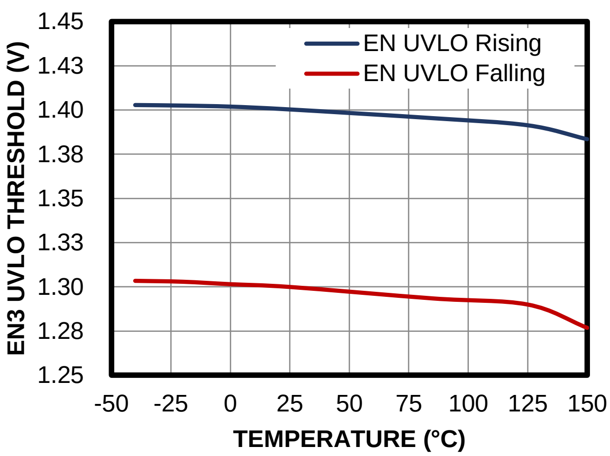
EN1 UVLO Threshold vs. Temperature



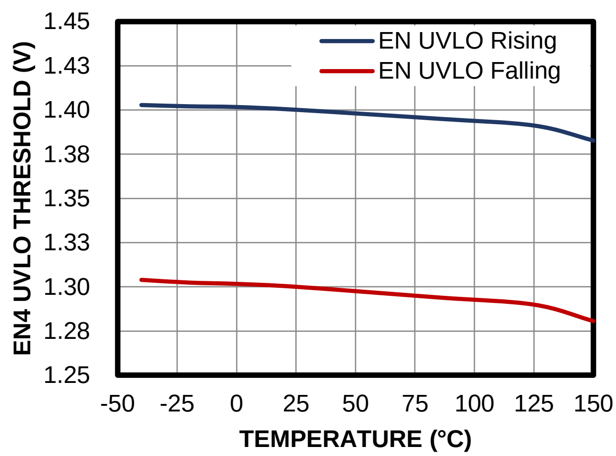
EN2 UVLO Threshold vs. Temperature



EN3 UVLO Threshold vs. Temperature



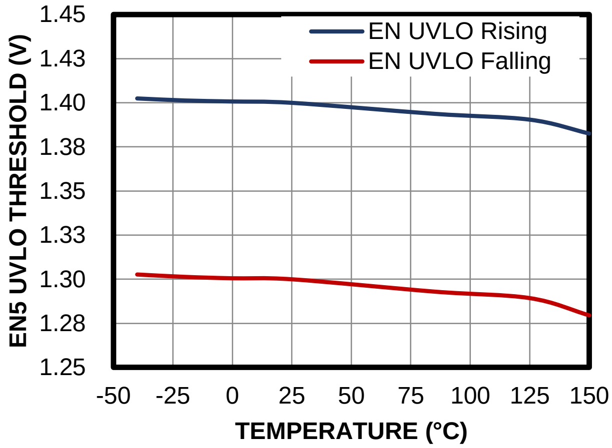
EN4 UVLO Threshold vs. Temperature



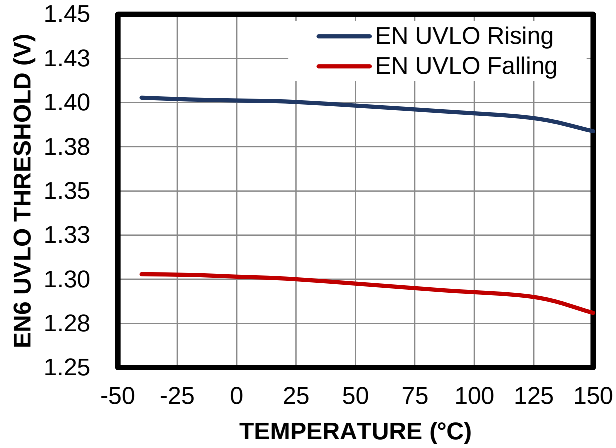
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_J = -40°C to +150°C, unless otherwise noted.

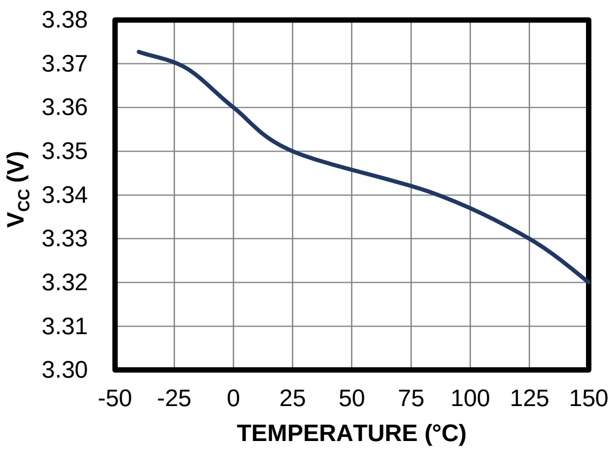
EN5 UVLO Threshold vs. Temperature



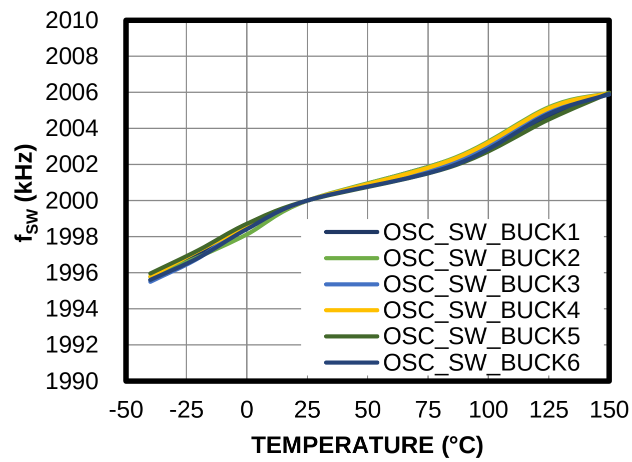
EN6 UVLO Threshold vs. Temperature



V_{CC} vs. Temperature



f_{SW} vs. Temperature

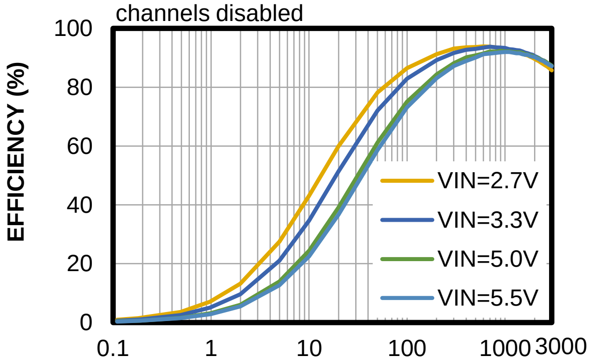


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT1} = V_{OUT2} = V_{OUT3} = V_{OUT4} = V_{OUT5} = V_{OUT6} = 1.8V, L1 = L2 = 1.5µH, L3 = L4 = 1µH, L5 = L6 = 3.3µH, C_{OUT1} = C_{OUT2} = 2 x 22µF, C_{OUT3} = C_{OUT4} = 2 x 22µF, C_{OUT5} = C_{OUT6} = 2 x 4.7µF, f_{SW} = 2MHz, T_A = 25°C, unless otherwise noted.

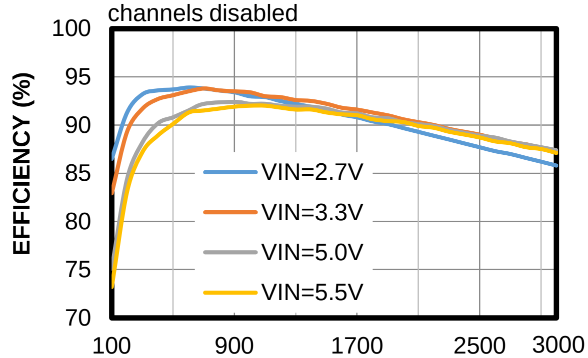
Efficiency vs. Load Current (Buck 1)

V_{OUT1} = 1.8V, f_{SW} = 2MHz, L1 = 1.5µH, DCR = 23.6mΩ, XAL4020-152MEB, other channels disabled



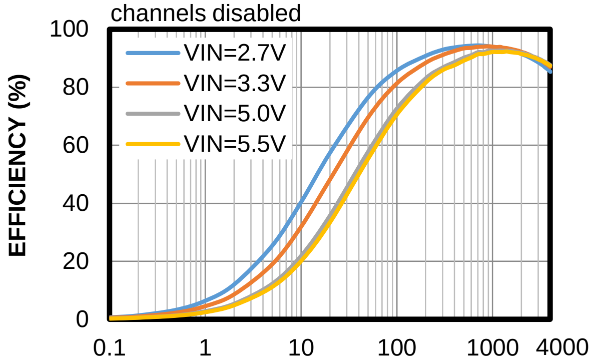
Efficiency vs. Load Current (Buck 1)

V_{OUT1} = 1.8V, f_{SW} = 2MHz, L1 = 1.5µH, DCR = 23.6mΩ, XAL4020-152MEB, other channels disabled



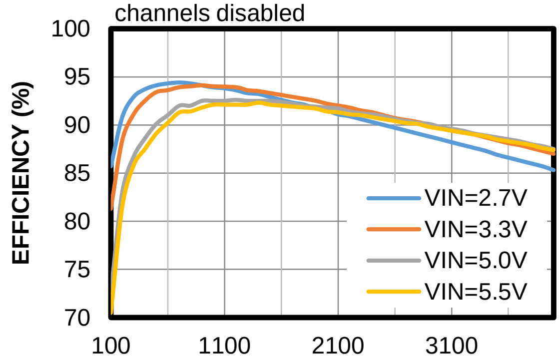
Efficiency vs. Load Current (Buck 3)

V_{OUT3} = 1.8V, f_{SW} = 2MHz, L3 = 1.0µH, DCR = 14.6mΩ, XEL4020-102MEB, other channels disabled



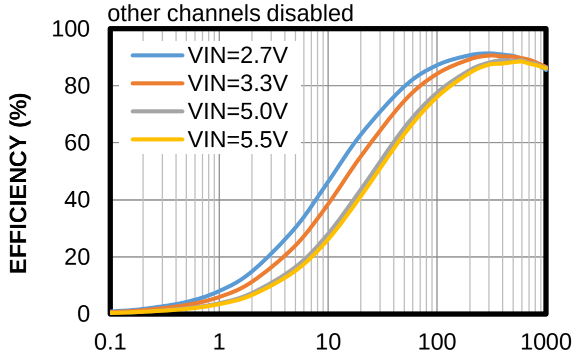
Efficiency vs. Load Current (Buck 3)

V_{OUT3} = 1.8V, f_{SW} = 2MHz, L3 = 1.0µH, DCR = 14.6mΩ, XEL4020-102MEB, other channels disabled



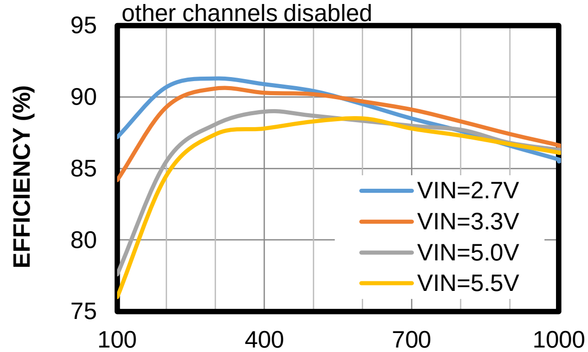
Efficiency vs. Load Current (Buck 5)

V_{OUT5} = 1.8V, f_{SW} = 2MHz, L5 = 3.3µH, DCR = 105mΩ, VCTA32251B-3R3MS6-99, other channels disabled



Efficiency vs. Load Current (Buck 5)

V_{OUT5} = 1.8V, f_{SW} = 2MHz, L5 = 3.3µH, DCR = 105mΩ, VCTA32251B-3R3MS6-99, other channels disabled

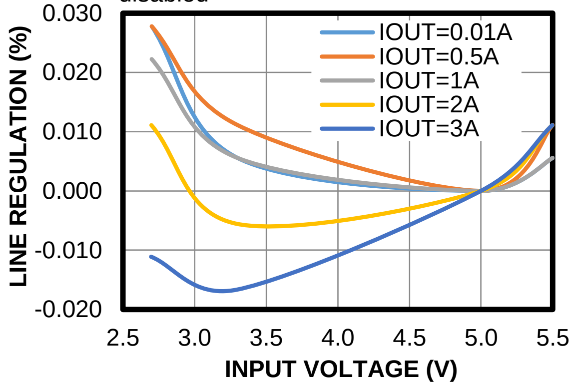


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = V_{OUT2} = V_{OUT3} = V_{OUT4} = V_{OUT5} = V_{OUT6} = 1.8V, L1 = L2 = 1.5µH, L3 = L4 = 1µH, L5 = L6 = 3.3µH, C_{OUT1} = C_{OUT2} = 2 x 22µF, C_{OUT3} = C_{OUT4} = 2 x 22µF, C_{OUT5} = C_{OUT6} = 2 x 4.7µF, f_{SW} = 2MHz, T_A = 25°C, unless otherwise noted.

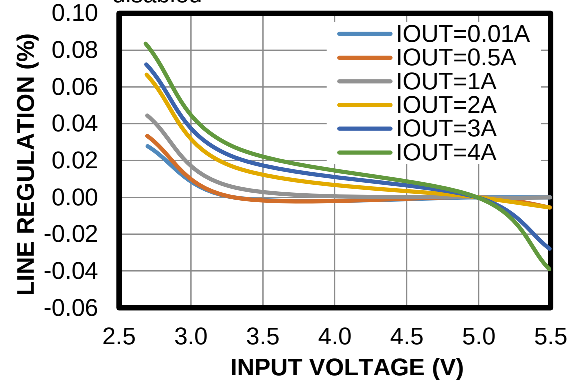
Line Regulation vs. Input Voltage (Buck 1)

V_{OUT1} = 1.8V, FCCM, other channels disabled



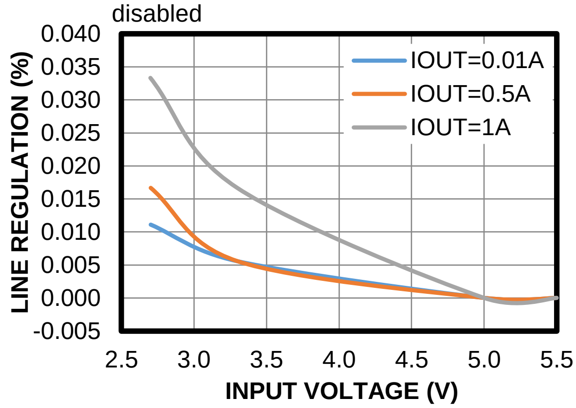
Line Regulation vs. Input Voltage (Buck 3)

V_{OUT3} = 1.8V, FCCM, other channels disabled



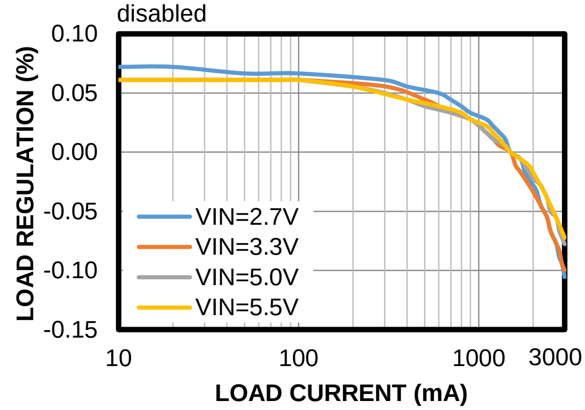
Line Regulation vs. Input Voltage (Buck 5)

V_{OUT5} = 1.8V, FCCM, other channels disabled



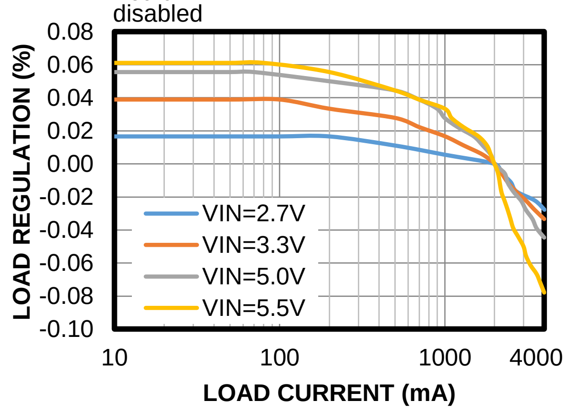
Load Regulation vs. Input Voltage (Buck 1)

V_{OUT1} = 1.8V, FCCM, other channels disabled



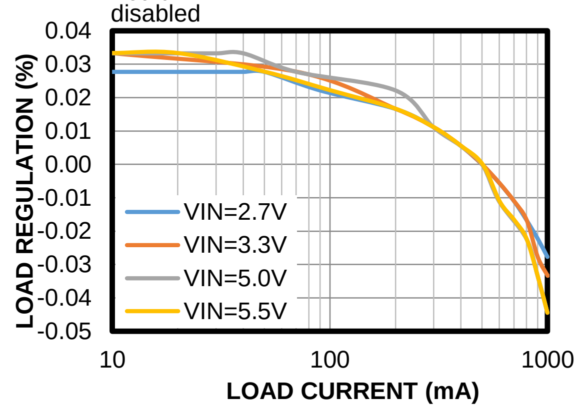
Load Regulation vs. Input Voltage (Buck 3)

V_{OUT3} = 1.8V, FCCM, other channels disabled



Load Regulation vs. Input Voltage (Buck 5)

V_{OUT5} = 1.8V, FCCM, other channels disabled

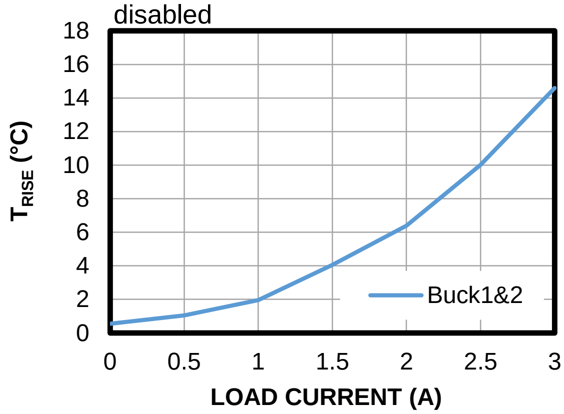


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = V_{OUT2} = V_{OUT3} = V_{OUT4} = V_{OUT5} = V_{OUT6} = 1.8V, L1 = L2 = 1.5μH, L3 = L4 = 1μH, L5 = L6 = 3.3μH, C_{OUT1} = C_{OUT2} = 2 x 22μF, C_{OUT3} = C_{OUT4} = 2 x 22μF, C_{OUT5} = C_{OUT6} = 2 x 4.7μF, f_{SW} = 2MHz, T_A = 25°C, unless otherwise noted.

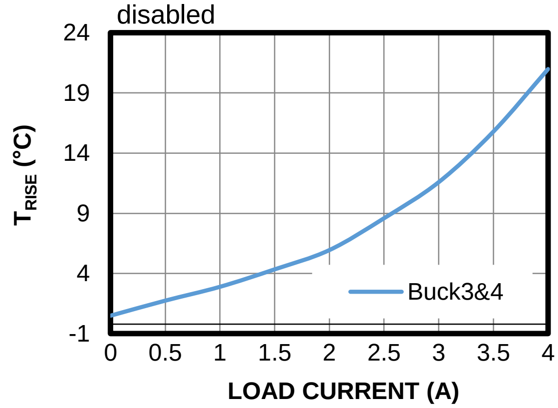
Case Thermal Rise vs. Load Current

V_{IN} =5V, V_{OUT} = 1.8V, other channels disabled



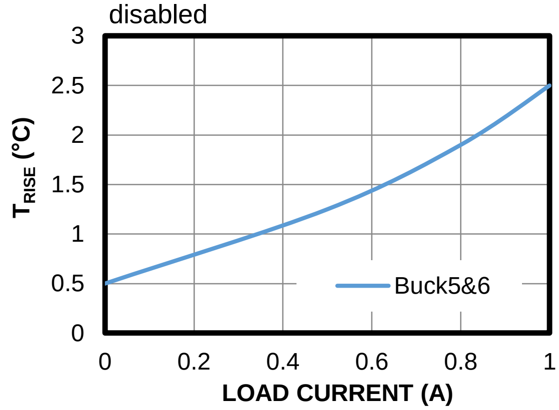
Case Temp Rise vs. Load Current

V_{IN} = 5V, V_{OUT} = 1.8V, other channels disabled



Case Thermal Rise vs. Load Current

V_{IN} = 5V, V_{OUT} = 1.8V, other channels disabled

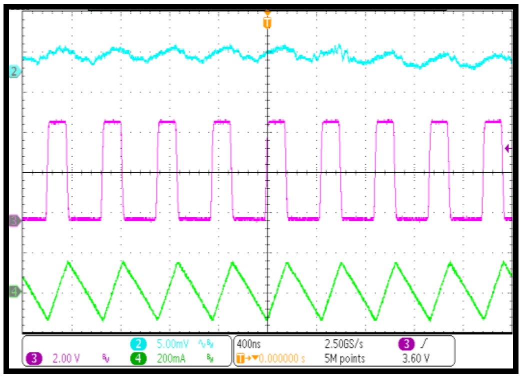


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = V_{OUT2} = V_{OUT3} = V_{OUT4} = V_{OUT5} = V_{OUT6} = 1.8V, L1 = L2 = 1.5µH, L3 = L4 = 1µH, L5 = L6 = 3.3µH, C_{OUT1} = C_{OUT2} = 2 x 22µF, C_{OUT3} = C_{OUT4} = 2 x 22µF, C_{OUT5} = C_{OUT6} = 2 x 4.7µF, f_{SW} = 2MHz, T_A = +25°C, unless otherwise noted.

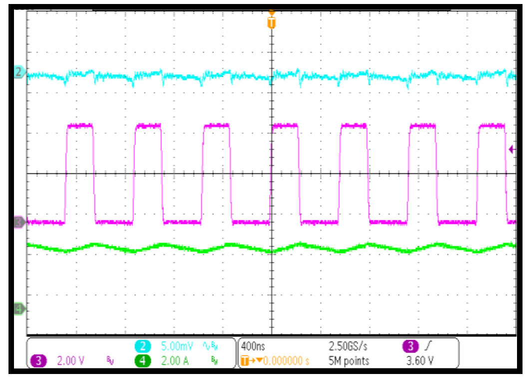
Steady State

Buck 1, all buck rails with no load



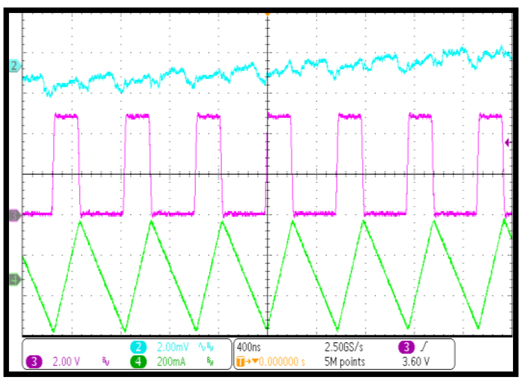
Steady State

Buck 1, I_{OUT1} = 3A, other buck rails with no load



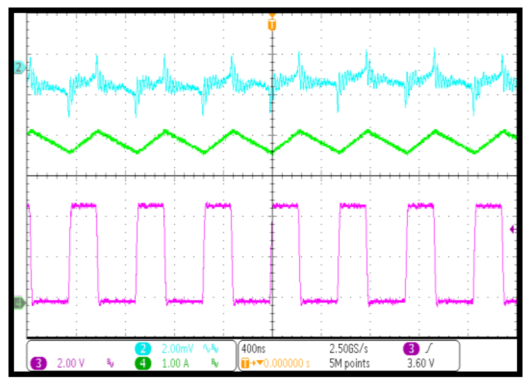
Steady State

Buck 3, all buck rails with no load



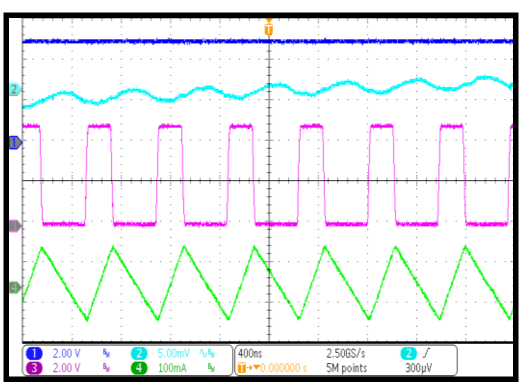
Steady State

Buck 3, I_{OUT3} = 4A, other buck rails with no load



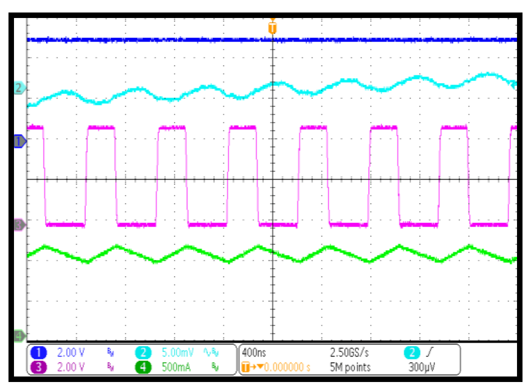
Steady State

Buck 5, all buck rails with no load



Steady State

Buck 5, I_{OUT5} = 1A, other buck rails with no load

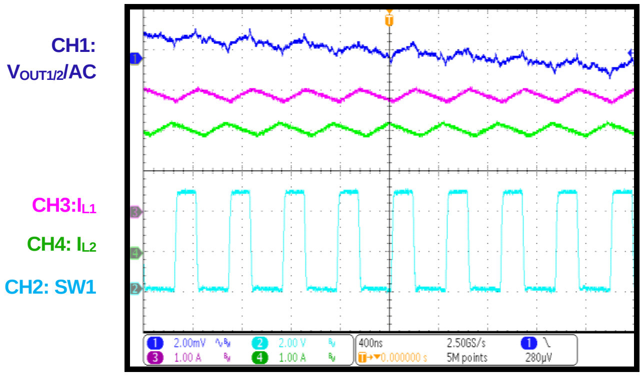


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = V_{OUT2} = V_{OUT3} = V_{OUT4} = V_{OUT5} = V_{OUT6} = 1.8V, L1 = L2 = 1.5µH, L3 = L4 = 1µH, L5 = L6 = 3.3µH, C_{OUT1} = C_{OUT2} = 2 x 22µF, C_{OUT3} = C_{OUT4} = 2 x 22µF, C_{OUT5} = C_{OUT6} = 2 x 4.7µF, f_{SW} = 2MHz, T_A = 25°C, unless otherwise noted.

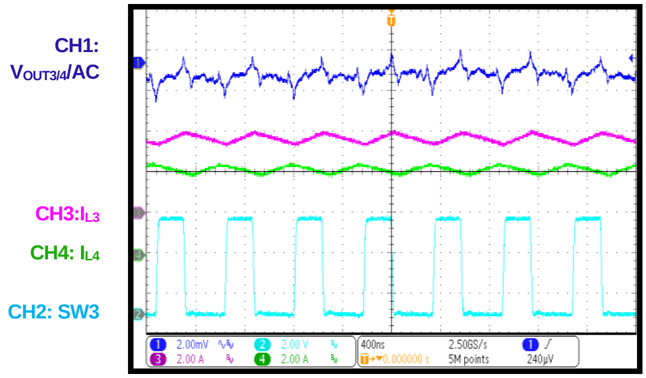
Multi-Phase Steady State

$I_{OUT1/2}$ = 6A, other buck rails with no load



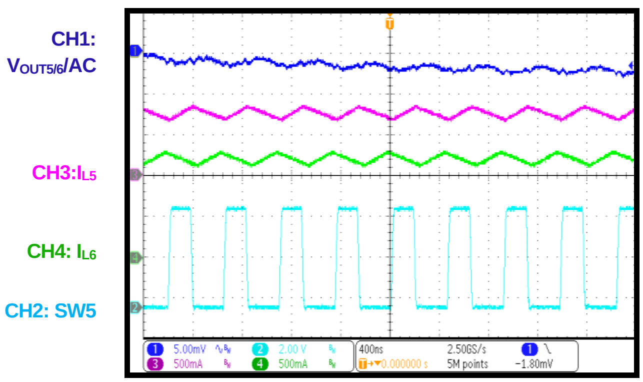
Multi-Phase Steady State

$I_{OUT3/4}$ = 8A, other buck rails with no load



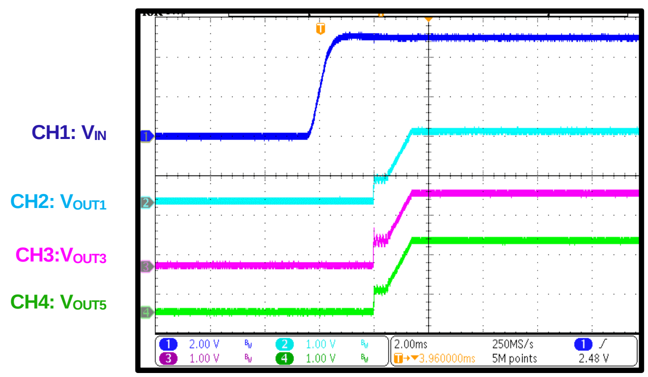
Multi-Phase Steady State

$I_{OUT5/6}$ = 2A, other buck rails with no load



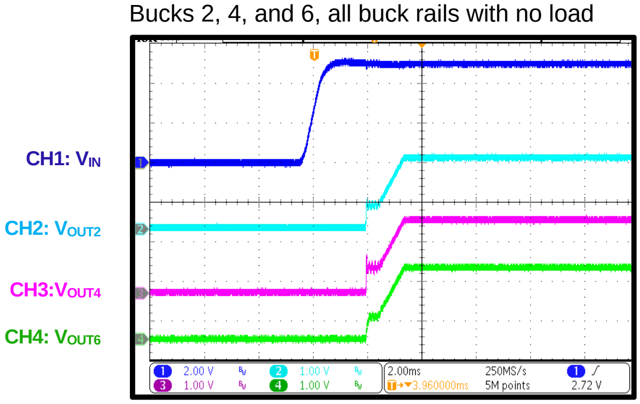
Start-Up through VIN (Start-Up Sequence)

Bucks 1, 3, and 5, all buck rails with no load



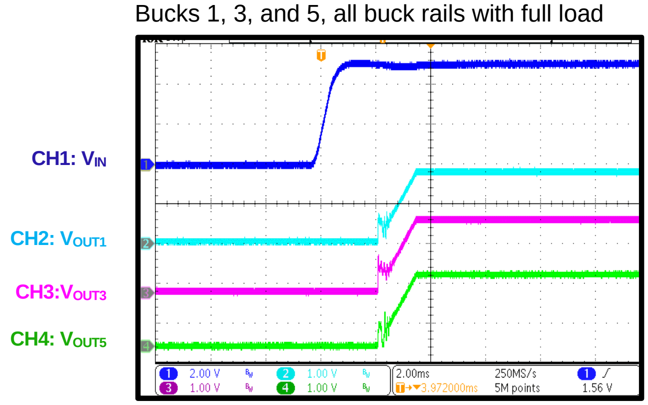
Start-Up through VIN (Start-Up Sequence)

Bucks 2, 4, and 6, all buck rails with no load



Start-Up through VIN (Start-Up Sequence)

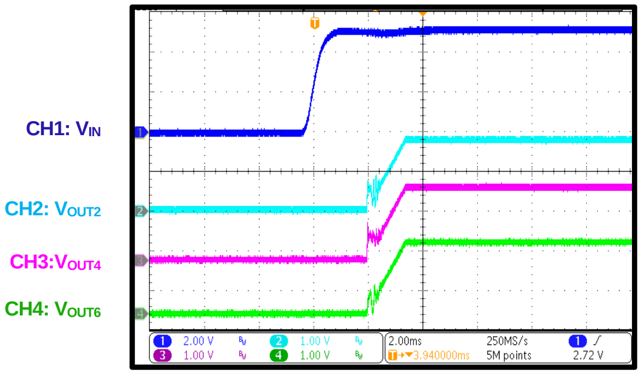
Bucks 1, 3, and 5, all buck rails with full load



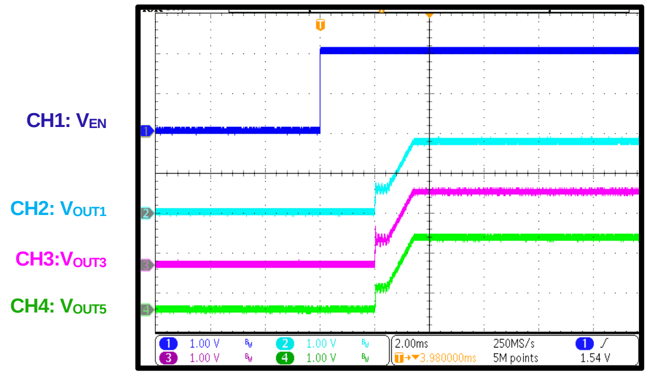
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = V_{OUT2} = V_{OUT3} = V_{OUT4} = V_{OUT5} = V_{OUT6} = 1.8V, L1 = L2 = 1.5µH, L3 = L4 = 1µH, L5 = L6 = 3.3µH, C_{OUT1} = C_{OUT2} = 2 x 22µF, C_{OUT3} = C_{OUT4} = 2 x 22µF, C_{OUT5} = C_{OUT6} = 2 x 4.7µF, f_{SW} = 2MHz, T_A = 25°C, unless otherwise noted.

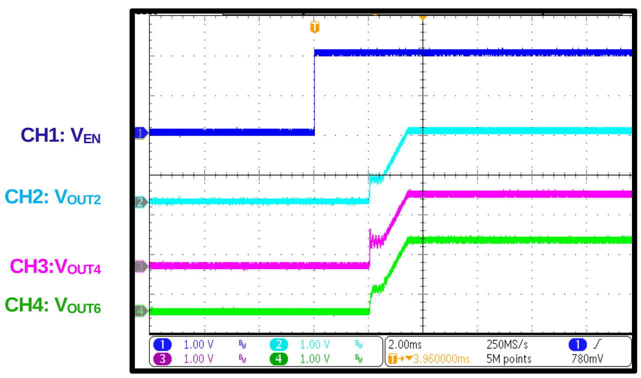
Start-Up through VIN (Start-Up Sequence)
Bucks 2, 4, and 6, all buck rails with full load



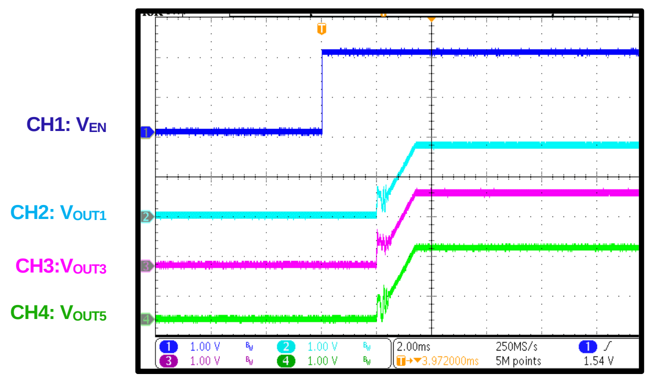
Start-Up through EN (Start-Up Sequence)
Bucks 1, 3, and 5, all buck rails with no load



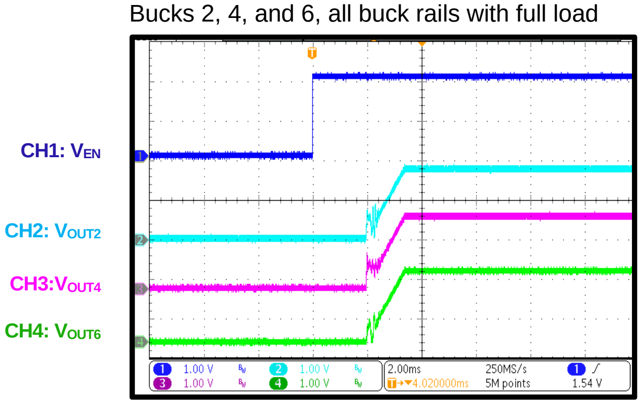
Start-Up through EN (Start-Up Sequence)
Bucks 2, 4, and 6, all buck rails with no load



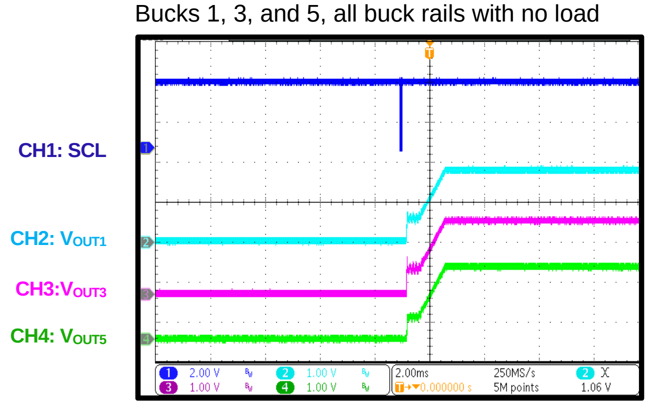
Start-Up through EN (Start-Up Sequence)
Bucks 1, 3, and 5, all buck rails with full load



Start-Up through EN (Start-Up Sequence)
Bucks 2, 4, and 6, all buck rails with full load



Start-Up through PMBus (Start-Up Sequence)
Bucks 1, 3, and 5, all buck rails with no load

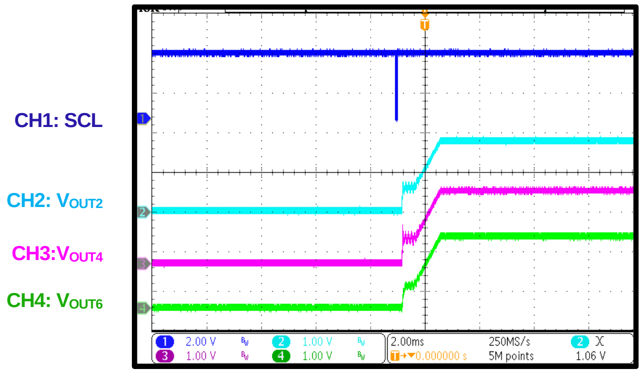


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = V_{OUT2} = V_{OUT3} = V_{OUT4} = V_{OUT5} = V_{OUT6} = 1.8V, L1 = L2 = 1.5µH, L3 = L4 = 1µH, L5 = L6 = 3.3µH, C_{OUT1} = C_{OUT2} = 2 x 22µF, C_{OUT3} = C_{OUT4} = 2 x 22µF, C_{OUT5} = C_{OUT6} = 2 x 4.7µF, f_{SW} = 2MHz, T_A = 25°C, unless otherwise noted.

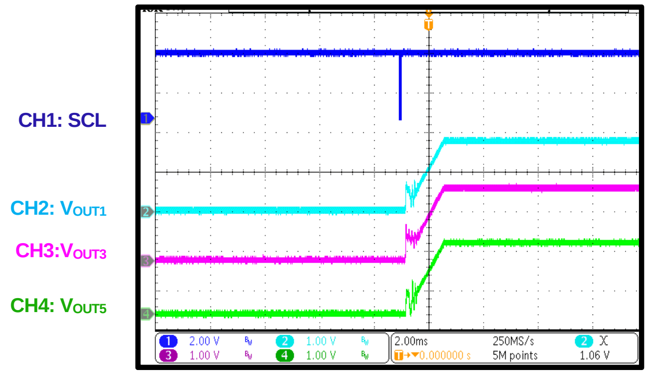
Start-Up through PMBus (Start-Up Sequence)

Bucks 2, 4, and 6, all buck rails with no load



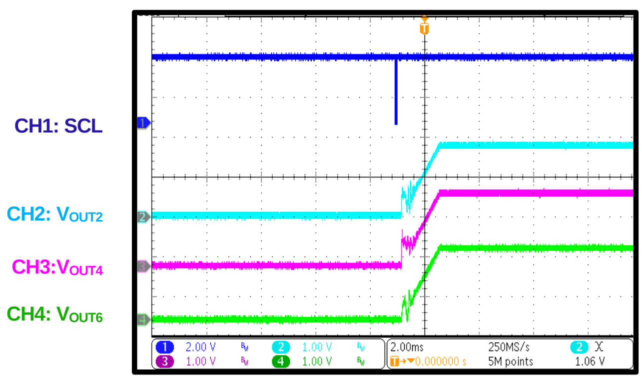
Start-Up through PMBus (Start-Up Sequence)

Bucks 1, 3, and 5, all buck rails with full load



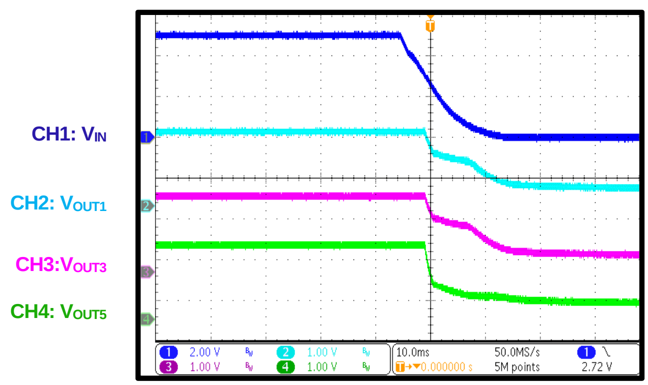
Start-Up through PMBus (Start-Up Sequence)

Bucks 2, 4, and 6, all buck rails with full load



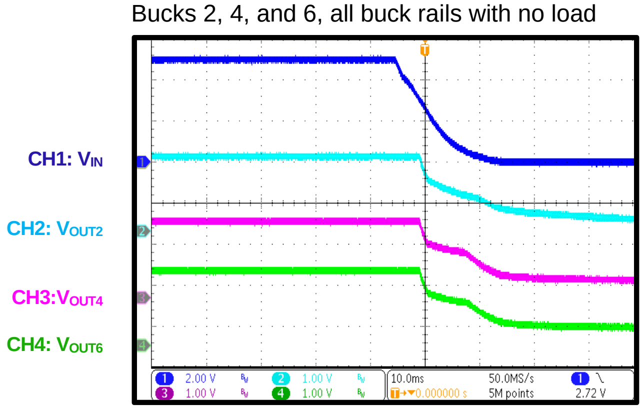
Shutdown through VIN (Shutdown Sequence)

Bucks 1, 3, and 5, all buck rails with no load



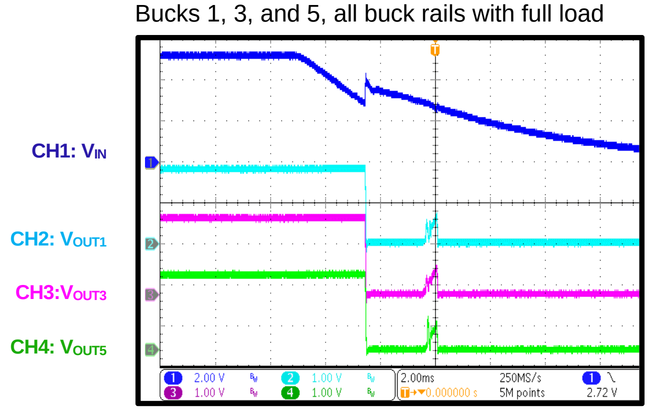
Shutdown through VIN (Shutdown Sequence)

Bucks 2, 4, and 6, all buck rails with no load



Shutdown through VIN (Shutdown Sequence)

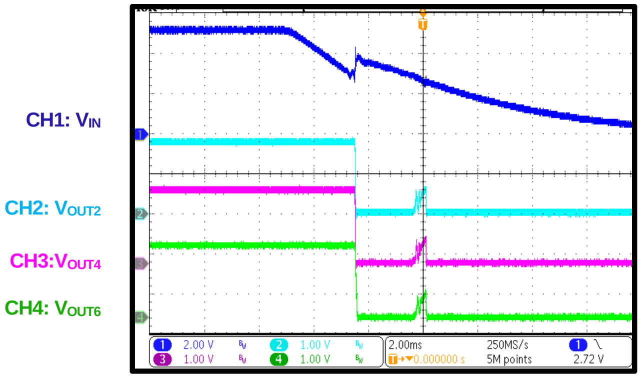
Bucks 1, 3, and 5, all buck rails with full load



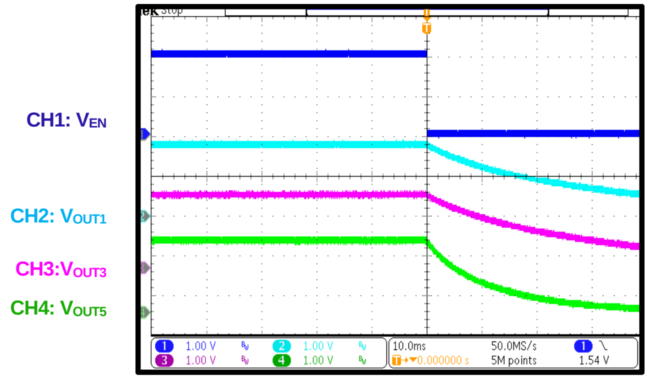
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = V_{OUT2} = V_{OUT3} = V_{OUT4} = V_{OUT5} = V_{OUT6} = 1.8V, L1 = L2 = 1.5µH, L3 = L4 = 1µH, L5 = L6 = 3.3µH, C_{OUT1} = C_{OUT2} = 2 x 22µF, C_{OUT3} = C_{OUT4} = 2 x 22µF, C_{OUT5} = C_{OUT6} = 2 x 4.7µF, f_{SW} = 2MHz, T_A = 25°C, unless otherwise noted.

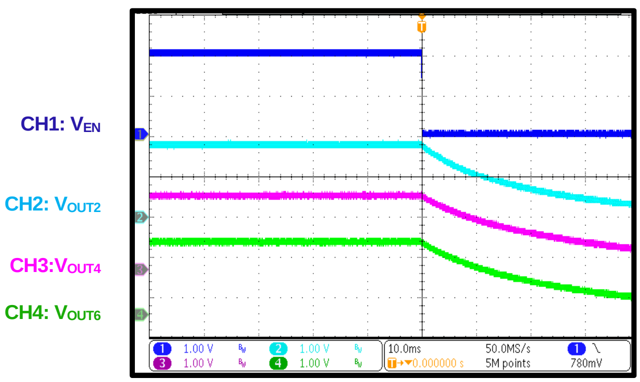
Shutdown through VIN (Shutdown Sequence)
Bucks 2, 4, and 6, all buck rails with full load



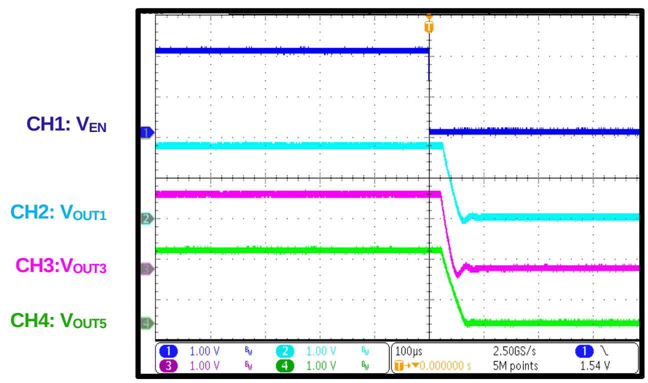
Shutdown through EN (Shutdown Sequence)
Bucks 1, 3, and 5, all buck rails with no load



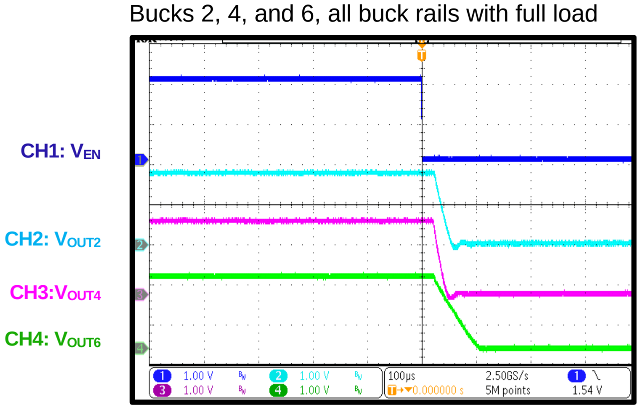
Shutdown through EN (Shutdown Sequence)
Bucks 2, 4, and 6, all buck rails with no load



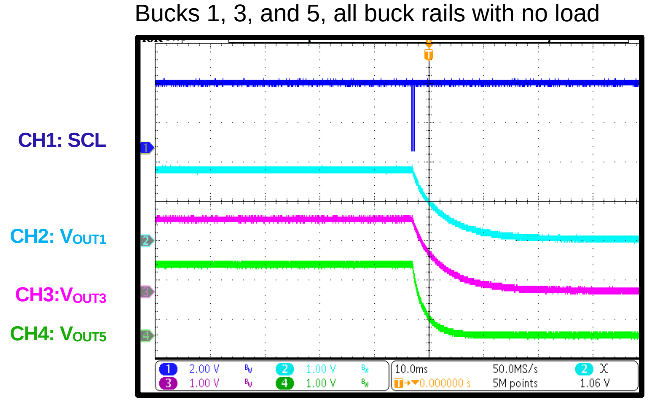
Shutdown through EN (Shutdown Sequence)
Bucks 1, 3, and 5, all buck rails with full load



Shutdown through EN (Shutdown Sequence)
Bucks 2, 4, and 6, all buck rails with full load



Shutdown through PMBus (Shutdown Sequence)
Bucks 1, 3, and 5, all buck rails with no load

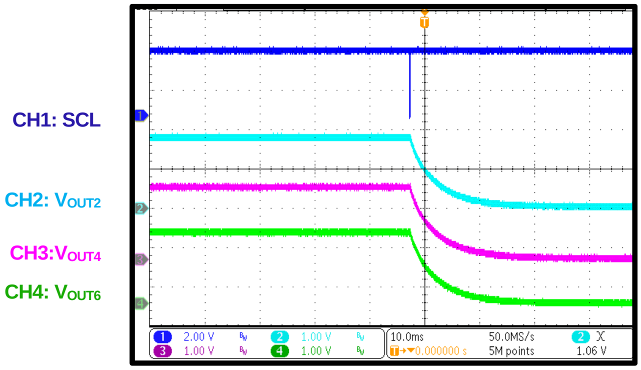


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = V_{OUT2} = V_{OUT3} = V_{OUT4} = V_{OUT5} = V_{OUT6} = 1.8V, L1 = L2 = 1.5µH, L3 = L4 = 1µH, L5 = L6 = 3.3µH, C_{OUT1} = C_{OUT2} = 2 x 22µF, C_{OUT3} = C_{OUT4} = 2 x 22µF, C_{OUT5} = C_{OUT6} = 2 x 4.7µF, f_{SW} = 2MHz, T_A = 25°C, unless otherwise noted.

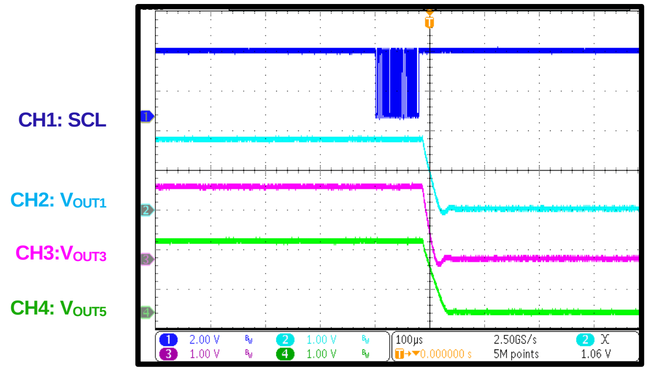
Shutdown through PMBus (Shutdown Sequence)

Bucks 2, 4, and 6, all buck rails with no load



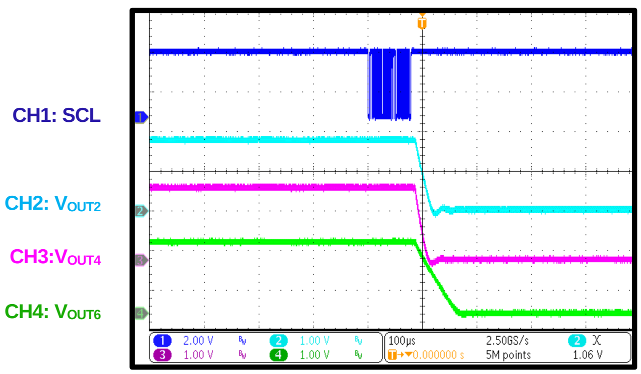
Shutdown through PMBus (Shutdown Sequence)

Bucks 1, 3, and 5, all buck rails with full load



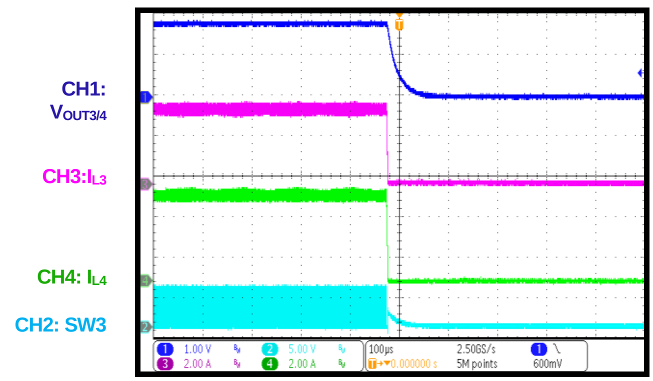
Shutdown through PMBus (Shutdown Sequence)

Bucks 2, 4, and 6, all buck rails with full load



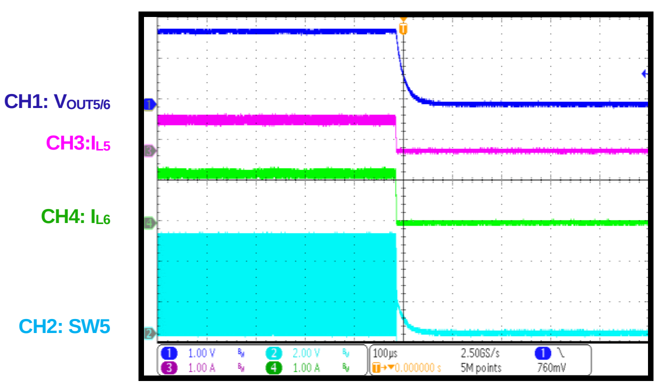
Multi-Phase PMBus Shutdown

$I_{OUT3/4}$ = 8A, other buck rails with no load



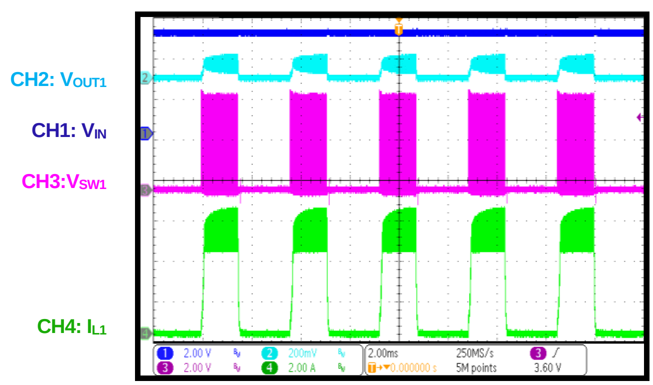
Multi-Phase Shutdown

$I_{OUT5/6}$ = 2A, other buck rails with no load



SCP Steady State

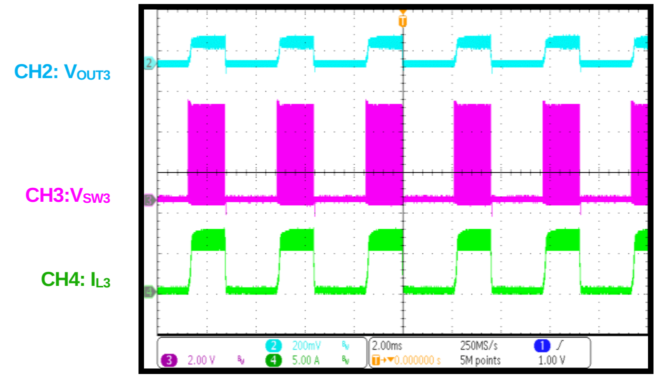
Buck 1 short circuit, all buck rails with no load



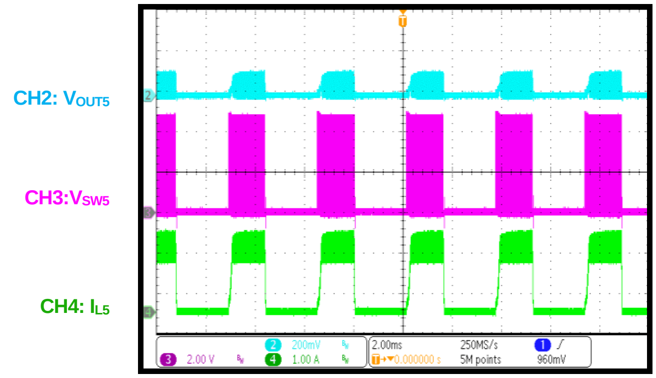
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = V_{OUT2} = V_{OUT3} = V_{OUT4} = V_{OUT5} = V_{OUT6} = 1.8V, L1 = L2 = 1.5µH, L3 = L4 = 1µH, L5 = L6 = 3.3µH, C_{OUT1} = C_{OUT2} = 2 x 22µF, C_{OUT3} = C_{OUT4} = 2 x 22µF, C_{OUT5} = C_{OUT6} = 2 x 4.7µF, f_{SW} = 2MHz, T_A = 25°C, unless otherwise noted.

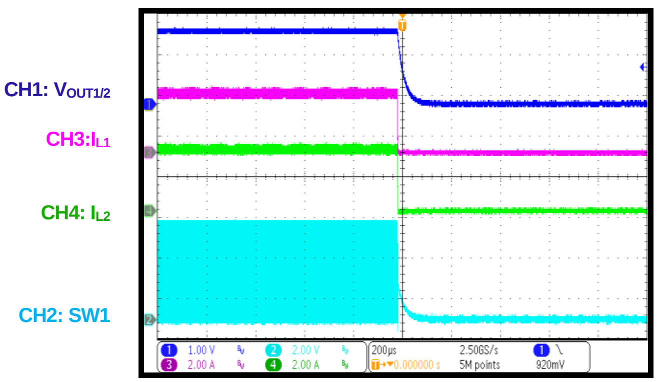
SCP Steady State
Buck 3 short circuit, all buck rails with no load



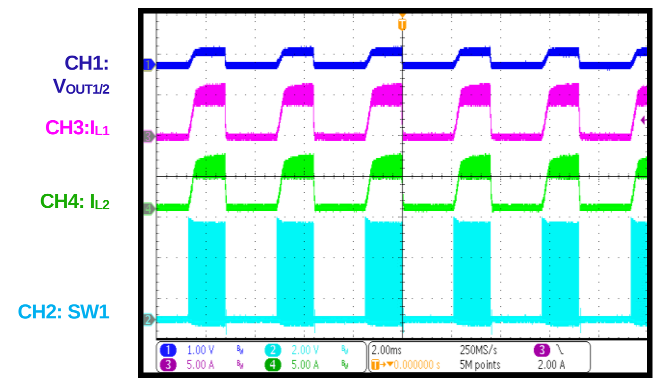
SCP Steady State
Buck 5 short circuit, all buck rails with no load



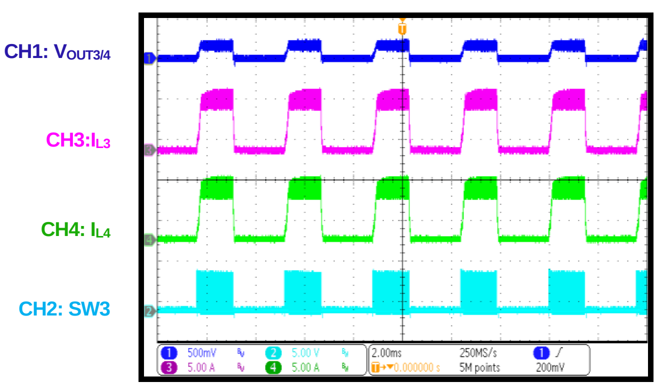
Multi-Phase PMBus Shutdown
$I_{OUT1/2}$ = 6A, other buck rails with no load



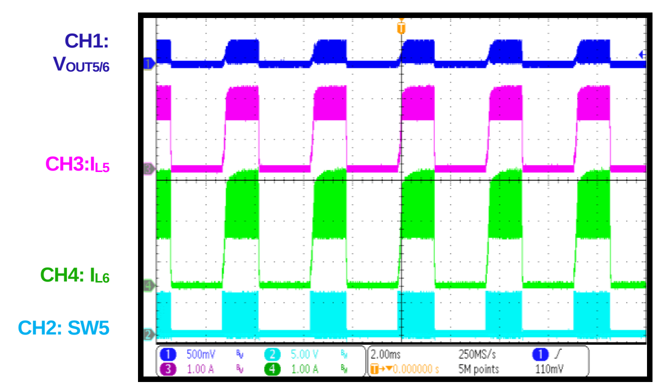
Multi-Phase SCP Steady State
Buck 1/2 short circuit, other buck rails with no load



Multi-Phase SCP Steady State
Buck 3/4 short circuit, other buck rails with no load



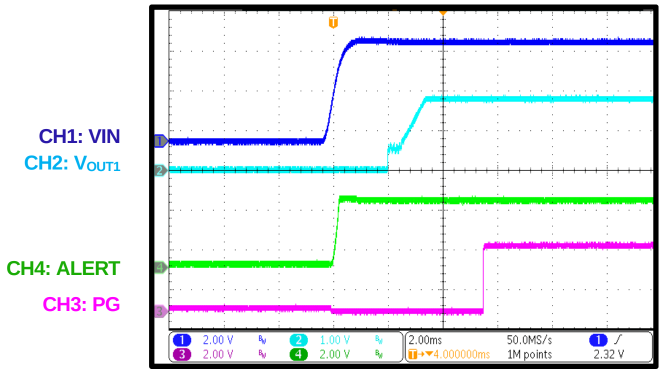
Multi-Phase SCP Steady State
Buck 5/6 short circuit, other buck rails with no load



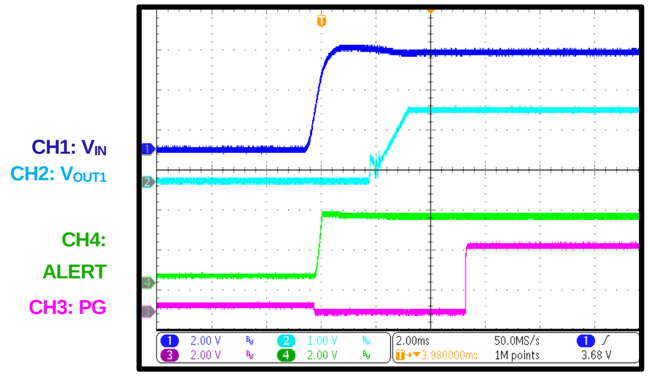
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = V_{OUT2} = V_{OUT3} = V_{OUT4} = V_{OUT5} = V_{OUT6} = 1.8V, L1 = L2 = 1.5µH, L3 = L4 = 1µH, L5 = L6 = 3.3µH, C_{OUT1} = C_{OUT2} = 2 x 22µF, C_{OUT3} = C_{OUT4} = 2 x 22µF, C_{OUT5} = C_{OUT6} = 2 x 4.7µF, f_{SW} = 2MHz, T_A = 25°C, unless otherwise noted.

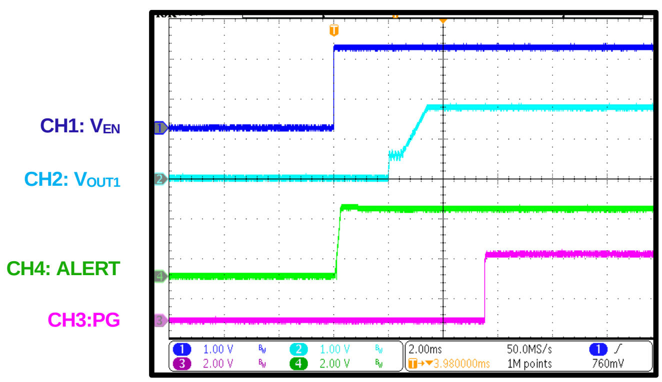
PG and ALERT during Start-Up through VIN
All buck rails with no load



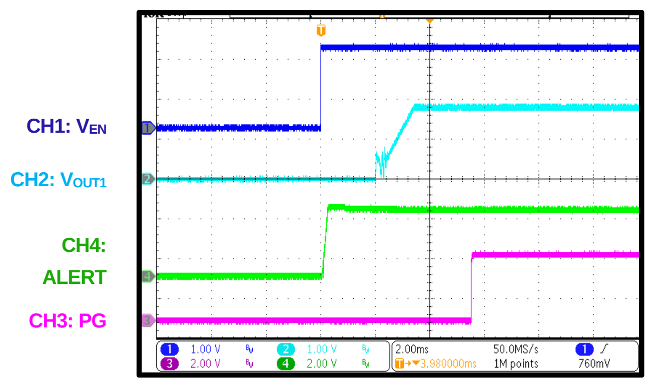
PG and ALERT during Start-Up through VIN
All buck rails with full load



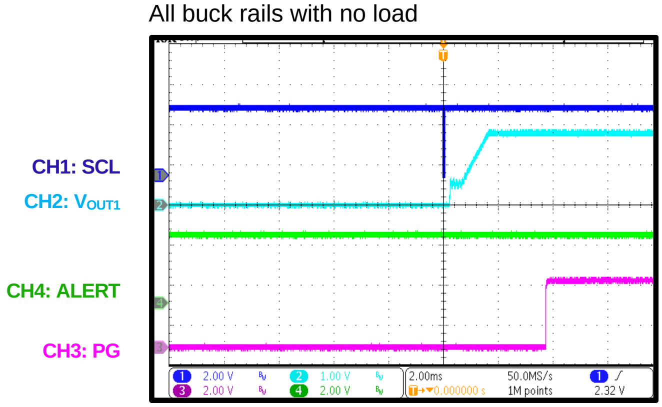
PG and ALERT during Start-Up through EN
All buck rails with no load



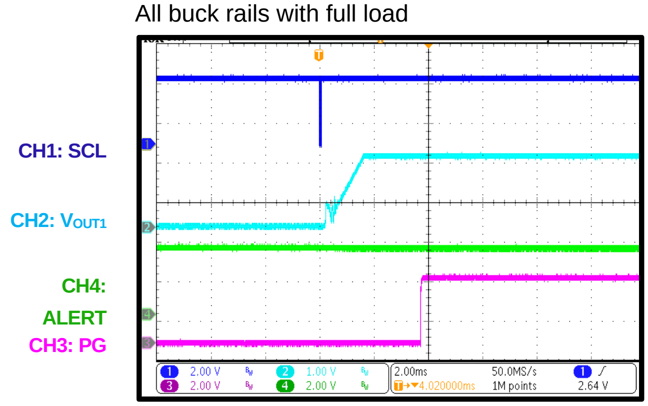
PG and ALERT during Start-Up through EN
All buck rails with full load



PG and ALERT during Start-Up through PMBus
All buck rails with no load



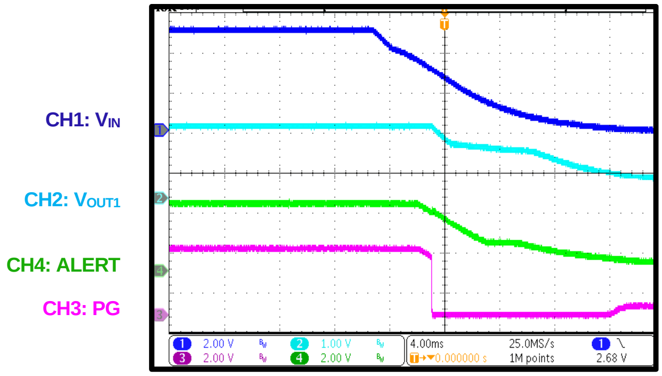
PG and ALERT during Start-Up through PMBus
All buck rails with full load



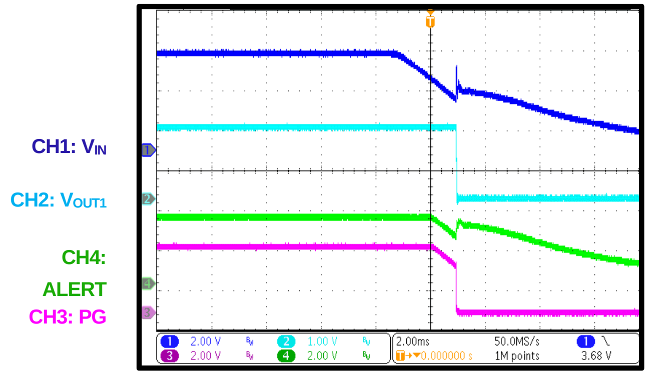
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = V_{OUT2} = V_{OUT3} = V_{OUT4} = V_{OUT5} = V_{OUT6} = 1.8V, L1 = L2 = 1.5µH, L3 = L4 = 1µH, L5 = L6 = 3.3µH, C_{OUT1} = C_{OUT2} = 2 x 22µF, C_{OUT3} = C_{OUT4} = 2 x 22µF, C_{OUT5} = C_{OUT6} = 2 x 4.7µF, f_{SW} = 2MHz, T_A = 25°C, unless otherwise noted.

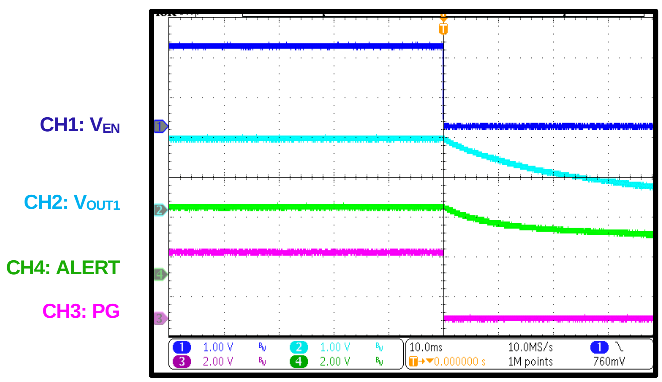
PG and ALERT during Shutdown through VIN
All buck rails with no load



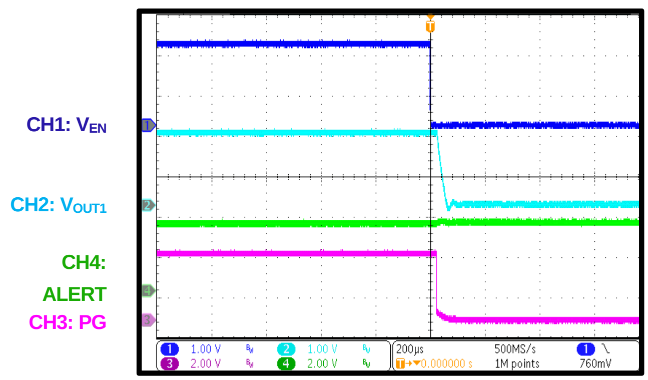
PG and ALERT during Shutdown through VIN
All buck rails with full load



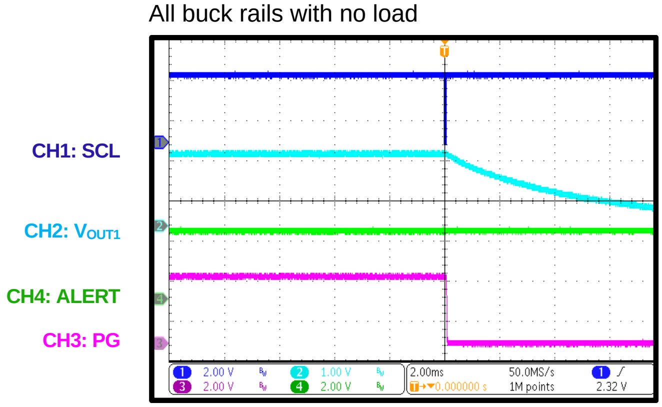
PG and ALERT during Shutdown through EN
All buck rails with no load



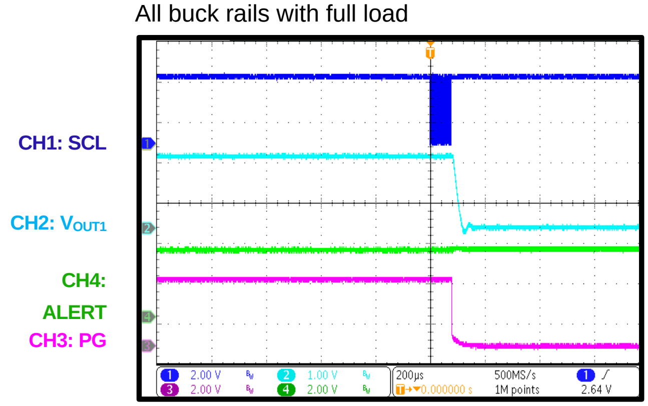
PG and ALERT during Shutdown through EN
All buck rails with full load



PG and ALERT during Shutdown through PMBus
All buck rails with no load



PG and ALERT during Shutdown through PMBus
All buck rails with full load

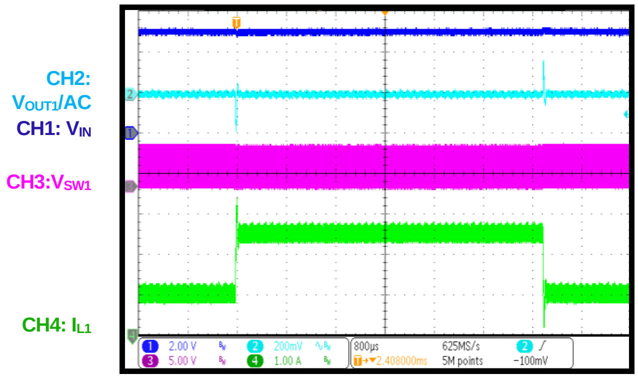


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = V_{OUT2} = V_{OUT3} = V_{OUT4} = V_{OUT5} = V_{OUT6} = 1.8V, L1 = L2 = 1.5µH, L3 = L4 = 1µH, L5 = L6 = 3.3µH, C_{OUT1} = C_{OUT2} = 2 x 22µF, C_{OUT3} = C_{OUT4} = 2 x 22µF, C_{OUT5} = C_{OUT6} = 2 x 4.7µF, f_{SW} = 2MHz, T_A = 25°C, unless otherwise noted.

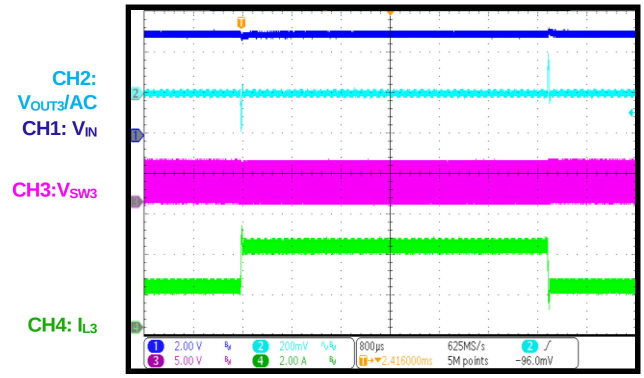
Load Transient Response

I_{OUT1} transient from 1.5A to 3A, slew rate is 2A/µs



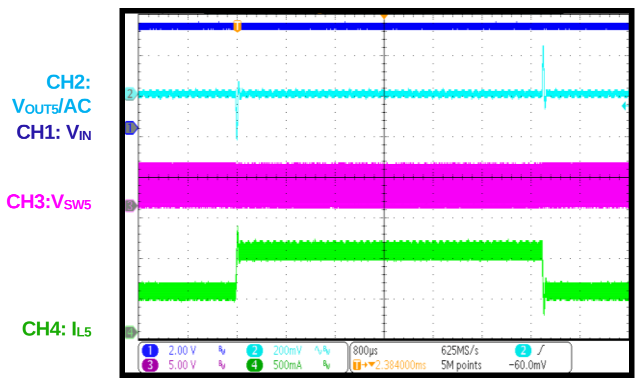
Load Transient Response

I_{OUT3} transient from 2A to 4A, slew rate is 2A/µs



Load Transient Response

I_{OUT5} transient from 0.5A to 1.0A, slew rate is 2.0A/µs



FUNCTIONAL BLOCK DIAGRAM

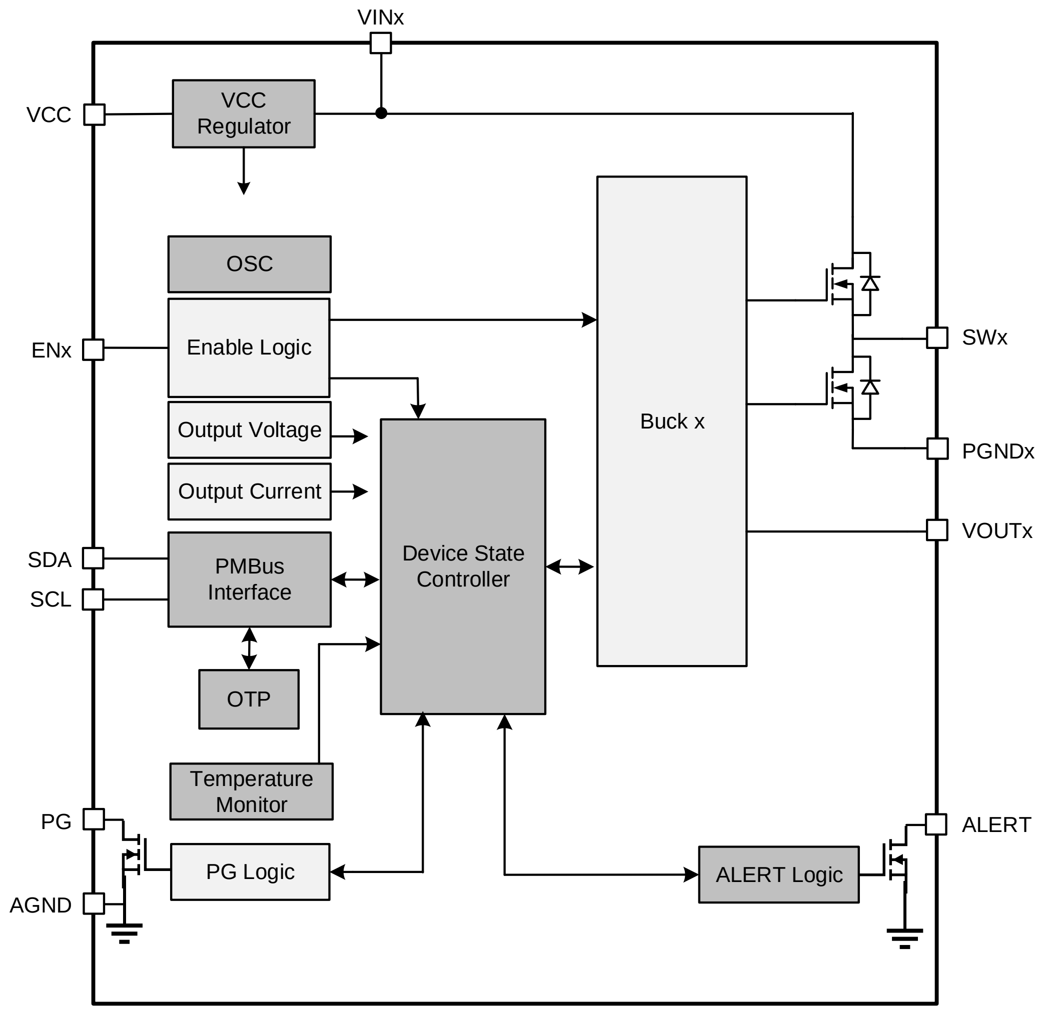


Figure 2: Functional Block Diagram

START-UP BEHAVIOR

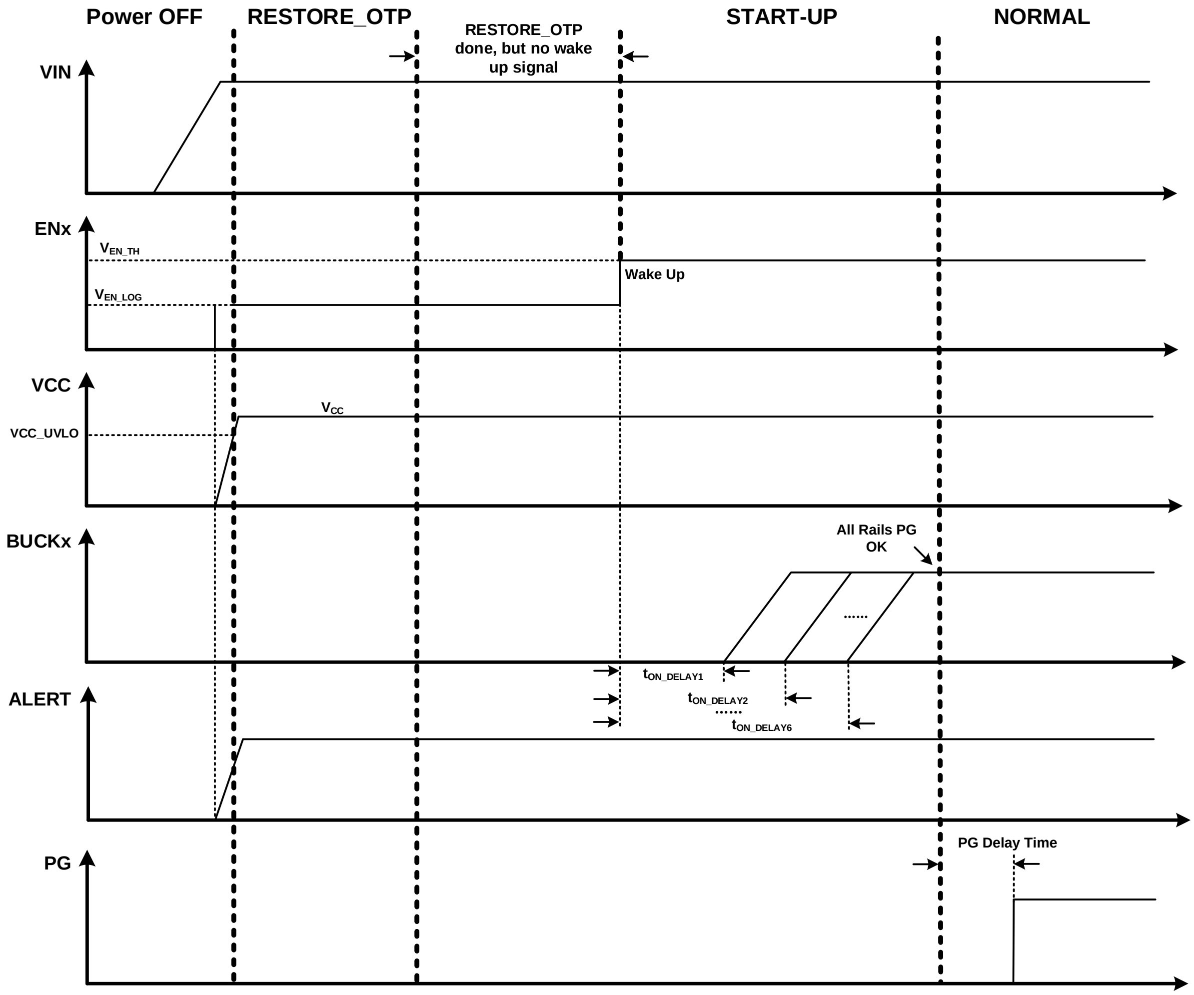


Figure 3: Start-Up Behavior

OPERATION

The MPQ7930 is a highly flexible power solution for advanced driver assistance systems (ADAS) and system-on-chip (SoCs). It integrates six high-frequency, synchronous, rectified step-down converters. The PMBus and multi-page one-time programmable (OTP) memory allow for significant configurations to meet the requirements of the target SoC.

High-Efficiency Buck Regulators

Bucks 1–6 are synchronous, step-down DC/DC converters with built-in under-voltage lockout (UVLO), soft start, compensation, and hiccup current limit protection. Fixed-frequency peak current control provides fast transient response and a stable frequency. The switching clock phase shifts from buck 1–6 during continuous conduction mode (CCM).

Multi-Phase Operation

Multi-phase operation is available and can be configured via the OTP. Any changes that are made are updated after the device restarts. The multi-phase pairs are buck 1 and buck 2, buck 3 and buck 4, then buck 5 and buck 6. If two bucks operate in parallel, the configuration page for the lower-numbered buck is used.

Light-Load Operation

The MPQ7930 can support forced continuous conduction mode (FCCM).

FCCM allows the inductor current to reach negative values up to the negative current limit. FCCM provides the best transient response and frequency performance. The advantages of FCCM are its controllable frequency, lower output ripple, and smaller peak inductor current under light loads.

Dynamic Voltage Scaling

The output voltage (V_{OUT}) can be changed via the PMBus during normal operation. When the voltage changes, the slope is determined by the VOUT_SLEW register.

If users regulate VOUT_CMD to exceed VOUT_MAX or VOUT_MIN via the VOUT_COMMAND register, V_{OUT} is limited to its maximum (V_{OUT_MAX}) or minimum (V_{OUT_MIN}). This protection mechanism can prevent abnormal system operation due to writing an incorrect value for VOUT_COMMAND. The values for V_{OUT_MAX} and V_{OUT_MIN} are determined by the VOUT_MAX and VOUT_MIN commands. If V_{OUT} changes due to external reasons, VOUT_MAX and VOUT_MIN do not protect from these changes.

V_{IN} and V_{CC} Under-Voltage Lockout (UVLO)

Input under-voltage lockout (UVLO) is derived from VIN (pin 23). If V_{IN} falls below V_{IN_UVLO} and V_{CC} exceeds V_{CC_UVLO}, the MPQ7930 enters the restore OTP state with no output. During this time, PMBus communication operates normally. If V_{CC} falls below V_{CC_UVLO}, the MPQ7930 enters the power off state, and PMBus communication is unavailable.

Power Sequencing

The MPQ7930 provides six enable pins (ENx), and each output is controlled by a separate pin. Typically, power sequencing is controlled externally, but each output can be further delayed. For each buck, the delay time can be independent and freely configured via the TON_DELAY register. TON_DELAY sets the time from when the EN level exceeds EN_RISING_THRESHOLD and when V_{OUT} starts to rise after the completion of RESORE_OTP.

Figure 4 shows the sequencing diagram. EN1 can be replaced by any ENx pin.

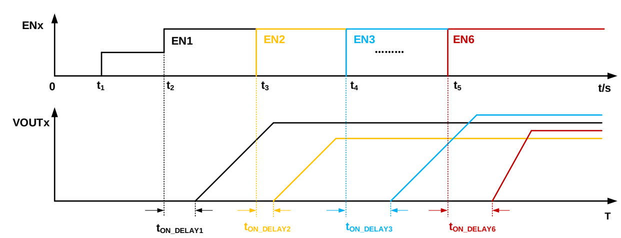


Figure 4: Sequencing Diagram

Internal Soft Start

The soft-start function is implemented to prevent the PMIC's V_{OUT} from overshooting during start-up. When the MPQ7930 starts up, the internal circuitry of each power rail generates a soft-start voltage that ramps up from 0V. During soft start, an initial step can be observed on the output voltage.

The soft-start period lasts until the voltage on the soft-start capacitor exceeds the reference voltage (V_{REF}). At this point, V_{REF} takes over. The soft start slew rate of each output can be configured via the OTP.

During soft start, an initial step can be observed on the output voltage.

Output Discharge

The MPQ7930 provide a 100Ω discharge resistor for each output. The discharge resistor is between the VOUTx pin and AGND. The resistor is connected to a discharge circuit only when the shutdown signal is enabled. The energy on the output capacitor is discharged through the 100Ω resistor. During normal operation, the discharge resistor is disconnected.

Power Good (PG) and ALERT Indicators

PG and ALERT are open-drain outputs. PG asserts if the voltage is not within the PG range. The PG range of each buck can be configured via the PG_CONFIG register.

The ALERT pin asserts to indicate issues with the device's status (see Table 1). By default, over-voltage protection (OVP), under-voltage protection (UVP), thermal warning, thermal shutdown, packet error checking (PEC) errors, and communications errors can assert the ALERT flag. The ALERT flag remains asserted until the relevant fault and status register are cleared. Some of faults can also be masked. CLEAR_FAULTS clears any fault bit in all status registers.

When PG and ALERT de-assert, the MPQ7930 provides a variety of delay time options (0ms, 2ms, 5ms, and 10ms) via the PG_ALERT_DELAY register.

Table 1: PG and ALERT Response for Different Fault Types

Fault Type	PG Assert?	ALERT Assert?
Thermal shutdown	Yes	Yes
Thermal warning	Yes	Yes
PMBus CRC error	Yes	Yes
PMBus communication error	Yes	Yes
Busy	Yes	Yes
Force PG assertion by register	Yes	No
Force ALERT assertion by register	No	Yes
VOUT_MAX/MIN register warning	Yes	Yes
OVP	Yes	Yes
UVP	Yes	Yes
PG threshold (OV)	Yes	No
PG threshold (UV)	Yes	No

Output Over-Voltage Protection (OVP)

If an output exceeds the OVP threshold, that output shuts off for the hiccup time, then the normal start-up sequence starts again. If enabled, the output discharge function works throughout the hiccup time.

Output Under-Voltage Protection (UVP)

If an output falls below the UVP threshold, that output shuts off for a hiccup time, then the normal start-up sequence starts again. If enabled, the output discharge function works throughout the hiccup time.

Compensation

The MPQ7930 integrates internal compensation for each buck output. The compensation can be adjusted via the OTP. If changes are made to the OTP values, these changes are made after the output is disabled then enabled again.

Figure 5 on page 33 shows a typical Type II compensation network that is fully integrated in the chip. The components' values can be configured via the PMBus.

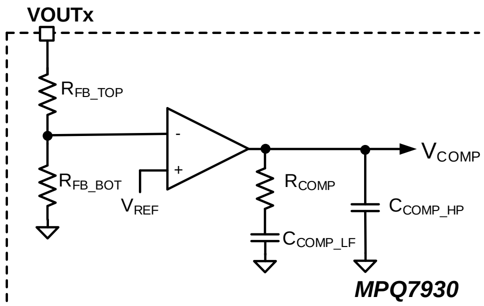


Figure 5: Compensation Network

Frequency Spread Spectrum (FSS)

Frequency spread spectrum (FSS) modulates the clock frequency with a triangle wave. The modulation range is typically 15%, and the frequency is 9kHz. This can be enabled or disabled via the PMBus. When FSS is enabled, the operating frequency drops from 2MHz to its minimum value, and then the operating frequency slowly increases. After reaching the maximum value, it slowly decreases again. When FSS is disabled, the operating frequency changes from its current value to 2MHz.

If the output voltage of any channel is below 0.8V, it is recommended to disable FSS. This reduces the output voltage ripple impact on PG, as caused by FSS.

Thermal Warning and Shutdown

Thermal warning is indicated by asserting a bit in the thermal warning register and asserting the PG and ALERT pins. All rails can operate normally when the device triggers thermal warning, but not thermal shutdown.

Thermal shutdown disables the device until the temperature drops below the hysteresis point. PG and ALERT also assert in thermal shutdown.

PMBUS INTERFACE

PMBus Serial Interface Description

The power management bus (PMBus) is an open standard, power management protocol that defines a means of communication with power conversion and other devices. The PMBus is a two-wire, bidirectional serial interface, consisting of a serial data line (SDA) and a serial clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. Connecting to the line, a master device generates the SCL signal and device address, then arranges the communication sequence.

The MPQ7930 works as a slave-only device that supports both the standard mode (100kb/s) and fast mode (400kb/s) bidirectional data transfer, adding flexibility to the power supply solution. The output voltage, transition slew rate, and other converter parameters can be instantaneously controlled by the PMBus interface.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the SDA line can only change when the clock signal on the SCL line is low (see Figure 6).

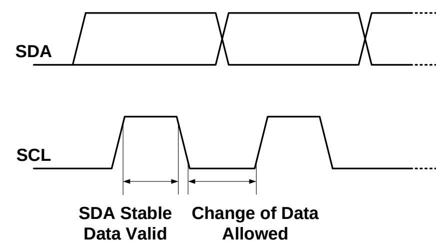


Figure 6: Bit Transfer on the PMBus

Start and Stop Commands

The start and stop commands are signaled by the master device, which signifies the beginning and the end of the PMBus transfer. The start command (S) is defined as the SDA signal transitioning from high to low while the SCL line is high. The stop command (P) is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 7).

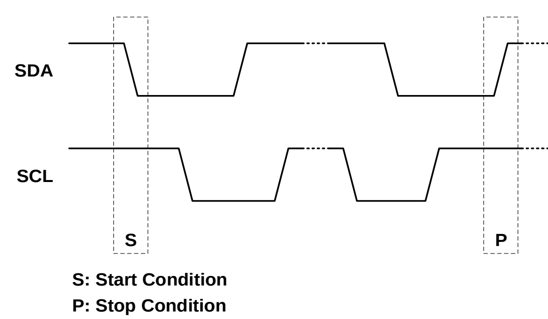


Figure 7: Start and Stop Commands

Start and stop commands are always generated by the master. The bus is considered busy after the start condition. The bus is considered free again after a certain time after the stop condition. The bus stays busy if a repeated start (Sr) is generated instead of a stop command. The start and repeated start commands are functionally identical.

Transfer Data

Every byte put on the SDA line must be 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse, so that it remains stable low during the high period of the clock pulse.

Figure 8 on page 34 shows the data transfer format. After the start command, a slave address is sent. This address is 7 bits long, followed by an eighth data direction bit (R/W). A 0 indicates a transmission (write), while a 1 indicates a request for data (read). A data transfer is always terminated by a stop command, which is generated by the master. However, if the master wants to continue to communicate on the bus, it can generate a repeated start command and address another slave without first generating a stop command.

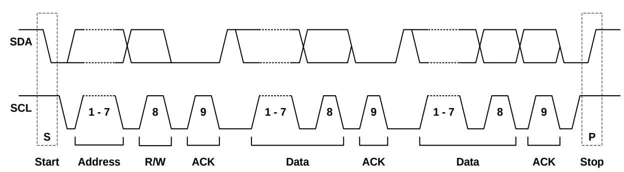


Figure 8: A Complete Data Transfer

Packet Error Checking (PEC)

The packet error checking (PEC) mechanism is employed to improve communication reliability and robustness. Whenever applicable, PEC is implemented by appending a packet error code after the data of each message transfer.

The PEC is a CRC-8 error-checking byte, calculated on all the message bytes (including addresses and read/write bits). The PEC is appended to the message by the device that supplied the last data byte.

If an incorrect PEC is received, a communications fault is triggered, and the PG flag and ALERT flag assert. The PG flag de-asserts after the PG_DELAY time. The ALERT de-asserts when the relevant fault register is cleared.

PMBus Communication Failure

A data transmission fault occurs when the data is not properly transferred between the devices. There are several data transmission faults, listed below:

- Sending too little data
- Reading too little data
- The host sends too many bytes
- The host reads too many bytes
- Improperly set read bit in the address byte
- Unsupported command code

The communication failure is recorded in the register STATUS_CML.

Write/Read Sequence

All PMBus commands are supported by the MPQ7930, following the write/read sequence (see Figure 9 on page 35 and Figure 10 on page 35). Five commands can be implemented with or without PEC:

1. Send command only
2. Write byte
3. Write word
4. Read byte
5. Read word

If the master writes a command to a read-only register, the MPQ7930 performs the same action as if the host has sent too many bytes. If the master reads a command from a write-only register, the MPQ7930 performs the same action as the host would if it read too many bytes.

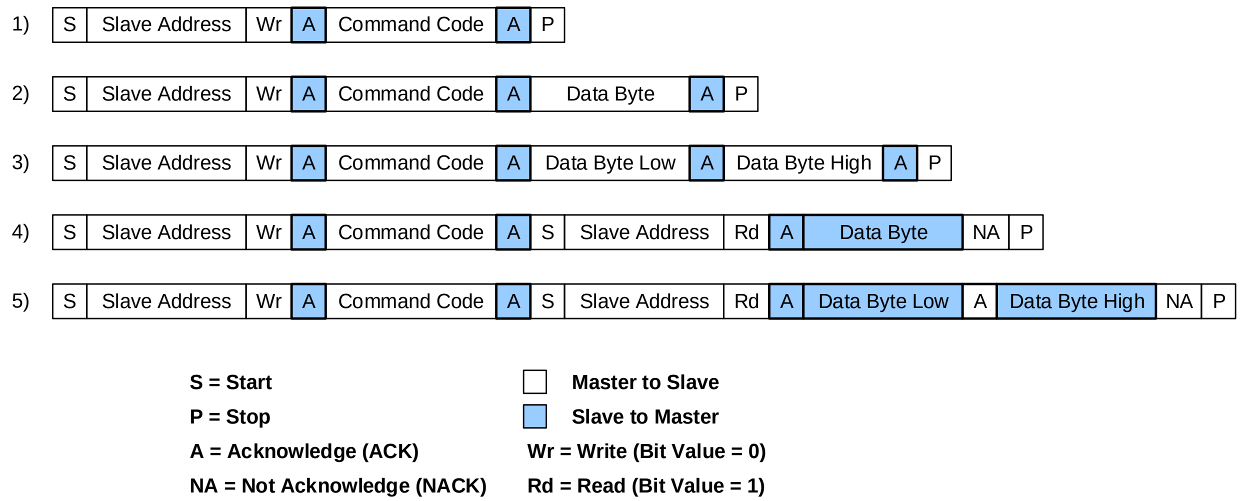


Figure 9: PMBus Write/Read Sequence without PEC

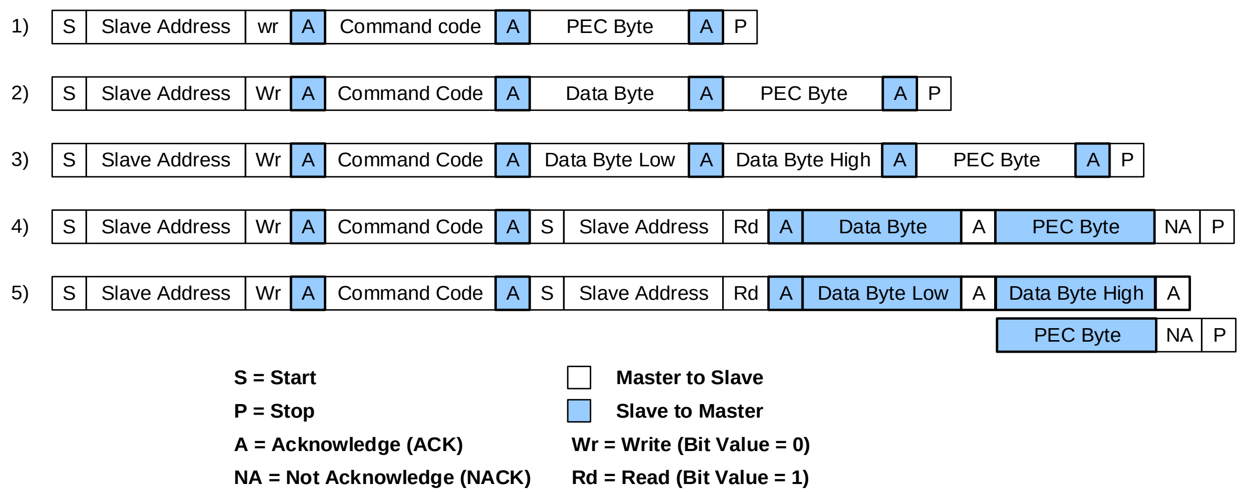


Figure 10: PMBus Write/Read Sequence with PEC

STATE MACHINE DESCRIPTION

The state machine describes the different states of operation. The device has 6 states: power off (POWER OFF), restore OTP (RESTORE_OTP), start-up (STARTUP), normal (NORMAL), store user (STORE_USER), and restore user (RESTORE_USER).

Figure 11 shows the state diagram. Each state is described in greater detail below.

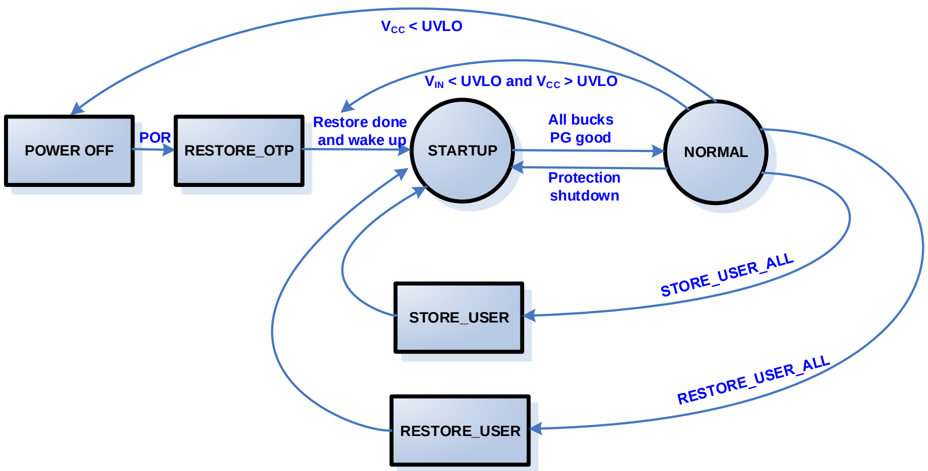


Figure 11: System State Machine

Power Off State (POWER OFF)

The MPQ7930 is in the power off state if V_{CC} is below its UVLO threshold. All functions are disabled in this state.

Restore OTP State (RESTORE_OTP)

When V_{CC} exceeds its rising UVLO threshold, the MPQ7930 enters the restore OTP state and begins to restore registers from the embedded OTP content data.

Start-Up State (STARTUP)

After OTP is complete, and the wake-up signal is enabled, the device enters the start-up state. If the wake-up signal is enabled during RESTORE_OTP, the MPQ7930 automatically enters the start-up state once the OTP is done being restored. In the start-up state, the other supplies are enabled and start to ramp up.

Normal State (NORMAL)

The MPQ7930 enters the normal state as soon as every output regulator voltage is detected to have a power good status. The normal state is the standard operating state for the MPQ7930, during which all relevant output regulators are up and running.

Store User State (STORE_USER)

The store user state writes the present data from the registers to the internal OTP content. Then the MPQ7930 transitions to the start-up state and restarts. Write to the STORE_USER_ALL register while in the normal state to trigger the store user state. See the STORE_USER_ALL (15h) section on page 39 for more details.

Restore User State (RESTORE_USER)

The restore user state copies the entire contents of the OTP values to the matching locations in the registers. The values in the registers are overwritten by the value retrieved from the OTP. Any items in the OTP that do not have matching locations in the operating memory are ignored. Then the MPQ7930 transitions to the start-up state and restarts. Write to the RESTORE_USER_ALL register while in the normal state to enter the restore user state. See the RESTORE_USER_ALL (15h) section on page 39 for more details.

REGISTER MAP

Addr.	Name	R/W	Bytes	Pages	OTP?	Default	Lockout?
00h	PAGE	R/W	1	No	No	FFh	N
01h	OPERATION	R/W	1	Yes	Yes	Pages 00–05: 80h	Yes
03h	CLEAR_FAULTS	W	0	No	No	-	No
10h	WRITE_PROTECT	R/W	1	No	No	00h	No
15h	STORE_USER_ALL	W	0	No	No	-	Yes
16h	RESTORE_USER_ALL	W	0	No	No	-	Yes
19h	CAPABILITY	R	1	No	No	C0h	-
20h	VOUT_MODE	R	1	No	No	40h	-
21h	VOUT_COMMAND	R/W	1	Yes	Yes	Pages 00–05: FFh	No
24h	VOUT_MAX	R/W	1	Yes	Yes	Pages 00–05: FFh	Yes
29h	VOUT_SCALE_LOOP	R/W	1	Yes	Yes	Pages 00–05: 00h	Yes
2Bh	VOUT_MIN	R/W	1	Yes	Yes	Pages 00–05: 00h	Yes
60h	TON_DELAY	R/W	1	Yes	Yes	Pages 00–05: 00h	Yes
64h	TOFF_DELAY	R/W	1	Yes	Yes	Pages 00–05: 00h	Yes
78h	STATUS_BYTE	R	1	Yes	No	-	No
79h	STATUS_WORD	R	2	Yes	No	-	No
7Ah	STATUS_VOUT	R	1	Yes	No	-	No
7Dh	STATUS_TEMPERATURE	R	1	No	No	-	No
7Eh	STATUS_CML	R	1	No	No	-	No
9Dh	SECURE_LOCKOUT	R/W	1	No	No	00h	Yes
9Eh	MULTIPHASE_CONFIG	R/W	1	No	Yes	00h	Yes
A0h	HICCUP_TIMER	R/W	1	No	Yes	00h	Yes
A1h	STATUS_PIN_STATE	R	1	No	No	-	-
A3h	VOUT_STARTUP_SLEW	R/W	1	Yes	Yes	Pages 00–05: 00h	Yes
A5h	VOUT_SHUTDOWN_SLEW	R/W	1	Yes	Yes	Pages 00–05: 00h	Yes
A7h	VOUT_SLEW	R/W	1	Yes	Yes	Pages 00–05: 00h	Yes
A9h	OUTPUT_DISCHARGE	R/W	1	Yes	Yes	Pages 0–5: 01h	Yes
ADh	FREQUENCY_DITHER	R/W	1	No	Yes	01h	Yes
B0h	COMPENSATION_CONFIG_1	R/W	1	Yes	Yes	Pages 00–05: 83h	Yes
B1h	COMPENSATION_CONFIG_2	R/W	1	Yes	Yes	Pages 00–05: 12h	Yes
C0h	ALERT_PG_FORCE_ASSERT	R/W	1	No	No	00h	No
C2h	PROTECTION_CONFIG	R/W	1	No	Yes	1Ch	Yes
C4h	ALERT_MAPPING	R/W	1	No	Yes	00h	Yes
C6h	PG_MAPPING	R/W	1	No	Yes	00h	Yes
C8h	PG_ALERT_DELAY	R/W	1	No	Yes	05h	Yes
CAh	PG_CONFIG	R/W	1	Yes	Yes	Pages 00–05: 00h	Yes
CCh	LIGHT_LOAD	R/W	1	No	Yes	01h	Yes
CEh	ILIM_SCALE	R/W	1	Yes	Yes	Pages 00–05: 00h	Yes
D5h	ADDRESS	R/W	1	No	Yes	03h	Yes
D6h	CONFIG_CODE	R	1	No	Yes	00h	-
DBh	MFR_OTP_MEM_STATUS	R	1	No	No	-	-

REGISTER DESCRIPTION

PAGE (00h)

The PAGE command provides the ability to configure, control, and monitor all outputs through only one physical address. All subsequent commands that allow for multi-page action (denoted as “Yes” in the Pages column in the Register Map section on page 37) are applied to the corresponding regulator(s) selected by the PAGE command.

Command	PAGE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	PAGE							

Bits	Bit Name	Description
7:0	PAGE	0x00: VOUT1 0x01: VOUT2 0x02: VOUT3 0x03: VOUT4 0x04: VOUT5 0x05: VOUT6 0x06~ 0xFE: Not supported 0xFF: All

OPERATION (01h)

The OPERATION command configures the converter output’s on/off state, in conjunction with the input from the ENx pin.

Command	OPERATION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	OPERATION	RESERVED						

Bits	Bit Name	Description
7	OPERATION	1: Output on (if enabled high) 0: Output off
6:0	RESERVED	Reserved.

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command clears any fault bit in the following status registers: STATUS_BYTE (78h), STATUS_WORD (79h), STATUS_VOUT (7Ah), STATUS_TEMPERATURE (7Dh), and STATUS_CML (7Eh)

This command is write-only. There is no data byte for this command.

WRITE_PROTECT (10h)

The WRITE_PROTECT command controls writing to the converter. The intent of this command is to provide protection against accident changes. It is not intended to provide protection against deliberate changes to the converter's configuration or operation. All the supported commands may have their parameters read, regardless of the WRITE_PROTECT settings.

Command	WRITE_PROTECT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	WRITE_PROTECT							

Bits	Bit Name	Description
7:0	WRITE_PROTECT	10000000: Disable all writes, except to the WRITE_PROTECT command 01000000: Disable all writes, except to the WRITE_PROTECT, OPERATION, and PAGE commands 00100000: Disable all writes except to the WRITE_PROTECT, OPERATION, PAGE, and VOUT_COMMAND commands 00000000: Enable writes to all commands

STORE_USER_ALL (15h)

The STORE_USER_ALL command instructs the MPQ7930 to copy the contents of the operating memory to the matching locations in the OTP, except for the internal trim registers. This process begins when MPQ7930 receives a STORE_USER_ALL command from the PMBus interface. This process can only be performed while the device is in its normal state.

This command is write-only. There is no data byte for this command.

RESTORE_USER_ALL (16h)

The RESTORE_USER_ALL command instructs the MPQ7930 to copy the contents from the OTP and overwrite the matching locations in the operating memory. Trim registers are not overwritten by this process. Any items in the OTP that do not have matching locations in the operating memory are ignored.

The RESTORE_USER_ALL command can be used while the MPQ7930 is operating. However, the MPQ7930 may be unresponsive during this operation with unpredictable or even catastrophic results.

This command is write-only. There is no data byte for this command.

CAPABILITY (19h)

The CAPABILITY command provides 1 byte to return key PMBus features that the MPQ7930 can support.

Command	CAPABILITY							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function		MAX_BUS_SPEED					RESERVED	

Bits	Bit Name	Description
7	PACKET_ERR_CHECKING	1: Packet error checking (PEC) is supported
6:5	MAX_BUS_SPEED	10: The maximum supported bus speed is 1MHz
4	SMBALERT	0: The device does not have a SMBALERT pin, and it does not support the SMBus Alert Response protocol

3	NUMERIC_FORMAT	0: The numeric data is in Linear11, ULinear16, SLinear16, or direct format
2	AVSBUS_SUPPORT	0: AVSBus is not supported
1:0	RESERVED	Reserved.

VOUT_MODE (20h)

The VOUT_MODE command commands and reads the output voltage mode. The 3MSB determine the data format. The MPQ7930 only supports direct format.

Command	VOUT_MODE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	VOUT_MODE							

Bits	Bit Name	Description
7:0	VOUT_MODE	01000000: Direct mode. The coefficients are m = 160, R = 0, and b = -33

VOUT_COMMAND (21h)

The VOUT_COMMAND command sets V_{OUT}.

Command	VOUT_COMMAND							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	VOUT_CMD							

Bits	Bit Name	Description
7:0	VOUT_CMD	V_{OUT} can be set between 0.20625V and 1.8V, and it can be calculated with the following equation: V_{OUT} = (VOUT_CMD x 6.25mV + 206.25mV) x VOUT_SL

VOUT_MAX (24h)

The VOUT_MAX command sets an upper limit on the converter's commanded output voltage, regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level. It is not the primary output over-voltage protection (OVP).

Command	VOUT_MAX							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	VOUT_MAX							

Bits	Bit Name	Description
7:0	VOUT_MAX	Sets the maximum V_{OUT}, which is between 0.20625V and 1.8V. The maximum V_{OUT} can be calculated with the following equation: V_{OUT_MAX} = (VOUT_MAX x 6.25mV + 206.25mV) x VOUT_SL Attempting to write a higher value to VOUT_COMMAND causes VOUT_COMMAND to be set to VOUT_MAX, and asserts a VOUT_MAX_MIN warning.

VOUT_SCALE_LOOP (29h)

The VOUT_SCALE_LOOP command sets the V_{OUT} scale.

Command	VOUT_SCALE_LOOP							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function		VOUT_SC_L						

Bits	Bit Name	Description
7:1	RESERVED	Reserved.
0	VOUT_SC_L	Sets the V_{OUT} scale. Direct mode. The coefficients are m = 1, R = 0, and b = -1. 0: VOUT_SL = 1 1: VOUT_SL = 2 Changes to this bit require that the device be turned off then on with the OPERATION command.

VOUT_MIN (2Bh)

The VOUT_MIN command sets a lower limit on the converter's commanded output voltage, regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level. It is not the primary under-voltage protection (UVP).

Command	**VOUT_MIN**							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	VOUT_MIN							

Bits	Bit Name	Description
7:0	VOUT_MIN	Sets the minimum V_{OUT} setting, which can be between 0.20625V and 1.8V. The minimum V_{OUT} can be calculated with following equation: V_{OUT_MIN} = (VOUT_MIN x 6.25mV + 206.25mV) x VOUT_SL Attempting to write a lower value to VOUT_COMMAND causes VOUT_COMMAND to be set to VOUT_MIN, and asserts a VOUT_MAX_MIN warning.

TON_DELAY (60h)

The TON_DELAY command sets the start-up delay.

Command	TON_DELAY							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED			TON_DELAY				

Bits	Bit Name	Description
7:5	RESERVED	Reserved.
4:0	TON_DELAY	The start-up delay (ranging between 0ms and 7.75ms) can be calculated with the following equation: Start-Up Delay = TON_DELAY x 0.25ms

TOFF_DELAY (64h)

The TOFF_DELAY command sets the shutdown delay.

Command	TOFF_DELAY							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED			TOFF_DELAY				

Bits	Bit Name	Description
7:5	RESERVED	Reserved.
4:0	TOFF_DELAY	The shutdown delay (ranging between 0ms and 7.75ms) can be calculated with the following equation: Shutdown Delay = TOFF_DELAY x 0.25ms

STATUS_BYTE (78h)

The STATUS_BYTE command returns flags indicating the state of the MPQ7930.

Command	STATUS_BYTE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function								

Bits	Bit Name	Description
7	BUSY	0: No busy fault has occurred 1: A fault was declared because the device was busy and unable to respond
6	OFF	0:The device is on 1: The device is off
5	VOUT_OV_FAULT	0: No output over-voltage (OV) fault has occurred 1: An output OV fault has occurred
4	VOUT_UV_FAULT	0: No output under-voltage (UV) fault has occurred 1: An output UV fault has occurred
3	RESERVED	Reserved.
2	TEMPERATURE	0: No temperature fault or warning has occurred 1: A temperature fault or warning has occurred
1	CML	0: No communications, memory, or logic fault has occurred. 1: A communications, memory, or logic fault has occurred.
0	FAULT_OTHER	0: No other fault has occurred 1: A VOUT_MAX/MIN fault has occurred.

STATUS_WORD (79h)

The STATUS_WORD command returns 2 bytes of information with a summary of the device's fault/warning conditions. The higher byte provides more detailed information on the fault conditions. The higher byte is shared with the STATUS_BYTE command.

Command	STATUS_WORD															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	STATUS_BYTE															

Bits	Bit Name	Description
15:8 (high byte)	STATUS_BYTE	These bits are the same as STATUS_BYTE.
7	VOUT_FAULT	0: No output voltage fault has occurred 1: An output voltage fault has occurred
6	VO_UV_FAULT	0: No output under-voltage (UV) fault has occurred 1: An output UV fault has occurred
5	RESERVED	RESERVED
4	MANUFAC_FAULT	0: No manufacturer-specific fault has occurred 1: A manufacturer-specific fault has occurred
3	PGOOD	0: This bit is high 1: This bit is low
2:0	RESERVED	Reserved.

STATUS_VOUT (7Ah)

The STATUS_VOUT command provides information on voltage-related faults.

Command	STATUS_VOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function						PG_OV	PG_UV	

Bits	Bit Name	Description
7	VOUT_OV_FAULT	0: No output over-voltage (OV) fault has occurred 1: An output OV fault has occurred
6:5	RESERVED	Reserved.
4	VOUT_UV_FAULT	0: No output-under voltage (UV) fault has occurred 1: An output UV fault has occurred
3	RESERVED	Reserved.
2	PG_OV	0: No PG OV fault has occurred 1: A PG OV fault has occurred
1	PG_UV	0: No PG UV has occurred 1: A PG UV fault has occurred
0	VOUT_MAX_MIN	0: No V_{OUT} max/min fault has occurred 1: A V_{OUT} max/min fault has occurred

STATUS_TEMPERATURE (7Dh)

The STATUS_TEMPERATURE command provides information on temperature-related faults and warnings.

Command	STATUS_TEMPERATURE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function			RESERVED					

Bits	Bit Name	Description
7	TEMP_OT_FAULT	0: No over-temperature (OT) fault has occurred 1: An OT fault has occurred

6	TEMP_OT_WARNING	0: No OT warning has occurred 1: An OT warning has occurred
5:0	RESERVED	Reserved.

STATUS_CML (7Eh)

The STATUS_CMEL command provides information on certain statuses.

Command	STATUS_CML							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function				RESERVED				

Bits	Bit Name	Description
7	INVALID_CMD	0: No invalid or unsupported commands have been received 1: An invalid or unsupported command has been received
6	INVALID_DATA	0: No invalid or unsupported data received 1: Invalid or unsupported data has been received
5	PEC_ERROR	0: The packet error check (PEC) has not failed 1: The PEC failed
4:1	RESERVED	Reserved.
0	COM_FAULT	0: No communication fault has occurred 1: A communication fault has occurred

SECURE_LOCKOUT (9Dh)

The SECURE_LOCKOUT command can lock out access to most registers.

Command	SECURE_LOCKOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	SECURE_LOCKOUT							

Bits	Bit Name	Description
7:0	SECURE_LOCKOUT	Write 01011010 to this command lock out write access to most registers. It is possible to write to registers listed as “No” in the Lockout column in the Register Map section on page 37. These bits can only be cleared by setting all enables to low.

MULTIPHASE_CONFIG (9Eh)

The MULTIPHASE_CONFIG command selects multi-phase or independent operation for the buck converters.

Command	MULTIPHASE_CONFIG							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED							

Bits	Bit Name	Description
7:3	RESERVED	Reserved.

2	MULTIPHASE_B5B6	Selects multi-phase operation for buck 5 and buck 6. 0: Independent 1: Multi-phase. Buck 5 operates as the primary converter
1	MULTIPHASE_B3B4	Selects multi-phase operation for buck 3 and buck 4. 0: Independent 1: Multi-phase. Buck 3 operates as the primary converter
0	MULTIPHASE_B2B1	Selects multi-phase operation for buck 1 and buck 2. 0: Independent 1: Multi-phase. Buck 1 operates as the primary converter

HICCUP_TIMER (A0h)

The HICCUP_TIMER command sets the hiccup timer.

Command	HICCUP_TIMER							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED						HICCUP_TIMER	

Bits	Bit Name	Description
7:2	RESERVED	Reserved.
1:0	HICCUP_TIMER	00: 2ms 01: 4ms 10: 6ms 11: 8ms

STATUS_PIN_STATE (A1h)

The STATUS_PIN_STATE command indicates the state of the EN1–6, PG, and ALERT pins. If a pin's voltage exceeds the threshold, its corresponding bit is set to 1.

Command	STATUS_PIN_STATE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function								

Bits	Bit Name	Description
7	EN_6_STATE	Indicates the state of the EN6 pin.
6	EN_5_STATE	Indicates the state of the EN5 pin.
5	EN_4_STATE	Indicates the state of the EN4 pin.
4	EN_3_STATE	Indicates the state of the EN3 pin.
3	EN_2_STATE	Indicates the state of the EN2 pin.
2	EN_1_STATE	Indicates the state of the EN1 pin.
1	PG_MEAS_STATE	Indicates the state of the PG pin.
0	ALERT_MEAS_STATE	Indicates the state of the ALERT pin.

VOUT_STARTUP_SLEW (A3h)

The VOUT_STARTUP_SLEW command sets the start-up slew rate.

Command	VOUT_STARTUP_SLEW							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED							

Bits	Bit Name	Description
7:2	RESERVED	Reserved.
1:0	VOUT_STARTUP_ SLEW	00: VOUT_SL x 1.25mV/µs 01: VOUT_SL x 2.5mV/µs 10: VOUT_SL x 5mV/µs 11: VOUT_SL x 10mV/µs

VOUT_SHUTDOWN_SLEW (A5h)

The VOUT_SHUTDOWN_SLEW command sets the shutdown slew rate.

Command	VOUT_SHUTDOWN_SLEW							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function								

Bits	Bit Name	Description
7:2	RESERVED	Reserved.
1:0	VOUT_SHUTDOWN_ SLEW	00: VOUT_SL x 1.25mV/µs 01: VOUT_SL x 2.5mV/µs 10: VOUT_SL x 5mV/µs 11: VOUT_SL x 10mV/µs

VOUT_SLEW (A7h)

The VOUT_SLEW command sets the V_{OUT} slew rate.

Command	VOUT_SLEW							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED						VOUT_SLEW	

Bits	Bit Name	Description
7:2	RESERVED	Reserved.
1:0	VOUT_SLEW	00: VOUT_SL x 2.5mV/µs 01: VOUT_SL x 5mV/µs 10: VOUT_SL x 10mV/µs 11: VOUT_SL x 20mV/µs

OUTPUT_DISCHARGE (A9h)

The OUTPUT_DISCHARGE command should be written to 01. This ensures that a 100Ω discharge resistor is connected between the VOUTx pin and AGND pin.

Command	OUTPUT_DISCHARGE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED							

Bits	Bit Name	Description
7:1	RESERVED	Reserved.
0	DISCHARGE_EN	1: A 100Ω discharge resistor is connected to between the VOUTx pin and the AGND pin

FREQUENCY_DITHER (ADh)

The FREQUENCY_DITHER command enables frequency spread spectrum (FSS).

Command	FREQUENCY_DITHER							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED							

Bits	Bit Name	Description
7:1	RESERVED	Reserved.
0	FREQUENCY_DITHER	Enables frequency spread spectrum (FSS). 0: Disabled 1: Enabled

COMPENSATION_CONFIG_1 (B0h)

The COMPENSATION_CONFIG_1 command configures the compensation network parameters.

Command	COMPENSATION_CONFIG_1							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RCOMP							

Bits	Bit Name	Description
7:4	RCOMP	Sets R_{COMP}. The default selection in 1000. 50kΩ/LSB. 0000: 550kΩ 0001: 600kΩ 0010: 450kΩ 0011: 500kΩ 0100: 750kΩ 0101: 800kΩ 0110: 650kΩ 0111: 700kΩ 1000: 150kΩ 1001: 200kΩ 1010: 50kΩ 1011: 100kΩ 1100: 350kΩ 1101: 400kΩ 1110: 250kΩ 1111: 300kΩ
3	RESERVED	Reserved.
2:0	CCOMP_HP	Sets C_{COMP_HP}. The default selection is 011. 100pF/LSB. 000: 0 001: +LSB … 111: +7 x LSB

COMPENSATION_CONFIG_2 (B1h)

The COMPENSATION_CONFIG_2 command configures the compensation network parameters.

Command	COMPENSATION_CONFIG_2							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function		CCOMP_LF			RESERVED		SLOPE_COMP	

Bits	Bit Name	Description
7	RESERVED	Reserved.
6:4	CCOMP_LF	Sets CCOMP_LF. The default selection is 001. 000: 44.5pF 001: 49.5pF 010: 54.5pF 011: 59.5pF 100: 24.5pF 101: 29.5pF 110: 34.5pF 111: 39.5pF
3:2	RESERVED	Reserved.
1:0	SLOPE_COMP	Sets SLOPE_COMP. The default selection is 10. 00: I_{SLOPE} 01: I_{SLOPE} x 2 10: I_{SLOPE} x 3 11: I_{SLOPE} x 4

ALERT_PG_FORCE_ASSERT (C0h)

The ALERT_PG_FORCE_ASSERT command forces PG and ALERT to assert.

Command	ALERT_PG_FORCE_ASSERT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function								

Bits	Bit Name	Description
7:2	RESERVED	Reserved.
1	ALERT_FORCE_ ASSERT	Forces ALERT to assert. 0: Do not force ALERT to be asserted 1: Forces ALERT to be asserted
0	PG_FORCE_ASSERT	Forces PG to assert. 0: Do not force PG to be asserted 1: Forces PG to be asserted

PROTECTION_CONFIG (C2h)

The PROTECTION_CONFIG command enables certain functions.

Command	PROTECTION_CONFIG							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED			OVP_EN	UVP_EN	RESERVED		PEC_REQ

Bits	Bit Name	Description
7:5	RESERVED	Reserved.
4	OVP_EN	0: Disable over-voltage protection (OVP) 1: Enable OVP
3	UVP_EN	0: Disable under-voltage protection (UVP) 1: Enable UVP
2:1	RESERVED	Reserved.
0	PEC_REQ	Enables the PEC function. 0: PEC disabled (default) 1: PEC is optional

ALTERT#_MAPPING (C4h)

The ALTERT#_MAPPING command configures whether ALERT pulls low for certain PMBus errors.

Command	ALTERT#_MAPPING							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED						RESERVED	

Bits	Bit Name	Description
7:4	RESERVED	Reserved.

3	PM_CML_ALERT_MAPPING	Maps the PMBus communication failure for ALERT. 0: A PMBus communication failure causes ALERT to pull low and the register asserts (default) 1: A PMBus communication failure cause register assertion only
2	PM_CRC_ALERT_MAPPING	Maps the PMBus cyclic redundancy check (CRC) failure for ALERT. 0: A PMBus CRC failure causes ALERT to pull low and the register asserts (default) 1: A PMBus CRC failure causes the related register to assert only
1:0	RESERVED	Reserved.

PG_MAPPING (C6h)

The PG_MAPPING command configures whether PG pulls low for certain PMBus errors.

Command	PG_MAPPING							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED						RESERVED	

Bits	Bit Name	Description
7:4	RESERVED	Reserved.
3	PM_CML_PG_MAPPING	Maps the PMBus communication failure for PG. 0: A PMBus communication failure causes PG to pull low and the register asserts (default) 1: A PMBus communication failure cause register assertion only
2	PM_CRC_PGMAPPING	Maps the PMBus cyclic redundancy check (CRC) failure for PG. 0: A PMBus CRC failure causes PG to pull low and the register asserts (default) 1: A PMBus CRC failure causes the related register to assert only
1:0	RESERVED	Reserved.

PG_ALERT_DELAY (C8h)

The PG_ALERT_DELAY command sets the de-assertion delays for ALERT and PG.

Command	PG_ALERT_DELAY							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED				ALERT_DELAY		PG_DELAY	

Bits	Bit Name	Description
7:4	RESERVED	Reserved.
3:2	ALERT_DELAY	Sets the ALERT de-assertion delay. 00: Immediate 01: 2ms (default) 10: 5ms 11: 10ms
1:0	PG_DELAY	Sets the PG de-assertion delay. 00: Immediate 01: 2ms (default) 10: 5ms 11: 10ms

PG_CONFIG (CAh)

The PG_CONFIG command sets certain configurations for PG.

Command	PG_CONFIG							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED							

Bits	Bit Name	Description
7:2	RESERVED	Reserved.
1	PG_MASK	Masks PG. 0: PG is not masked for this channel 1: PG is masked for this channel
0	PG_THRESHOLD	Sets the PG threshold. 0: +6.5% / -5.5% 1: +4.5% / -3.5%

LIGHT_LOAD (CCh)

POR/soft reset value: 00000001

The LIGHT_LOAD command should be written to 01. This ensures that the MPQ7930 can work normally in FCCM.

Command	LIGHT_LOAD							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED							FCCM

Bits	Bit Name	Description
7:1	RESERVED	Reserved.
0	FCCM	1: The MPQ7930 can work normally in FCCM

ILIM_SCALE (CEh)

The ILIM_SCALE command sets the current limit scale.

Command	ILIM_SCALE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RESERVED						ILIM_SCALE	

Bits	Bit Name	Description
7:2	RESERVED	Reserved.
1:0	ILIM_SCALE	Sets the current limit scale. 00: 100% 01: 75% 10: 50%

ADDRESS (D5h)

The ADDRESS command sets the address for PMBus communication.

Command	ADDRESS							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function		ADDRESS						

Bits	Bit Name	Description
7	RESERVED	Reserved.
6:0	ADDRESS	7-bit PMBus Address

CONFIG_CODE (D6h)

The CONFIG_CODE command returns the configuration code.

Command	CONFIG_CODE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	CONFIG_CODE							

Bits	Bit Name	Description
7:0	CONFIG_CODE	Returns the configuration code info.

MFR_OTP_MEM_STATUS (DBh)

The MFR_OTP_MEM_STATUS command indicates whether certain OTP-related errors have occurred.

Command	MFR_OTP_MEM_STATUS							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	RESERVED					RESERVED		

Bits	Bit Name	Description
7:6	RESERVED	Reserved.
5	STRUP_OTP_CRC_ ERR	0: No start-up load OTP CRC error has occurred 1: A start-up load OTP CRC error has occurred
4	STRUP_OTP_IND_ ERR	0: No start-up load OTP indicator error has occurred 1: A start-up load OTP indicator error has occurred
3	STORE_OTP_ERR	0: No store OTP failure has occurred 1: A store OTP failure has occurred
2:0	RESERVED	Reserved.

APPLICATION INFORMATION

Figure 12 shows the MPQ7930's typical application circuit.

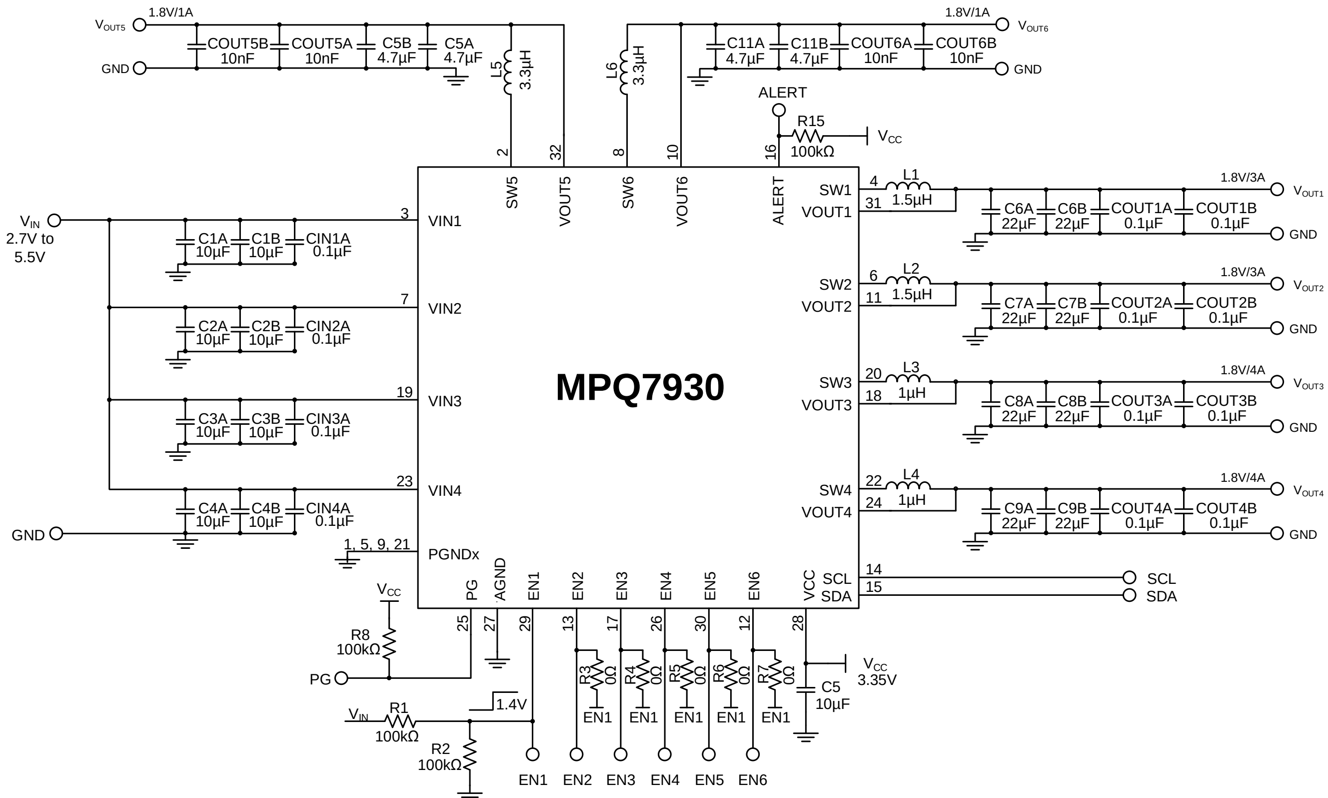


Figure 12: Typical Application Circuit (V_{OUT1-6} = 1.8V, f_{SW} = 2MHz)

Table 2: Design Guide Index

Pin #	Pin Name	Component	Design Guide Index
1, 5, 9, 21	PGNDx	-	GND Connection (PGNDx, Pins 1, 5, 9 and 21; AGND, Pin 27)
2	SW5	L5, C10A, C10B, COUT5A, COUT5B	Selecting the Output Capacitors (SW1, Pin 4; SW2, Pin 6; SW3, Pin 20; SW4, Pin 22; SW5, Pin 2; SW6, Pin 8) Selecting the Inductors (SW1, Pin 4; SW2, Pin 6; SW3, Pin 20; SW4, Pin 22; SW5, Pin 2; SW6, Pin 8)
3, 7, 19, 23	VINx	C1A, C1B, C2A, C2B, C3A, C3B, C4A, C4B, CIN1A, CIN1B, CIN2A, CIN2B ,CIN3A, CIN3B, CIN4A, CIN4B	Selecting the Input Capacitors (VINx, Pins 3, 7, 19, and 23)
4	SW1	L1, C6A, C6B, COUT1A, COUT1B	Selecting the Output Capacitors (SW1, Pin 4; SW2, Pin 6; SW3, Pin 20; SW4, Pin 22; SW5, Pin 2; SW6, Pin 8) Selecting the Inductors (SW1, Pin 4; SW2, Pin 6; SW3, Pin 20; SW4, Pin 22; SW5, Pin 2; SW6, Pin 8)
6	SW2	L2,C7A,C7B,COUT2A, COUT2B	Selecting the Output Capacitors (SW1, Pin 4; SW2, Pin 6; SW3, Pin 20; SW4, Pin 22; SW5, Pin 2; SW6, Pin 8) Selecting the Inductors (SW1, Pin 4; SW2, Pin 6; SW3, Pin 20; SW4, Pin 22; SW5, Pin 2; SW6, Pin 8)

Table 2: Design Guide Index *(continued)*

Pin #	Pin Name	Component	Design Guide Index
8	SW6	L6, C11A, C11B, COUT6A, COUT6B	Selecting the Output Capacitors (SW1, Pin 4; SW2, Pin 6; SW3, Pin 20; SW4, Pin 22; SW5, Pin 2; SW6, Pin 8) Selecting the Inductors (SW1, Pin 4; SW2, Pin 6; SW3, Pin 20; SW4, Pin 22; SW5, Pin 2; SW6, Pin 8)
10	VOUT6	-	Setting the Output Voltage (VOUT1, Pin 31; VOUT2, Pin 11; VOUT3, Pin 18; VOUT4, Pin 24; VOUT5, Pin 32; VOUT6, Pin 10)
11	VOUT2	-	Setting the Output Voltage (VOUT1, Pin 31; VOUT2, Pin 11; VOUT3, Pin 18; VOUT4, Pin 24; VOUT5, Pin 32; VOUT6, Pin 10)
12	EN6	R7	Buck Enable Signal (EN1, Pin 29; EN2, Pin 13; EN3, Pin 17; EN4, Pin 26; EN5, Pin 30; EN6, Pin 12)
13	EN2	R3	Buck Enable Signal (EN1, Pin 29; EN2, Pin 13; EN3, Pin 17; EN4, Pin 26; EN5, Pin 30; EN6, Pin 12)
14	SCL	-	PMBus Interface (SCL, Pin 14; SDA, Pin 15)
15	SDA	-	PMBus Interface (SCL, Pin 14; SDA, Pin 15)
16	ALERT	-	Power Good and ALERT Indicators (ALERT, Pin 16; PG, Pin 25)
17	EN3	R4	Buck Enable Signal (EN1, Pin 29; EN2, Pin 13; EN3, Pin 17; EN4, Pin 26; EN5, Pin 30; EN6, Pin 12)
18	VOUT3	-	Setting the Output Voltage (VOUT1, Pin 31; VOUT2, Pin 11; VOUT3, Pin 18; VOUT4, Pin 24; VOUT5, Pin 32; VOUT6, Pin 10)
20	SW3	L3, C8A, C8B, COUT3A, COUT3B	Selecting the Output Capacitors (SW1, Pin 4; SW2, Pin 6; SW3, Pin 20; SW4, Pin 22; SW5, Pin 2; SW6, Pin 8) Selecting the Inductors (SW1, Pin 4; SW2, Pin 6; SW3, Pin 20; SW4, Pin 22; SW5, Pin 2; SW6, Pin 8)
22	SW4	L4, C9A ,C9B, COUT9A, COUT9B	Selecting the Output Capacitors (SW1, Pin 4; SW2, Pin 6; SW3, Pin 20; SW4, Pin 22; SW5, Pin 2; SW6, Pin 8) Selecting the Inductors (SW1, Pin 4; SW2, Pin 6; SW3, Pin 20; SW4, Pin 22; SW5, Pin 2; SW6, Pin 8)
24	VOUT4	-	Setting the Output Voltage (VOUT1, Pin 31; VOUT2, Pin 11; VOUT3, Pin 18; VOUT4, Pin 24; VOUT5, Pin 32; VOUT6, Pin 10)
25	PG	-	Power Good and ALERT Indicators (ALERT, Pin 16; PG, Pin 25)
26	EN4	R5	Buck Enable Signal (EN1, Pin 29; EN2, Pin 13; EN3, Pin 17; EN4, Pin 26; EN5, Pin 30; EN6, Pin 12)
27	AGND	-	GND Connection (PGND, Pins 1, 5, 9, and 21; AGND, Pin 27)
28	VCC	C5	Internal VCC (VCC, Pin 28)
29	EN1	R1, R2	Buck Enable Signal (EN1, Pin 29; EN2, Pin 13; EN3, Pin 17; EN4, Pin 26; EN5, Pin 30; EN6, Pin 12)
30	EN5	R6	Buck Enable Signal (EN1, Pin 29; EN2, Pin 13; EN3, Pin 17; EN4, Pin 26; EN5, Pin 30; EN6, Pin 12)
31	VOUT1	-	Setting the Output Voltage (VOUT1, Pin 31; VOUT2, Pin 11; VOUT3, Pin 18; VOUT4, Pin 24; VOUT5, Pin 32; VOUT6, Pin 10)
32	VOUT5	-	Setting the Output Voltage (VOUT1, Pin 31; VOUT2, Pin 11; VOUT3, Pin 18; VOUT4, Pin 24; VOUT5, Pin 32; VOUT6, Pin 10)

Setting the Output Voltage (VOUT1, Pin 31; VOUT2, Pin11; VOUT3, Pin 18; VOUT4, Pin 24; VOUT5, Pin 32; VOUT6, Pin 10) (9) (10) (11)

The OTP registers VOUT_COMMAND and VOUT_SCALE_LOOP set the output voltage.

Write to VOUT_CMD (VOUT_COMMAND (21h), bits[7:0]), and VOUT_SC_L VOUT_SCALE_LOOP (29h), bit[0]).

The output voltage can be calculated with Equation (1):

$$V_{OUT}(mV) = (VOUT\_CMD \times 6.25 + 206.25) \times VOUT\_SL \quad (1)$$

Notes:

9) It is recommended that the duty cycles for buck 1, buck 2, buck 5, and buck 6 do not exceed 40%. If buck 1 is disabled, then the buck 5 duty cycle is not limited. If buck 5 is disabled, the buck 1 duty cycle is not limited. If buck 2 is disabled, the buck 6 duty cycle duty cycle is not limit. If buck 6 is disabled, the buck 2 duty cycle is not limited.
10) The output voltage should be ≤1.8V before the next start-up.
11) If the voltage on the VOUTx pin is below 0.5V, the corresponding buck's switching frequency decreases, and the other buck's switching frequency is not affected.

Selecting the Input Capacitor (VINx, Pins 3, 7, 19, and 23)

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

It is strongly recommended to use another lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and GND as possible.

Since C_{IN} absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (2):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (2)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (3):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (3)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (4):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

Selecting the Output Capacitor (SW1, Pin 4; SW2, Pin 6; SW3, Pin 20; SW4, Pin 22; SW5, Pin2; SW6, Pin 8)

The output capacitor maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be calculated with Equation (5):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}}\right) \quad (5)$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple.

For simplification, the output voltage ripple can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be calculated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (7)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ7930 can be optimized for a wide range of capacitance and ESR values.

Selecting the Inductor (SW1, Pin 4; SW2, Pin 6; SW3, Pin 20; SW4, Pin 22; SW5, Pin 2; SW6, Pin 8)

A 1µH to 10µH inductor with a DC current rating at least 25% higher than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductor value is to allow the inductor ripple current to be approximately 30% of the maximum load current. The inductance value can be estimated with Equation (8):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (9):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

Internal VCC (VCC, Pin 28)

The VCC capacitor (C5) is recommended to be 10µF.

Most of the internal circuitry is powered by the internal 3.35V VCC regulator. This regulator uses VIN as its input and operates across the full V_{IN} range. When V_{IN} exceeds 3.35V, V_{CC} is in full regulation. When V_{IN} drops below 3.35V, the VCC output degrades.

PMBus Interface (SCL, Pin 14; SDA, Pin 15)

The MPQ7930 works as a slave-only device that supports both standard mode (100kb/s) and fast mode (400kb/s) bidirectional data transfer, adding flexibility to the power supply solution. Refer to the PMBus Interface section on page 33 for details.

The SCL and SDA lines are externally pulled to a bus voltage with a resistor (e.g. 1kΩ).

Power Good and ALERT Indicators (ALERT, Pin 16; PG, Pin 25)

The PG and ALERT pins have an internal, integrated push-pull structure and do not require external components. They have different behaviors for different faults. See Table 1 on page 32 for more details.

Buck Enable Signal (EN1, Pin 29; EN2, Pin 13; EN3, Pin 17; EN4, Pin 26; EN5, Pin 30; EN6, Pin 12)

The MPQ7930 provides six EN pins (EN1–6). Each buck is controlled by the corresponding ENx pin.

If the ENx level is between ENx_Logic_Threshold and ENx_Rising_Threshold, the corresponding buck has no output voltage, but VCC and the PMBus operate normally.

Short EN2–6 with EN1 to control all bucks by the same EN.

GND Connection (PGNDx, Pins 1, 5, 9 and 21; AGND, Pin 27)

See the PCB Layout Guidelines section on page 57 for more details.

PCB Layout Guidelines [12]

Efficient PCB layout, especially for input capacitor placement, is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 13 and follow the guidelines below:

1. Place the input capacitors as close to VIN and GND as possible.
2. Use a large ground plane to connect to PGND directly.
3. Add vias near PGND if the bottom layer is a ground plane.
4. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
5. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high frequency noise.
6. Keep the connection between the input capacitor and VIN as short and wide as possible.
7. Place the VCC capacitor as close to VCC and GND as possible.
8. Route SW away from sensitive analog areas, such as FB.
9. Ensure that the trace between FB and the output is as short as possible.
10. Use multiple vias to connect the power planes to the internal layers.

Notes:

12) The recommended PCB layout is based on Figure 12 on page 53.

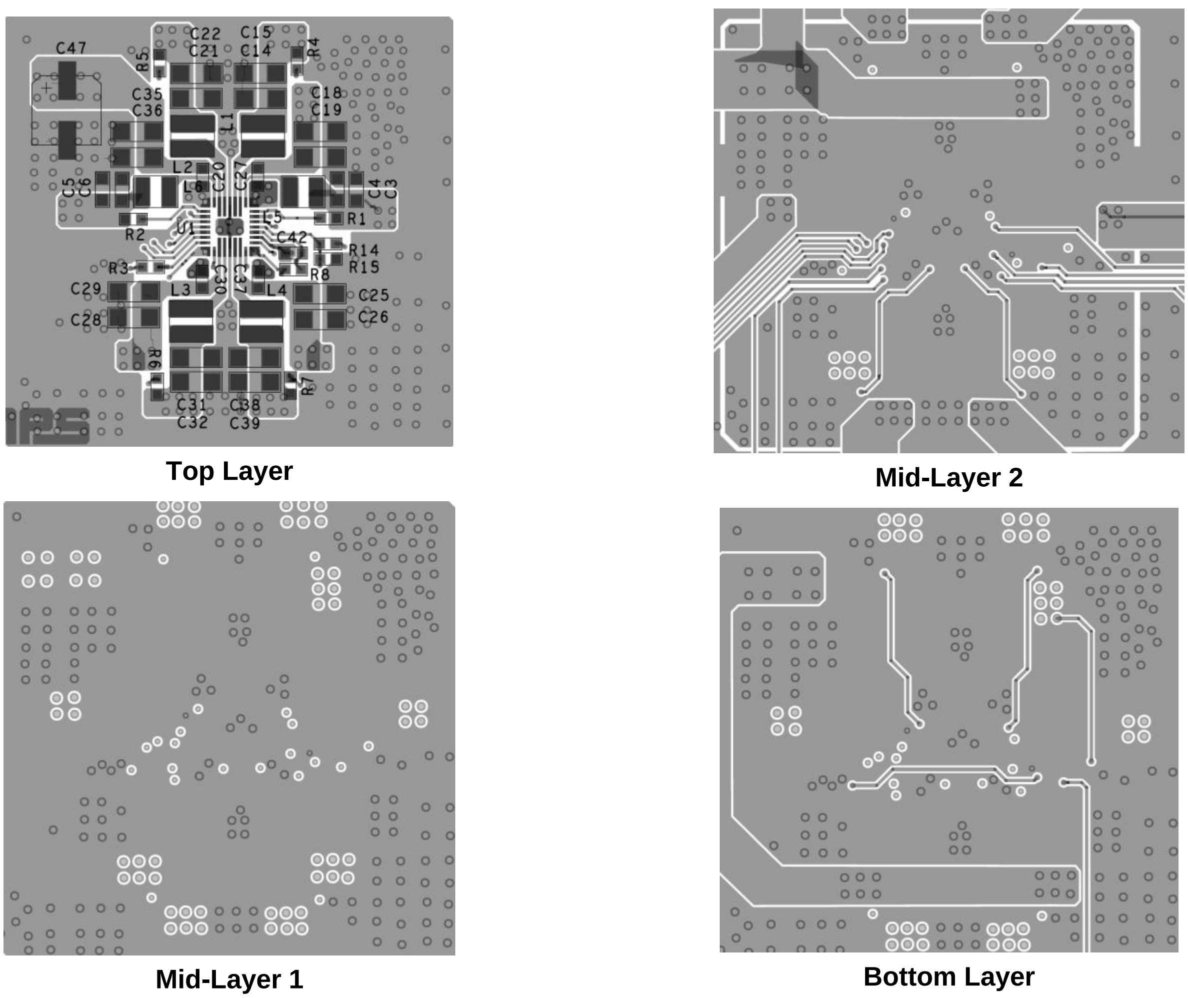


Figure 13: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

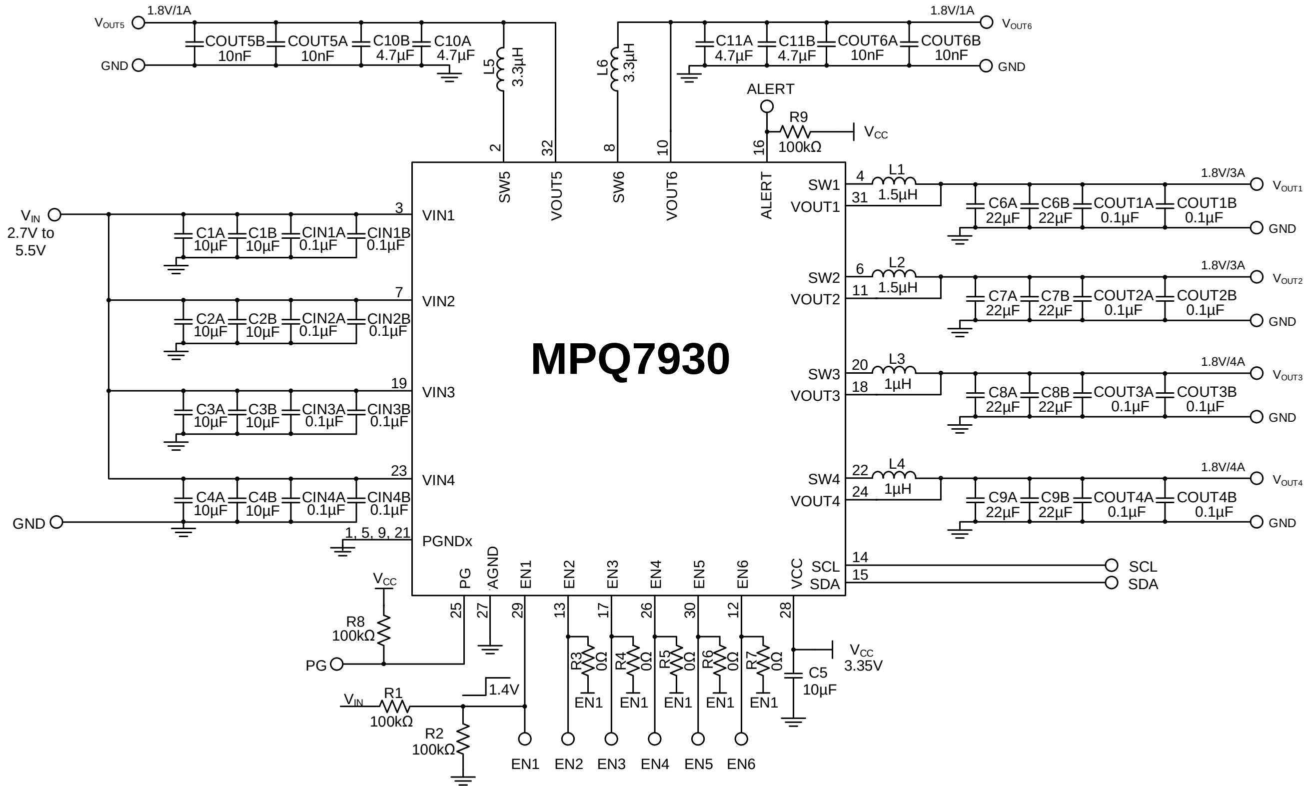
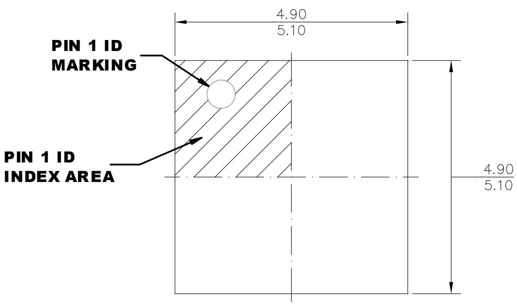


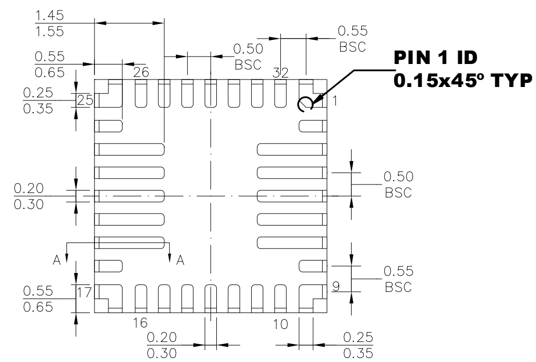
Figure 14: Typical Application Circuit (V_{OUT1-6} = 1.8V, f_{SW} = 2MHz)

PACKAGE INFORMATION

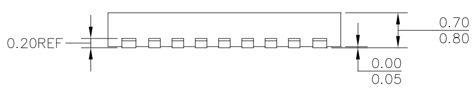
TQFN-32 (5mmx5mm)
Wettable Flank



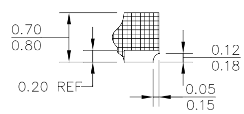
TOP VIEW



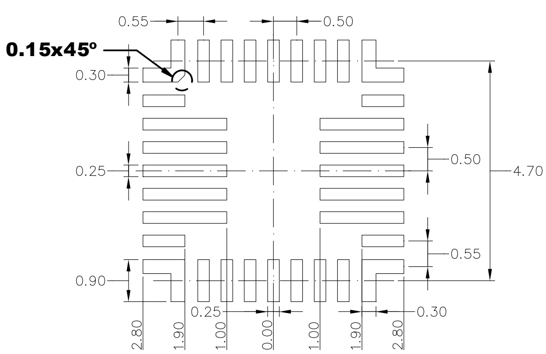
BOTTOM VIEW



SIDE VIEW



SECTION A-A

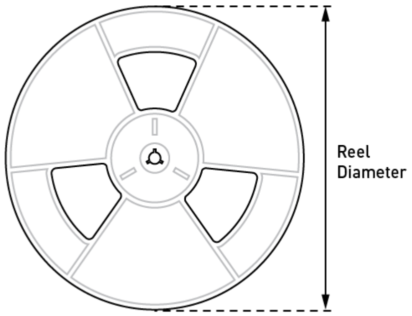


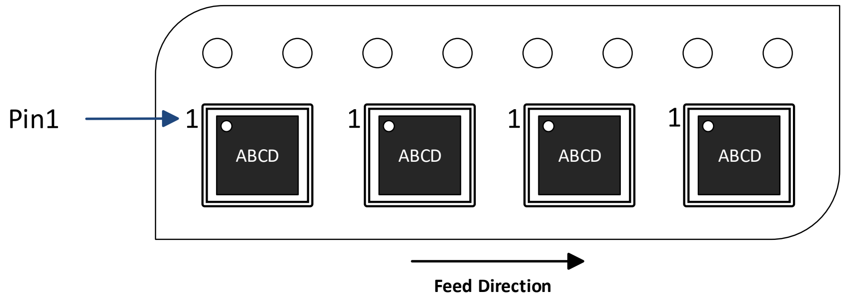
RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube (13)	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ7930GUTE-xxxx-AEC1-Z	TQFN-32 (5mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

Note:

13) N/A indicates "not available" in tubes. For 500 pieces tape and reel prototype quantities, contact the factory. (The order code for 500 pieces, which is a partial reel is, "-P". The tape and reel dimensions are the same as the full reel.)

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/14/2023	Initial Release	-