Mask Set Errata for Mask 1N00R

This report applies to mask 1N00R for these products:

• S912ZVMC256

Table 1. Errata and Information Summary

Erratum ID	Erratum Title
	PMF: Unexpected pulse visible on the PMF output, if in PMF ASYM mode the odd VAL register are set to zero to deactivate the ongoing PWM signal generation

Table 2. Revision History

Revision	Changes
1 July 2016	Initial revision

e10418: PMF: Unexpected pulse visible on the PMF output, if in PMF ASYM mode the odd VAL register are set to zero to deactivate the ongoing PWM signal generation

Description: When any of the PWM pairs in the PMF module is operating in asymmetric complementary center-aligned mode, with half cycle reload enabled.

PMF configuration:

- Prescaler value: PRSC{A,B,C} != 00
- Complementary mode: PMFCFG0 INDEP{A,B,C}=0
- Center aligned outputs: PMFCFG0 EDGE{A,B,C}=0
- Asymmetric mode: PMFICCTL_ICC{A,B,C}=1
- Normal pulse edge control: PMFICCTL PEC{A,B,C}=0
- Half cycle reload enabled: PMFFQC{A,B,C}_HALF{A,B,C}=1



And any of the following two conditions below (A or B) occur, an unexpected pulse with a width of "dead time" will be visible in the corresponding odd PWM channel output (PWM1,3 or 5)

Condition A.

- 1a. Setting the odd PWM channel to 0 (PMFVAL{1,3,5}=0) and loaded into the internal buffer (LDOKA=1) before next half cycle start, and
- 2a. Setting the even PWM channel to 0 (PMFVAL{0,2,4}=0)) and loaded into the internal buffer (LDOKA=1) before next full cycle start.

Condition B.

- 1b. Setting the odd PWM channel to 0 (PMFVAL{1,3,5}=0) and loaded into the internal buffer (LDOKA=1) before next full cycle start, and
- 2b. Setting the even PWM channel to 0 (PMFVAL{0,2,4}=0)) before next full cycle start and loaded into the internal buffer (LDOKA=1) before next full cycle start

Workaround: Set both VAL registers of each complementary pair, PMFVAL{1,3,5} and PMFVAL{0,2,4}, to zero before the next half cycle start to disable the PMF output and correct the unexpected pulse

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