SR150

Ultra-Wideband Transceiver

Rev. 1.0 — 13 October 2021 Product short data sheet
709010 COMPANY PUBLIC

1 Introduction

The SR150 is a single die UWB controller that provides common Ultra-Wideband (UWB) ranging technologies like Single-Sided (SS) and Double-Sided (DS) Two-Way-Ranging (TWR) and Time Differential of Arrival (TDoA) Ranging. SR150 also supports generation of the Scrambled Timing Sequence (STS) needed for IEEE802.15.4z enhanced and secure ranging. The SR150 is capable of secure ranging achieving an accuracy of < ±10cm. Further the SR150 can perform measurement of the angle of arrival with an accuracy of ±3° in one measurement cycle using the on-chip dual receiver architecture. It is designed for Ranging applications in an IOT environment.

2 Features and benefits

SR150 support the following features:

- IEEE 802.15.4z HRP PHY compliant
- Supports SHF UWB bands from 6.24 GHz to 8.24 GHz for worldwide use (channel 5, 6, 8 and 9)
- Supports 64MHz and 128MHz PRF mode to optimize FCC TX spectrum efficiency
- Optimized for short frame mode operation at maximum FCC TX limits
- Programmable transmitter output power of up to 10dBm
- Complies with FCC & ETSI UWB spectral masks
- Data rates of 850kbps, 6.8Mbps, 7.8Mbps, 27Mbps and 31.2Mbps
- Supports 2-way ranging and one-way ranging (TDOA)
- Supports Angle of Arrival Measurement
- Support connection to Secure Element (SE051x)
- Security PHY Layer Secure Ranging features to reject Cicada and Preamble Injection attacks
- Scrambled Timestamp Sequence (STS) generation compliant to NIST SP 800-90A (see [3])
- Based on ARM® Cortex-M33 with ARM® TrustZone (see [1] and [2])
- FiRa ready MAC and PHY; with priority based scheduling and hopping
- Built-in Secure FW Update capability
- Pre-programmed Firmware. No customer programming required

3 Applications

- IOT applications
- Location Service Anchor
- Smart Home Devices
- Access Control (Physical and Logical)

4 Pinning information

4.1 Pinning

SR150 is packaged in a WLSCP68

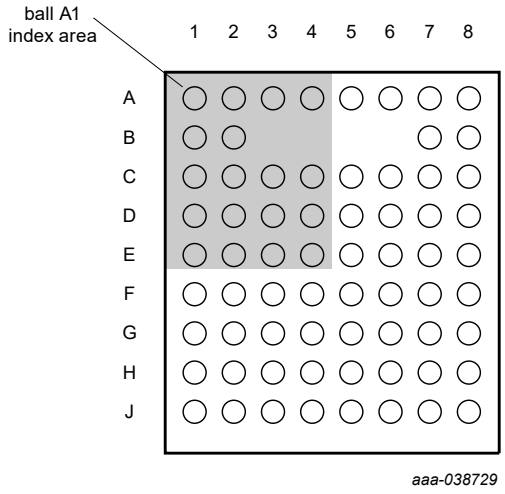

Figure 1. SR150 Transparent view

4.2 Pin description

Table 1. SR150 pin description

Symbol	Pin	Type	Refer	Description
XTAL1_38M	A1	I	N/A	RF-Interface oscillator input, supported clock frequency is 38.4MHz
VSS_REF	A2	G	N/A	Ground connection of the reference Voltage
RX1_IN	A3	I		Input of receiver 1
RX1_RFGND	A4	G		Ground supply of receiver 1
RX2_RFGND	A5	G		Ground supply of receiver 2
RX2_IN	A6	I		Input of receiver 2
VSS_Balun	A7	G	N/A	The ground supply
TX_OUT	A8	O		The signal output which can be connected to the transmitting Antenna
XTAL2_38M	B1	I	N/A	The second input for the 38.4MHz oscillator
VDD_AON	B2	P	N/A	The supply for the always on LDO
-	B3			unpopulated IO
-	B4			unpopulated IO
-	B5			unpopulated IO
-	B6			unpopulated IO
VSS_PA	B7	G	N/A	Ground supply for Power Amplifier

Table 1. SR150 pin description*...continued*

Symbol	Pin	Type	Refer	Description
VDD_PA	B8	P	N/A	VDD supply for the Power Amplifier
VDD_1V8	C1	P	N/A	1.8V supply Input
VSS_PLL	C2	G	N/A	Ground supply for the PLL
VSS_RX1	C3	G	N/A	Ground supply for RX1
VSS_LO	C4	G	N/A	Ground for the local oscillator
VSS_ANA_BB	C5	G	N/A	Ground supply for the analog baseband
VSS_RX2	C6	G	N/A	Ground supply for RX2
VSS_TX	C7	G	N/A	Ground supply for TX
XTAL1_32K	C8	I	N/A	Input for the 32KHz oscillator
VDD_DIG	D1	P	N/A	VDD decap output for the Digital
AMUX_P	D2	I/O		Reserved pin
AMUX_N	D3	I/O		Reserved pin
VIN_RF_1V8	D4	P	N/A	Vin input 1.8V RF
VDD_ANA_BB	D5	P	N/A	VDD supply for the analog baseband
VDD_1V8	D6	P	N/A	Vin input to all Digital LDOs
VDD_DIG_BB	D7	P	N/A	VDD for the digital baseband
XTAL2_32K	D8	I	VDD_PLL	Second input for the 32KHz oscillator
VSS_SUB	E1	G	N/A	Ground connection
HOST_1	E2	I	VDDIO_HOST	Host interface line 1, SPI clock line, switching time is 125ns.
HOST_4	E3	I/O	VDDIO_HOST	Host interface line 4, SPI MISO connection, switching time is 125ns.
CHIPENABLE	E4	I	VDD_IO	Connection for disabling/enabling the chip
TESTMODE	E5	I/O	VDD_IO	Reserved pin
SWD_CLK	E6	I/O	VDD_IO	Serial Wire Debug interface
GPIO06	E7	IO	VDD_IO	General Purpose IO, switching time is 125ns.
VSS_SUB	E8	G	N/A	Ground supply
HOST_3	F1	I/O	VDDIO_HOST	Host interface line 3. SPI MOSI connection, switching time is 125ns.
HOST_2	F2	I/O	VDDIO_HOST	Host interface line 2. SPI Slave select connection, switching time is 125ns.
GPIO02	F3	I/O	VDDIO_HOST	General Purpose IO, switching time is 125ns.
VSS_DIG	F4	G	N/A	Digital ground connection
SWD_IO	F5	I/O	VDD_IO	Serial Wire Debug interface
SE_1	F6	I/O	VDD_IO	NA Kept open.
GPIO05_HOST_INT	F7	I/O	VDD_IO	IRQ to host for indicating data ready, switching time is 125ns.
EF2	F8	I/O	VDD_IO	High switching speed general purpose IO used for antenna external switches

Table 1. SR150 pin description*...continued*

Symbol	Pin	Type	Refer	Description
VDDIO_HOST	G1		N/A	Power Supply for the Host Interface
GPIO03_SYNC	G2	I	VDDIO_HOST	SPI Rx handshake from the Host to the chip, switching time is 125ns.
GPIO09	G3	I/O	VDD_IO	General Purpose IO, switching time is 125ns.
SE_4	G4	I/O	VDD_IO	NA. Kept open.
SE_3	G5	I/O	VDD_IO	General purpose IO. Alternative customer configuration, switching time is 125ns.
SE_2	G6	I/O	VDD_IO	NA. Kept open.
UART2_TX	G7	I/O	VDD_IO	NA. Kept Open.
EF1	G8	I/O	VDD_IO	High switching speed general purpose IO used for antenna external switches.
GPIO14_ANT_CTRL2	H1	I/O	VDDIO_HOST	High switching speed general purpose IO used for antenna external switches.
GPIO04	H2	I/O	VDDIO_HOST	General Purpose IO, switching time is 125ns.
GPIO11_ANT_CTRL1	H3	I/O	VDD_IO	General purpose IO.
GPIO10	H4	I/O	VDD_IO	General Purpose IO, switching time is 125ns.
GPIO12	H5	I/O	VDD_IO	General purpose IO.
COEX_2	H6	I/O	VDD_IO	NA. Kept Open.
GPIO07	H7	I/O	VDD_IO	GPIO7 - General Purpose IO, switching time is 125ns.
UART2_RX	H8	I/O	VDD_IO	NA. Kept Open.
GPIO01	J1	I/O	VDDIO_HOST	General Purpose IO, switching time is 125ns.
VSS_DIG	J2	G	N/A	Ground supply for the Digital
RTC_SYNC	J3	I	VDD_IO	Not used. Kept open
GPIO08_SE_IRQ	J4	I/O	VDD_IO	NA. Kept open.
VDD_IO	J5		N/A	VDD supply for the IO pins
COEX_1	J6	I/O	VDD_IO	NA. Kept Open.
VSS_DIG	J7			Ground supply for the digital
GPIO13	J8	I/O	VDD_IO	General Purpose IO, switching time is 125ns.

5 Functional description

The SR150 can be connected to a host controller through SPI bus. SR150 is fully controllable by firmware. The SR150 has its own power management Unit which is supplied by the host PIMC with 1.8V. SR150 can be connected to external embedded Secure element though Host (AP) using secure channel. SR150 has 2 RX and one TX these can be connected via external switched to antenna matrix.

5.1 SYSTEM MODES

The SR150 has 6 power modes that are specified: Host power down mode, Deep power down mode, Deep power down retention mode, Sleep, Active mode and Hardware configuration Autoload. A description of the states can be found in Table 2.

Table 2. System Power states description

System power state	Description
Active mode	The device is running and supplied by the Platform PMU, in this mode several active states are available: Idle, TX, RX and Dual RX.
Deep power down mode (DPD) retention mode	The device is in low power mode and supplied by the Platform PMU, the memory is supplied, a configured wake up can bring the device back to the Active mode, for this a firmware reload is necessary, no RF communication is possible.
Sleep	Specific parts can be active or inactive, this sleep mode can be configured by firmware which enables several power states, no RF communication is possible.
Hard power down mode	The device is powered down and supplied by the PMU, it can by activated by the chip enable signal.
Hardware configuration Autoload	The devices is supplied by the platform PMU and is loading the Hardware configuration and firmware into the memory.

5.2 State Diagram and Power modes

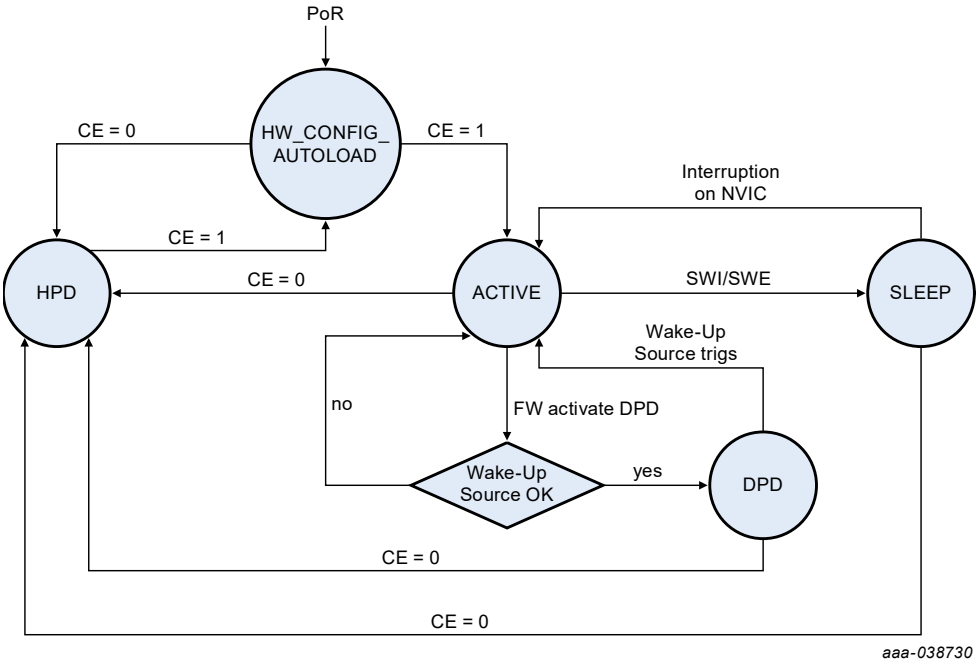

Figure 2. SR150 power modes state diagram

5.2.1 Power Mode Entry and Exit conditions

Table 3. SR150 Power state conditions

Power State	Entry Condition	Exit Conditions
HPD	Two possible methods • Software command • Assert CE low for > 80us	• Assert CE to high
DPD with memory retention mode	• Software command	Exit to HPD State: • Assert CE low for > 80us Exit to ACTIVE state: • Wakeup timer expired • Temperature sensor event • SPI NSS Negative Edge, GPIO (3,5) event
ACTIVE	• Enod of System Boot after wake up • Wakeup timer expired • Temperature sensor event • SPI NSS Negative Edge, GPIO (3,5) event	• Software command • Assert CE low for > 80us

The time required for SR150 to go into DPD from is <100us controlled by the firmware. Similarly, the required time for SR150 to enter HPD state is less than 100us starting for the instance that CE is de-asserted, in both modes VDD_DIG is turned OFF. The Wakeup timing from DPD state is around 370 us, the wakeup form HPD state is triggered once CE is asserted and takes around 380us.

Figure 3 shows the full system power cycle from wakeup until ranging.

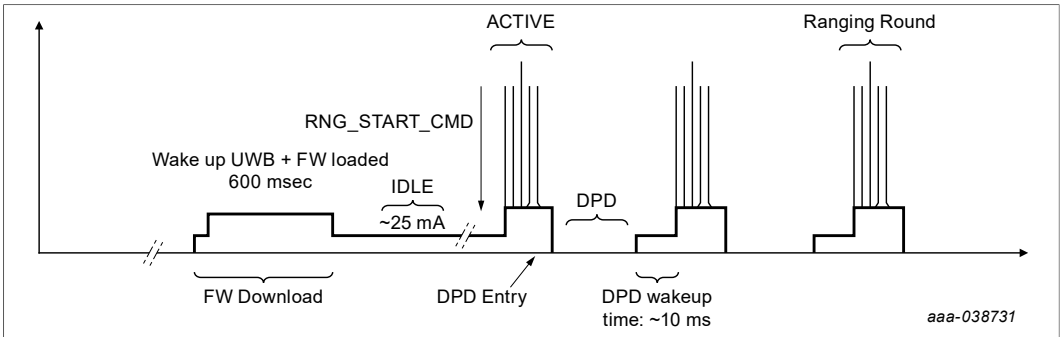

Figure 3. Typical system behavior form power on to ranging

5.3 CPU Subsystem

The digital control of the device is done with an ARM® Cortex®-M33 processor (see [3]). The 32-bit microcontroller implements the ARM® TrustZone extension. It is designed to provide low power and high-performance applications.

The CPU has optimized peripherals to facilitate quick and efficient control of the baseband and the analog RF. Timers and mathematical units are also implemented in hardware to allow the CPU to concentrate upon the UWB MAC and PHY functionalities. Boot ROM and ROM Code patching support is provided. Dedicated hardware blocks implement strong cypher functions.

5.4 SR150 Serial Peripheral Interface

The SR150 supports SPI-bus Master/Slave interface, up to 16.66 Mbits/s.

Features

- Data frames of 8-bits and 16bits supported
- Programmable clock polarity and phase
- LSB/MSB first order
- Programmable SSEL polarity

SPI-bus configuration options

In order to select SPI-bus interface for host communication, the host interface choice and settings are programmed during production. The SPI-bus IP supports four operating modes selectable using SPInCfg register The operation mode of the SPI-bus is shown in Table 4, CPHA refers to the Clock Phase option and CPOL refers to the Clock Polarity.

Table 4. SPI-bus configuration

Connection
CPHA switch: Clock Phase: defines the sampling edge of MOSI data • CPHA = 1: data are sampled on MOSI on the even clock edges of SCK after NSS goes low • CPHA = 0: data are sampled on MOSI on the odd clock edges of SCK after NSS goes low
CPOL switch: Clock Polarity • CPOL = 0: the clock is idle low and the first valid edge of SCK will be a rising one • CPOL = 1: the clock is idle high and the first valid edge of SCK will be a falling one

The SPI-bus interface shares the pins with the other host interfaces that are supported by SR150. When SPI-bus is configured the functionality of the interface pins is as described in Table 4.

Table 5. SPI-bus configuration

Pin name	Functionality
Host_1	SCK (Serial input Clock)
Host_2	NSS (Not Slave Select)
Host_3	MOSI (Master Out Slave In)
Host_4	MISO (Master In Slave Out)

SPI-bus functional description

When a master device transmits data to the SR150 via the MOSI line, the SR150 responds by sending data to the master device via the MISO line. This implies full-duplex transmission with both, data out and data in synchronized with the same clock signal.

SR150 starts sampling when receiving a logic low at pins NSS Host_2 pin and the clock at input pin SHOST_1. Thus, SR150 is synchronized with the master. Data from the master is received serially at the slave MOSI line and loaded in the 8-bit shift register. After the 8bit shrift register is loaded, its data is transferred to the read buffer. During a write cycle, data is written into the shift register, then the SR150 waits for a clock train form the master to shift the data out on the MISO line.

Both master and slave devices must operate with the same timing. The master device always places data on the MOSI line a half cycle before the clock edge SCK, for the slave device to latch the data.

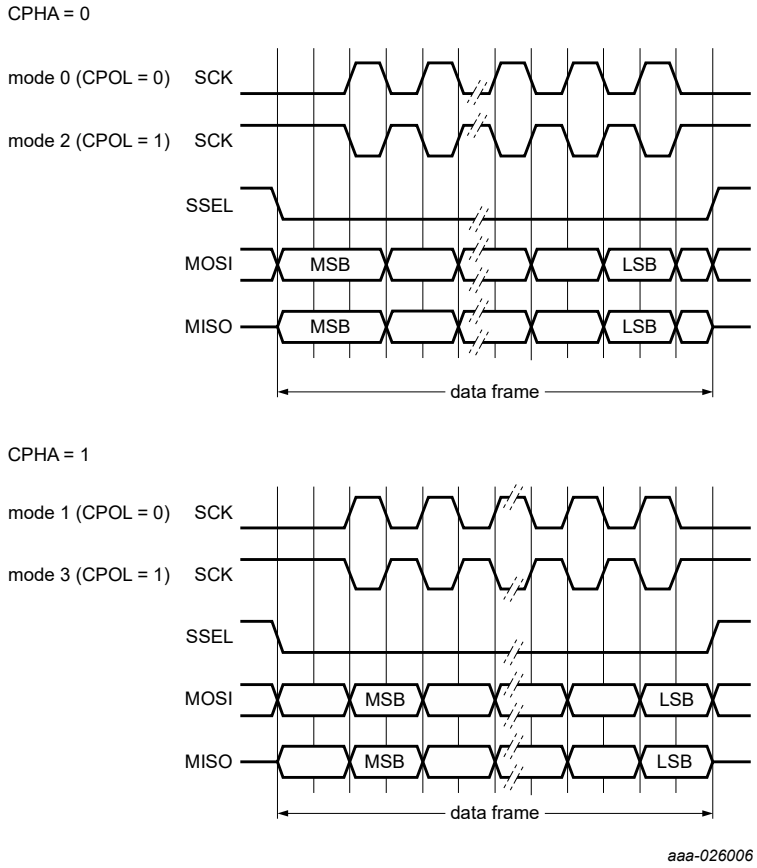

Figure 4. SR150 SPI date frame

5.5 SR150 max output power

SR150 integrated power amplifier delivers power levels that exceed the FCC limits allowing for more than 6 dB application loss due to antenna gain and additional RF passives such as switches and filters.

5.6 SR150 Timing diagrams

SR150 PMU subsystem has a main power up sequence that require VDD_1V8, VDD_RF_1V8,VDD_IO VDDIO_HOST and VCE to be orderly powered to boot-up SR150.

In all cases, host communication with SR150 will only be possible after one defined amount of time from the different supply sequence setup and VCE at rising edge.

High level boot sequence is indicated below, when voltages are settled down CE can be asserted along with VDD_1V8/VDD_RF_1V8 or within 50us, else design will transition to HPD state.

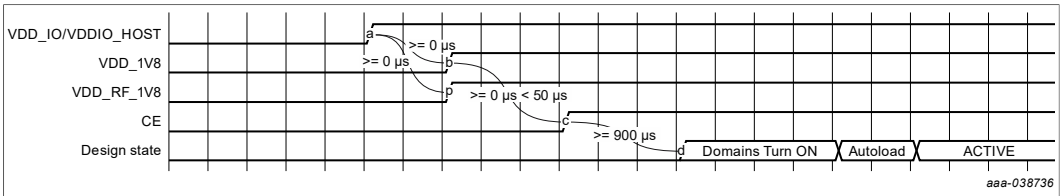

Figure 5. SR150 power up sequence

5.6.1 Deep Power-down (DPD)sequence

In DPD Low power mode CE need to be High all the time, Modem domain needs to be turned OFF before decided to go to DPD. All IOs are retained to same state before going to DPD.All high frequency clocks are turned OFF, XTAL clock can be ON or OFF internal LFO clock will be running all the time. Design has configuration provision to retain ARM and Modem memories.

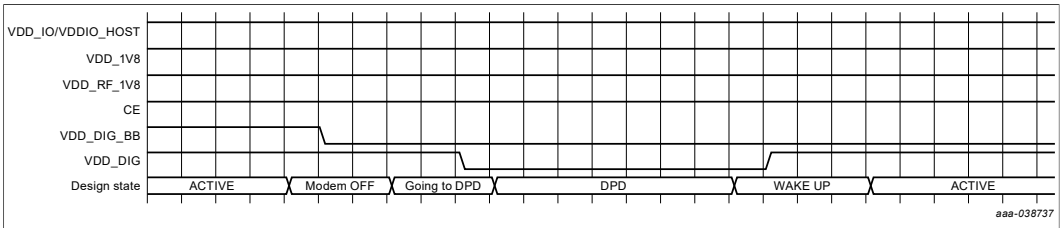

Figure 6. SR150 deep power down sequence

5.6.2 Hard Power-down (HPD) sequence

HPD is lowest Power mode where only Helios AON domain is ON and rest of the power domains are in OFF state. HPD state can be entered or exited only by CE Pin

In HPD state IOs can be kept in known state via OTP or Pad control configuration.

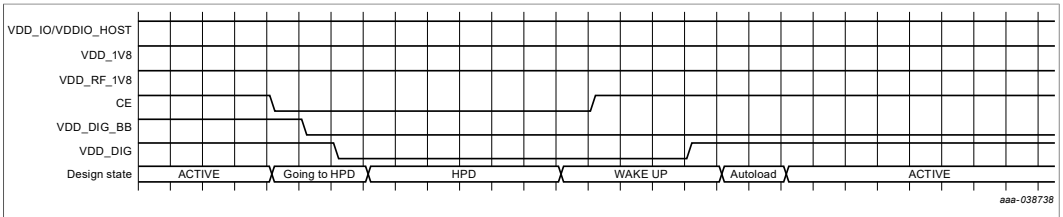

Figure 7. SR150 hard power down sequence

5.6.3 SR150 GPIO

The SR150 GPIOs pullup/pulldown state are configured during the manufacturing phase of SR150, the defaults setting are written in OTP memory. An override state is possible by the firmware. Which only available when firmware is loaded in SR150.

6 Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
VDDIO_HOST	Pad supply voltage for host interface	-	-	2.5	V
VDDIO	Pad supply voltage for other interfaces	-	-	2.5	V
VDD_1V8	Supply voltage for digital domain	-	-	2.5	V
RF_1V8	Supply voltage for RF domain	-	-	2.5	V
PA_1V8	Supply voltage for PA	-	-	2.5	V
$I_{VDD\_1P8\_MAX}$	Digital supplies: Includes the following power pins: VDD_1V8 [C1,D6], VDDIO_HOST [G1], VDDIO – [J5]	All Voltages pins @ 1.8V, @ 85C	-	250	mA
$I_{VDD\_RF\_1P8\_MAX}$	Digital supplies: Includes the following power pins: VDD_RF_1V8 [D6] and VDD_PA [B7]	All Voltages pins @ 1.8V, @ 85C	-	275	mA
$RX_{CHIP\_OFF\_NODAMAGE}$	Max. input level during off mode or HPD power mode	CW signal or other UWB, no damage		7	dBm
VESDH	ESD susceptibility (Human Body Model)	1500 Ω, 100 pF; EIA/JESD22-A114-D	-	2	kV
VESDC	ESD susceptibility (Charge Device model)	field induced model; EIA/JESC22-C101-C, for all IO except RF group	-	1	kV
		RF group IO: RX1_IN, RX2_IN, TX_OUT, VDD_1V8, VIN_RF_1V8, VDD_PA, VSS_TX, VSS_Balun and VSS_PA	-	350	V
Tstg	storage temperature	-	-55	+150	°C
Ptot	total power dissipation	all modes	-	920	mW

7 Recommended operating conditions

Table 7. Operating conditions

Parameter	Conditions	Min	Typ	Max	Unit
Frequency range	Operating frequency Ch5, Ch6, Ch8 and Ch9	6.24	-	8.24	GHz
Operating Temperature	Ambient temperature	--30	+25	+85	°C
Supply Voltage	VDD supply	1.71	1.8	1.98	V
Max. input level	CW signal or other UWB, no damage	-	-	7	dBm
	UWB signal, functional	-	-14	-	dBm
Start-up time	from wake-up or reset release to start of application execution (depends on SPI speed)		500		ms
Maximum allowed operating junction temperature	Maximum junction temperature before SR150 enters into automatic DPD state	-	-	+118	°C
ESD HBM	1500 Ω, 100 pF; EIA/JESD22-A114-D	-	-	2	kV
ESD CDM	field induced model; EIA/JESC22-C101-C, for all IO except RF group	-	-	1	kV
	RF group IO: RX1_IN, RX2_IN, TX_OUT, VDD_1V8, VIN_RF_1V8, VDD_PA, VSS_TX, VSS_Balun and VSS_PA	-	-	350	V

8 Glossary

Table 8. Glossary

Abbreviation	Long term
DPD	Deep Power Down
ESD	ElectroStatic Discharge
HBM	Human Body Model
HPD	Hard Power Down
PLL	Phase Locked Loop
RF	Radio Frequency
RX	Receiver
SHF	Super High Frequency
SPI	Serial Peripheral Interface
STS	Scrambled Timing Sequence
SWD	Serial Wire Debug
TX	Transmitter
UART	Universal Asynchronous Receiver and Transmitter
UWB	Ultra Wideband

9 References

[1] Marcin Poturalski, Manuel Flury, Panos Papadimitratos, Jean-Pierre Hubaux, and Jean-Yves Le Boudec. Distance Bounding with IEEE 802.15.4a: Attacks and Countermeasures. IEEE Transactions on Wireless Communications, Year: 2011, Volume: 10, Issue: 4

[2] Manuel Flury, Marcin Poturalski, Panos Papadimitratos, Jean-Pierre Hubaux, JeanYves Le Boudec. Effectiveness of Distance-Decreasing Attacks Against Impulse Radio Ranging. 3rd ACM Conference on Wireless Network Security, 2010.

[3] Number Generation Using Deterministic Random Bit Generators

10 Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
709010	13 October 2021	Product short data sheet	-	-
Modifications:	• Initial version			

11 Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

11.2 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

11.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

11.4 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Figures

Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 13 October 2021
Document number: 709010