

UJA113xA series

Buck/boost HS-CAN/(dual) LIN system basis chip

Rev. 1 — 28 March 2024

Product data sheet

1 General description

The UJA113xA System Basis Chip (SBC) contains a fully integrated buck and boost converter along with a number of features commonly found in the latest generation of automotive Electronic Control Units (ECUs). It interfaces directly with CAN and LIN bus lines, supplies the microcontroller, handles input and output signals and supports fail-safe features including a watchdog and advanced 'limp home' functionality configurable via non-volatile memory. The UJA113xA is available in number of variants as detailed in [Section 3](#).

To satisfy the demand for SBCs that operate at low battery supply voltages and feature low power dissipation, a switched mode power supply (SMPS) with automatic down (Buck mode) or up conversion (Boost mode) has been integrated into the UJA113xA. In Boost mode, the SMPS of the UJA1131A and UJA1132A variants can continue supplying a microcontroller during dips in the battery voltage, ensuring uninterrupted operation. The boost stage of the UJA1135A and the UJA1136A has limited output current capability, and is suitable for supplying the memory in a microcontroller to prevent information being lost. The SMPS requires only a single external coil and some capacitors but no separate semiconductors.

The UJA113xA implements the standard CAN physical layer as defined in ISO 11898-2:2016. This implementation enables reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s.

The UJA113xAHW/xFx variants support ISO 11898-2:2016 compliant CAN partial networking with a selective wake-up function incorporating CAN FD-passive. CAN FD-passive is a feature that allows CAN FD bus traffic to be ignored in Sleep/Standby mode. CAN FD-passive partial networking is the perfect fit for networks that support both CAN FD and classic CAN communications. It allows normal CAN controllers that do not need to communicate CAN FD messages to remain in partial networking Sleep/Standby mode during CAN FD communication without generating bus errors.

A number of configuration settings are stored in non-volatile memory. This makes it possible to adapt the power-on and limp home behavior of the UJA113xA to meet the specific requirements of an application.



2 Features and benefits

2.1 General

- Generic SBC functions:
 - Fully integrated buck-boost converter
 - 5 V/3.3 V voltage regulator delivering up to 500 mA
 - Separate voltage regulator with optional protection against shorts to battery and loss of module ground
 - CAN transceiver and up to two LIN transceivers
 - Two-channel battery monitoring with integrated A/D converter
 - Watchdog with Window and Timeout modes and on-chip oscillator
 - Serial Peripheral Interface (SPI) for communicating with the microcontroller
 - ECU power management system
 - Protected general-purpose high-voltage I/O pins configurable as high-side drivers (HS), low-side drivers (LS) or wake-up inputs
 - Four internal PWM/pulse timers in derivatives containing high-voltage I/O pins (see [Table 1](#))
- Qualified for use in road vehicles with a nominal 12 V system:
 - Excellent ElectroMagnetic Compatibility (EMC) performance
 - ± 6 kV ElectroStatic Discharge (ESD) protection according to the Human Body Model (HBM) on the CAN/LIN bus pins
 - ± 6 kV ESD protection according to IEC 61000-4-2 on the CAN/LIN bus pins, the sensor supply output (VEXT) and the HVIO pins
 - ± 40 V short-circuit proof CAN/LIN bus pins
 - Battery and CAN/LIN bus pins are protected against transients in accordance with ISO 7637-3
 - Very low-current Standby and Sleep modes with full wake-up capability
- Supports remote flash programming via the CAN-bus
- Compact 10 mm × 10 mm HTQFP48 package with low thermal resistance
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)
- Hardware and software compatible with the UJA113x product family

2.2 Integrated buck and boost converter (SMPS)

- Buck and boost functions with a single external coil:
 - Automatic Buck or Boost mode selection depending on input voltage and output load conditions
 - Boost function allows the UJA1131A and UJA1132A to operate at very low supply voltages (e.g. 2 V; lowest achievable supply voltage depends on output load conditions)
 - Boost function of the UJA1135A and UJA1136A can be used to supply the volatile memory of a microcontroller down to battery voltages as low as 2 V
 - Soft-start function
- The SMPS functions as a pre-regulator for V1 and, optionally, V2:
 - Results in excellent load response at V1 and V2
 - Results in negligible ripple at V1 and V2 outputs
 - Pre-regulator output voltage selectable via the SPI
 - The SMPS can be switched to Pass-through mode to ensure the lowest possible current consumption with immediate full output current capability
- The SMPS can be used to supply external loads directly:
 - e.g. as an energy-efficient supply for an LED chain

2.3 Low-drop voltage regulators (LDOs)

- Main voltage regulator V1:
 - 5 V or 3.3 V nominal output voltage (depending on the selected device)
 - 500 mA output current capability
 - capable of 500 mA transient load current jump in Standby mode
 - Current limiting above 500 mA
 - On-resistance of less than 2 Ω
 - ± 2 % accuracy
 - Undervoltage reset; selectable threshold on the 5 V version: 60 %, 70 %, 80 % or 90 % of nominal value (default detection and release at 90 %)
 - Excellent transient response with a small ceramic output capacitor
 - Short-circuit protection
 - Integrated clamp protects the microcontroller by maintaining the output voltage below 6 V, even when reverse currents of up to 50 mA are injected
 - Turned off in Sleep mode
- Auxiliary voltage regulator V2 with configurable output stage:
 - 5 V nominal output voltage
 - ± 2 % accuracy (± 1.5 % up to 5 mA output current)
 - Excellent transient response with a small ceramic output capacitor
 - Short-circuit protection
 - Current limiting above 100 mA
 - Configurable as supply for on-board loads
 - Configurable as supply for off-board loads ('sensor supply'); protected against shorts to GND and battery; loss-of-ground proof; high ESD robustness

2.4 CAN transceiver

- ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5 compliant high-speed CAN transceiver supporting CAN FD active communication up to 5 Mbit/s in the CAN FD data field
- Autonomous bus biasing according to ISO 11898-2:2016
- CAN-bus connections are truly floating when power to pin BAT is off
- UJA113xAHW/xFx: ISO 11898-2:2016 compliant selective wake-up frame detection
 - No 'false' wake-ups due to CAN FD traffic
 - Bit rates of 50 kbit/s, 100 kbit/s, 125 kbit/s, 250 kbit/s, 500 kbit/s and 1 Mbit/s supported during selective wake-up
- Separate supply pin for flexibility (e.g. can be supplied from V1 or V2)

2.5 LIN transceivers

- One or two channels depending on the selected device
- LIN2.x and ISO 17987-4:2016 (12 V LIN) compliant
- Compliant with SAE J2602
- Downward compatible with LIN 1.3
- Integrated LIN responder termination
- Improved EMC emission performance with optimized curve shaping

2.6 High-voltage I/Os (HVIOs; not available in UJA113xAHW/xF0 variants)

- 4 or 8 general-purpose input/output pins individually configurable as high- or low-side output drivers
 - On/off control via the SPI or by mapping to one of four internal PWM timers
 - Optional direct output on/off control via another HVIO configured as an input (HVIO1 to HVIO4 controlled by HVIO5 to HVIO8 in variants with 8 HVIO pins)
 - PWM timing options include 8-bit dimming up to 250 Hz as well as periodic pulses with variable length and variable repetition rate; e.g. for cyclic contact monitoring
 - On-resistance less than 24 Ω
 - Two or more HVIOs can be combined to form a single output with increased driver capability
 - Combined into one or two banks of four HVIOs with individual supply pins for each bank; the banks can be supplied independently from the battery ($\cong 12$ V), the SMPS ($\cong 6$ V) or V1/V2 (5 V)
 - Reverse-current protection of the output in Off mode (loss-of-ground and loss-of-battery proof)
 - Open-load diagnostics and short-circuit protection and diagnostics
 - Can be configured individually to shut down in response to a battery supply undervoltage and/or overvoltage
- Individually configurable as inputs with wake-up capability
 - Selectable wake-up edge
 - Selectable wake-up threshold: ratiometric to HVIO supply pin or absolute level
 - Wake-up threshold tolerates ground offsets of up to 2.5 V
 - Wake-up source reporting via SPI
 - Continuous or periodic input level sampling; timing can be synchronized with another HVIO pin configured as an output driver for cyclic contact monitoring
- Three HVIOs can be configured individually as limp-home outputs
 - HVIO2 as static high-side driver limp-home signal
 - HVIO3 as 100 Hz, 10 % duty cycle limp-home signal
 - HVIO4 as 1.25 Hz, 50 % duty cycle limp-home signal

2.7 A/D converter for monitoring the battery voltage

- 10-bit resolution, accurate to ± 300 mV at 20 V full scale
- Two channels:
 - Measures the voltage level on pin BAT or pin BATSENSE
 - Measures the battery voltage on either side of a polarity protection diode connected to pin BATSENSE via a series resistor
- Continuous measurement on both channels
- Optional software interrupt and/or shutdown of functions when measured supply voltage is outside a defined range (undervoltage and overvoltage detection)

2.8 Power management

- Wake-up via CAN, LIN or HVIO pins with wake-up source recognition
- HVIO wake input functionality can be disabled to reduce current consumption
- Cyclic output signal for biasing various wake-up applications with selectable period and configurable on-time
- Cyclic wake-up with selectable period
- Standby mode featuring very low supply current with V1 active to maintain supply to the microcontroller
- Sleep mode featuring very low supply current with V1 off
- Sleep mode option can be disabled via non-volatile memory

2.9 System control and diagnostic features

- Watchdog that can operate in Window, Timeout (with optional cyclic wake-up) and Off Modes (with automatic re-enable if an interrupt is generated)
- Watchdog period selectable between 8 ms and 4 s
- 16-, 24- or 32-bit SPI for configuration, control and diagnosis
- 2 Interrupt output pins - one for high- and low-priority interrupts, one for high-priority interrupts; interrupts can be enabled individually:
 - V1 and V2/VEXT undervoltage; V2/VEXT overvoltage; battery over- and undervoltage; CAN, LIN and local wake-up (HVIO); CAN and HVIO diagnostics; overtemperature warning; cyclic wake-up; SPI failure
- Bidirectional reset pin with selectable reset length to support various microcontrollers; triggered, for example, by a watchdog overflow or by a V1 undervoltage event
- Limp-home output (LIMP) for activating application-specific 'limp-home' hardware in the event of a serious system malfunction
- Configuration information for selected functions stored in non-volatile memory
- Enable output (EN) for controlling safety-critical hardware; e.g. shut-down if the microcontroller fails
- Overtemperature warning and shut-down

3 Product family overview

Table 1. Feature overview of UJA113xA SBC family

	Buck/high-current boost SMPS	Buck/low-current boost SMPS	V1 LDO 5 V, 500 mA	V1 LDO 3.3 V, 500 mA	V2/VEXT LDO 5 V 100 mA	CAN FD transceiver up to 5 Mbit/s	CAN partial networking; CAN FD passive	1 x LIN transceiver	2 x LIN transceivers	4 x HVIOs: HS/LS driver or WAKE input	8 x HVIOs: HS/LS driver or WAKE input	4 x timers for HVIO control	Battery monitoring	Watchdog	LIMP pin	Advanced LIMP function	SPI interface	Reset input/output	EN pin for controlling critical hardware	Mode control: Normal, Standby, Sleep	Overtemperature warning and shutdown	HTQFP48 package
UJA1131AHW/5	•		•		•	•		•			•	•	•	•	•	•	•	•	•	•	•	•
UJA1131AHW/3	•			•	•	•		•			•	•	•	•	•	•	•	•	•	•	•	•
UJA1132AHW/5	•		•		•	•			•		•	•	•	•	•	•	•	•	•	•	•	•
UJA1132AHW/3	•			•	•	•			•		•	•	•	•	•	•	•	•	•	•	•	•
UJA1135AHW/5		•	•		•	•		•			•	•	•	•	•	•	•	•	•	•	•	•
UJA1135AHW/3		•		•	•	•		•			•	•	•	•	•	•	•	•	•	•	•	•
UJA1136AHW/5		•	•		•	•			•		•	•	•	•	•	•	•	•	•	•	•	•
UJA1136AHW/3		•		•	•	•			•		•	•	•	•	•	•	•	•	•	•	•	•
UJA1131AHW/5F4	•		•		•	•	•	•		•		•	•	•	•	•	•	•	•	•	•	•
UJA1131AHW/3F4	•			•	•	•	•	•		•		•	•	•	•	•	•	•	•	•	•	•
UJA1131AHW/5F0	•		•		•	•	•	•					•	•	•		•	•	•	•	•	•
UJA1131AHW/3F0	•			•	•	•	•	•					•	•	•		•	•	•	•	•	•
UJA1132AHW/5F4	•		•		•	•	•		•	•		•	•	•	•	•	•	•	•	•	•	•
UJA1132AHW/3F4	•			•	•	•	•		•	•		•	•	•	•	•	•	•	•	•	•	•
UJA1132AHW/5F0	•		•		•	•	•		•				•	•	•		•	•	•	•	•	•
UJA1132AHW/3F0	•			•	•	•	•		•				•	•	•		•	•	•	•	•	•

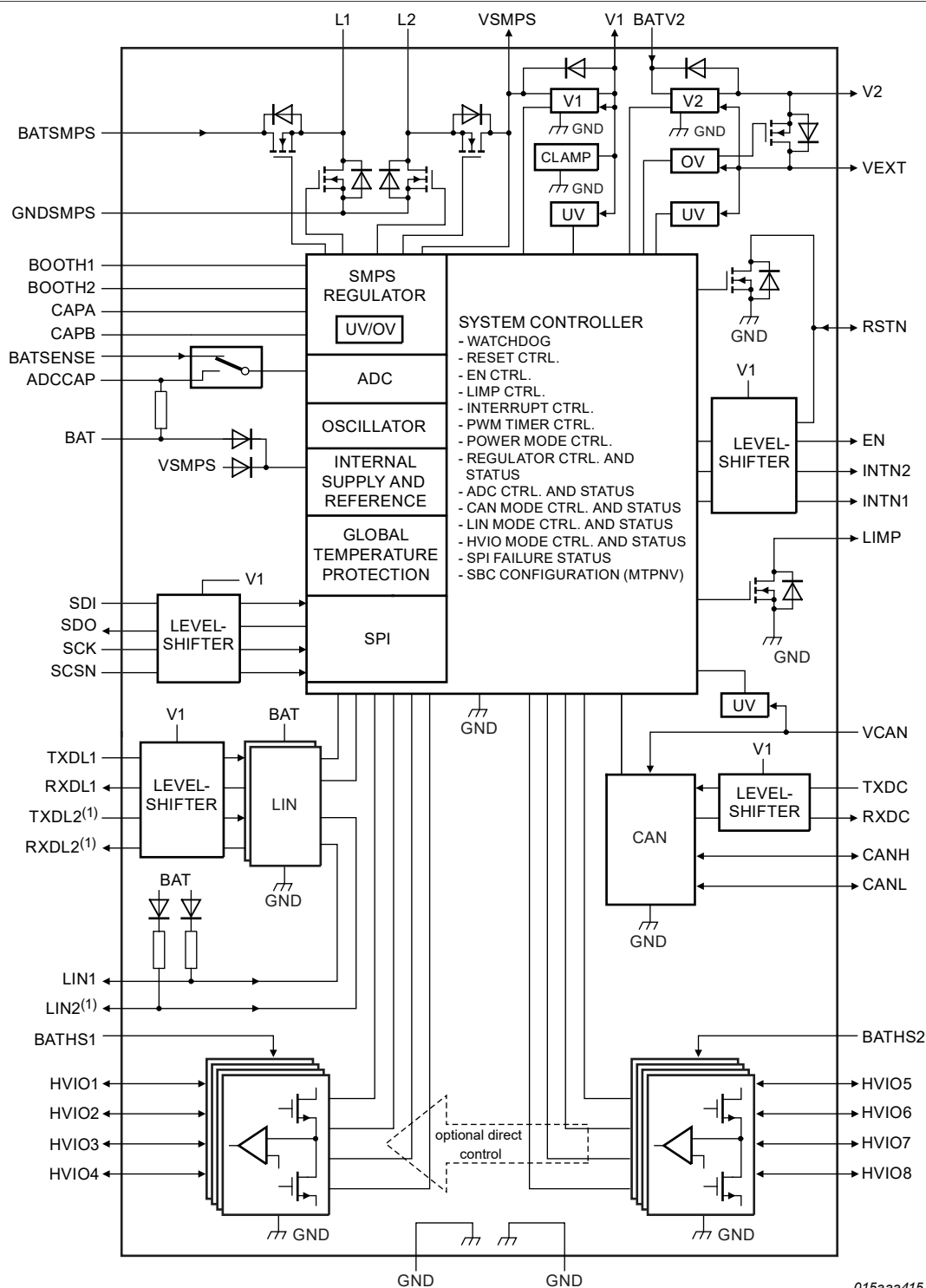
4 Ordering information

Table 2. Ordering information

Type number ^[1]	Package		
	Name	Description	Version
UJA1131AHW/5	HTQFP48	plastic thermal enhanced thin quad flat package; 48 leads; body 10 x 10 x 1.0 mm; exposed die pad	SOT1181-2
UJA1131AHW/3			
UJA1132AHW/5			
UJA1132AHW/3			
UJA1135AHW/5			
UJA1135AHW/3			
UJA1136AHW/5			
UJA1136AHW/3			
UJA1131AHW/5F4			
UJA1131AHW/3F4			
UJA1131AHW/5F0			
UJA1131AHW/3F0			
UJA1132AHW/5F4			
UJA1132AHW/3F4			
UJA1132AHW/5F0			
UJA1132AHW/3F0			

[1] UJA113xAHW/5x variants contain a 5 V regulator (V1); UJA113xAHW/3x variants contain a 3.3 V regulator (V1); UJA113xAHW/xFx variants support CAN partial networking.

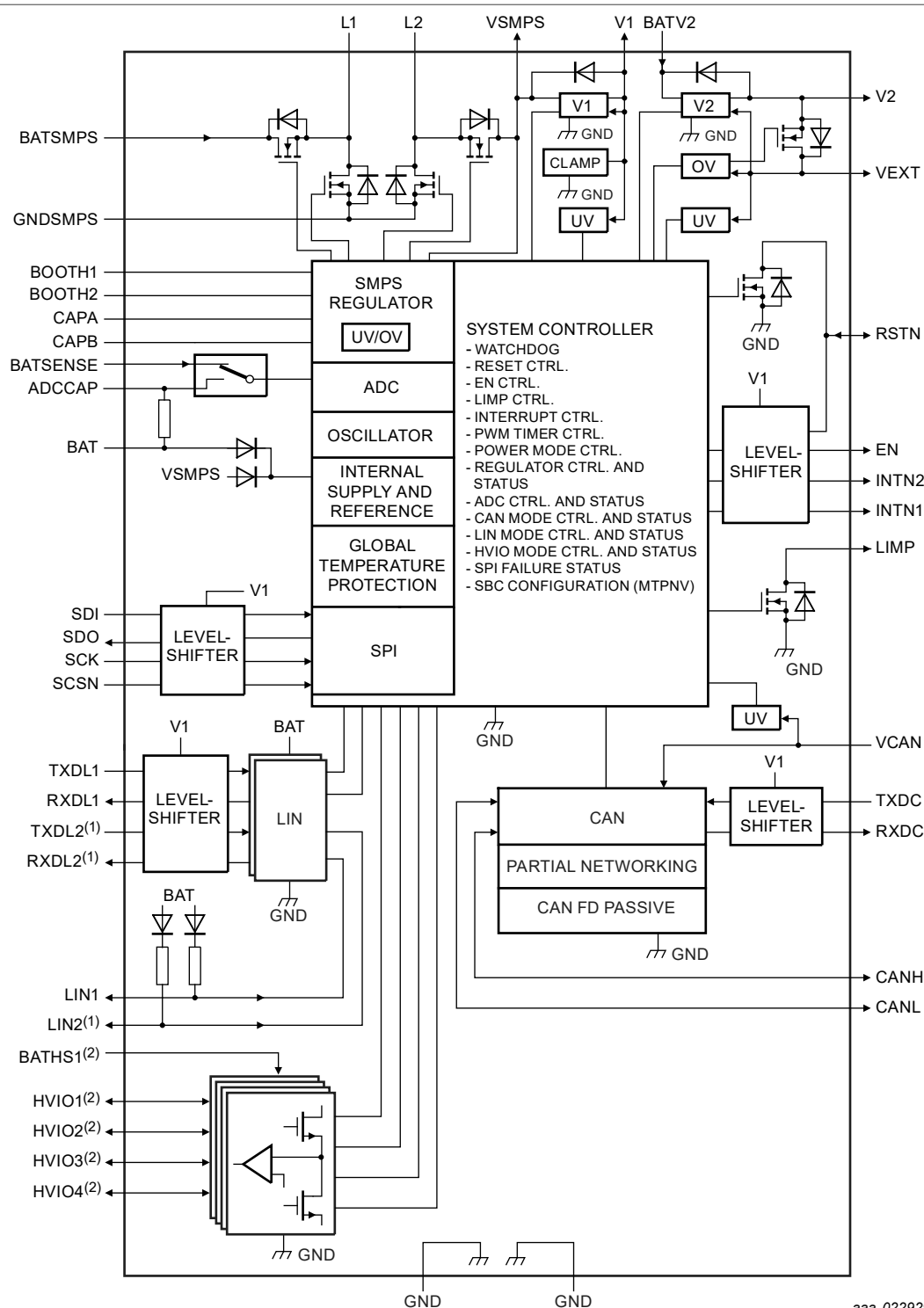
5 Block diagram



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1. UJA1132A and UJA1136A only

Figure 1. Block diagram of UJA113xA variants without partial networking



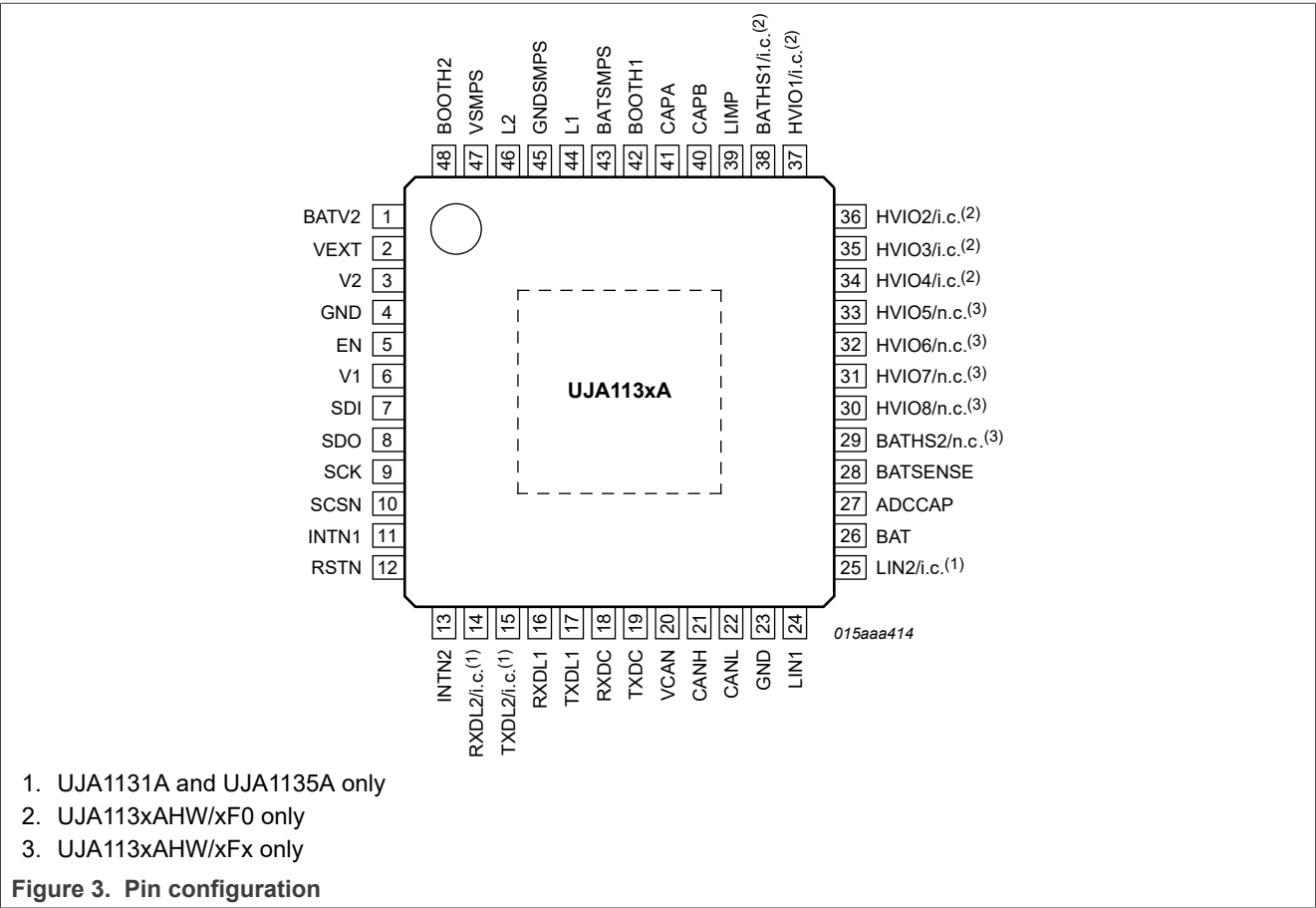
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1. UJA1132AHW/xFx
2. UJA113xAHW/xF4

Figure 2. Block diagram of UJA113xAHW/xFx variants featuring CAN partial networking

6 Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type ^[1]	Description
BATV2	1	P	supply input for V2 regulator
VEXT	2	AO	protected output of voltage regulator V2 ('sensor supply')
V2	3	AIO	protection selection for voltage regulator V2: leave pin unconnected for a protected LDO with output at VEXT; connect to pin VEXT for an unprotected LDO with lower drop-out
GND ^[2]	4	G	ground
EN	5	O	enable output
V1	6	AO	voltage regulator output for the microcontroller (5 V or 3.3 V depending on SBC version)
SDI	7	I	SPI data input
SDO	8	O	SPI data output
SCK	9	I	SPI clock input
SCSN	10	I	SPI chip select input

Table 3. Pin description...continued

Symbol	Pin	Type ^[1]	Description
INTN1	11	O	interrupt output 1 to the microcontroller (triggered by all interrupts)
RSTN	12	IO	reset input/output to and from the microcontroller; referenced to V1 (see Section 7.3.1)
INTN2	13	O	interrupt output 2 to the microcontroller (triggered by high-priority interrupts)
RXDL2/i.c.	14	O	LIN2 receive data output; internally connected and should be left open in UJA1131A and UJA1135A
TXDL2/i.c.	15	I	LIN2 transmit data input; internally connected and should be left open in UJA1131A and UJA1135A
RXDL1	16	O	LIN1 receive data output
TXDL1	17	I	LIN1 transmit data input
RXDC	18	O	CAN receive data output
TXDC	19	I	CAN transmit data input
VCAN	20	P	5 V supply input for the integrated HS-CAN transceiver
CANH	21	AIO	CANH bus line
CANL	22	AIO	CANL bus line
GND ^[2]	23	G	ground
LIN1	24	AIO	LIN bus line 1
LIN2/i.c.	25	AIO	LIN bus line 2; internally connected and should be left open in UJA1131A and UJA1135A
BAT	26	P	12 V battery supply for the LIN transceiver; input source 0 for battery A/D converter
ADCCAP	27	AIO	connection for A/D converter source 0 input filter capacitor
BATSENSE	28	AI	battery A/D converter source 1 input
BATHS2/n.c.	29	P	battery supply input for HVIO 5, 6, 7 and 8 (bank 1); not connected in UJA113xAHW/xFx
HVIO8/n.c.	30	AIO	high voltage input/output 8; not connected in UJA113xAHW/xFx
HVIO7/n.c.	31	AIO	high voltage input/output 7; not connected in UJA113xAHW/xFx
HVIO6/n.c.	32	AIO	high voltage input/output 6; not connected in UJA113xAHW/xFx
HVIO5/n.c.	33	AIO	high voltage input/output 5; not connected in UJA113xAHW/xFx
HVIO4/i.c.	34	AIO	high voltage input/output 4; internally connected in UJA113xAHW/xF0
HVIO3/i.c.	35	AIO	high voltage input/output 3; internally connected in UJA113xAHW/xF0
HVIO2/i.c.	36	AIO	high voltage input/output 2; internally connected in UJA113xAHW/xF0
HVIO1/i.c.	37	AIO	high voltage input/output 1; internally connected in UJA113xAHW/xF0
BATHS1/i.c.	38	P	battery supply input for HVIO 1, 2, 3 and 4 (bank 0); internally connected and should be left open in UJA113xAHW/xF0
LIMP	39	AO	limp home output
CAPB	40	AIO	terminal B for SMPS bootstrap capacitor
CAPA	41	AIO	terminal A for SMPS bootstrap capacitor
BOOTH1	42	AIO	terminal for bootstrap capacitor 1 (connected between BOOTH1 and L1)
BATSMPS	43	P	12 V battery supply input for SMPS
L1	44	AIO	SMPS coil terminal 1

Table 3. Pin description...continued

Symbol	Pin	Type ^[1]	Description
GNDSMPS	45	G	ground connection for SMPS
L2	46	AIO	SMPS coil terminal 2
VSMPS	47	AO	SMPS output voltage
BOOTH2	48	AIO	terminal for bootstrap capacitor 2 (connected between BOOTH2 and L2)

[1] I: digital input; O: digital output; IO: digital input/output; AI: analog input; AO: analog output; AIO: analog input/output; P: power supply; G: ground.
[2] The exposed die pad at the bottom of the package allows for better heat dissipation from the SBC via the printed-circuit board. It is internally connected to GND (pins 4, 23) and must be connected to ground on the PCB.

7 Functional description

7.1 System Controller

The system controller manages register configuration and controls the internal functions of the SBC. Detailed device status information is collected and made available to the microcontroller. The system controller also generates reset and interrupt signals.

7.1.1 Operating modes

The system controller is a state machine. SBC operating modes and state transitions are illustrated in [Figure 4](#).

7.1.1.1 Off mode

The UJA113xA switches to Off mode when the battery supply voltage is too low to power the SBC. When the battery is initially connected, the UJA113xA powers up in Off mode. As soon as the battery supply rises above the power-on detection threshold ($V_{th(det)pon}$), the SBC executes a system reset and enters Standby mode (for exceptions, see [Section 7.1.3](#)). It switches automatically to Off mode from all other modes if the battery supply voltage and the SMPS output voltage fall below the power-off threshold ($V_{th(det)poff}$). In Off mode, the voltage regulators are disabled and the CAN and LIN bus systems are in a high-resistive state.

7.1.1.2 Standby mode

Standby mode is a low-power mode in which regulator V1 is switched on. The SBC switches to Standby mode from Reset mode when the reset event has been processed successfully and pin RSTN has been switched HIGH again. Standby mode can also be selected from Normal mode via an SPI command (MC = 100; see [Table 4](#)). The SBC exits Standby mode if:

- Normal or Sleep mode is selected via an SPI command
- a reset event is generated
- the global chip temperature rises above the OverTemperature Protection (OTP) activation threshold, $T_{th(act)otp}$, causing the SBC to enter Overload mode
- the battery voltage rises above the overvoltage detection threshold ($V_{th(det)ov}$), causing the SBC to enter Overload mode
- the battery supply voltage and the SMPS output voltage fall below the power-off threshold ($V_{th(det)poff}$), causing the SBC to switch to Off mode

7.1.1.3 Normal mode

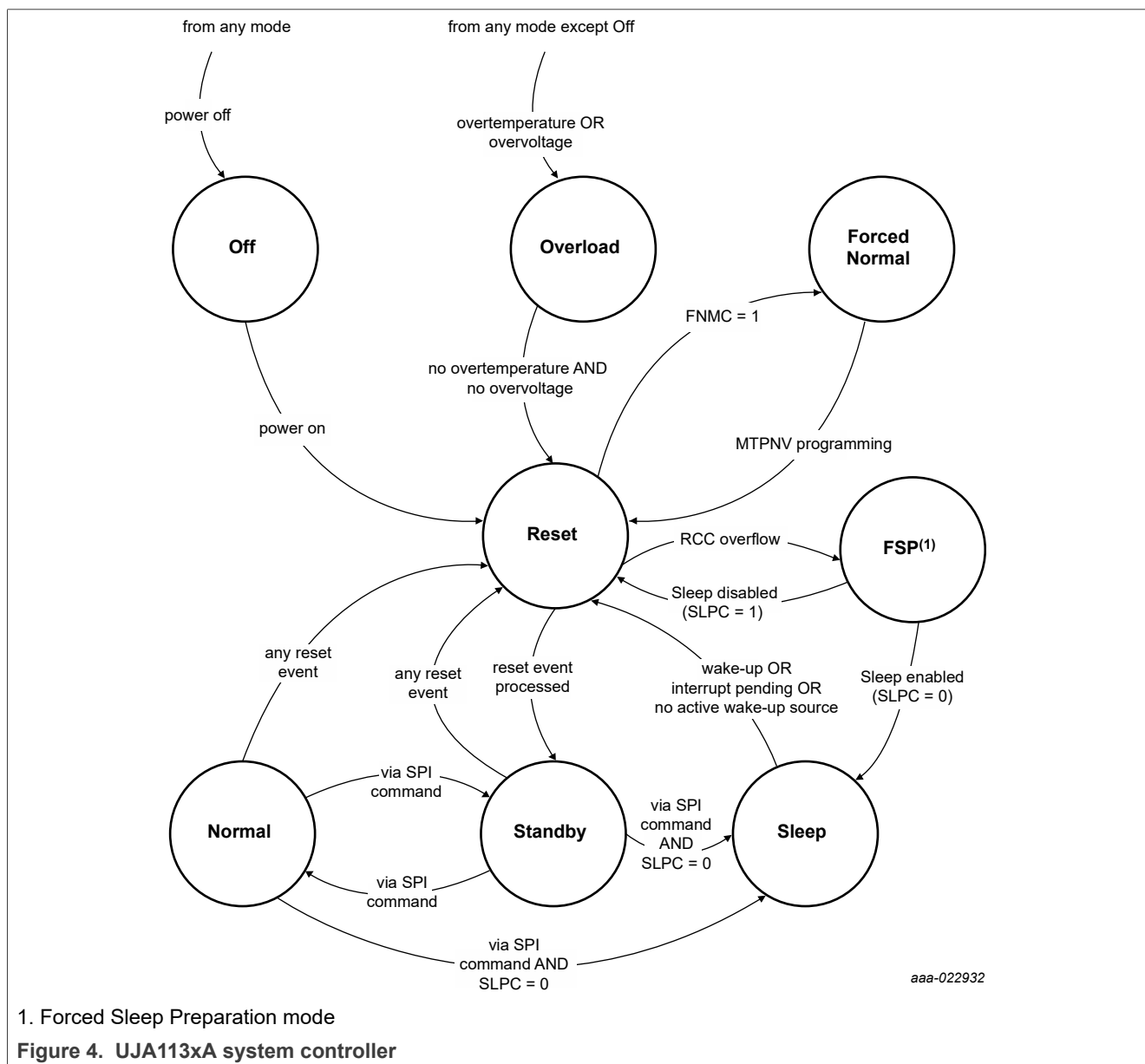
Normal mode is the active SBC operating mode. In this mode, the SBC is fully operational and all onboard hardware can be activated.

Normal mode can be selected from Standby mode via an SPI command (MC = 111).

The SBC immediately exits Normal mode if:

- a reset event is triggered
- Standby or Sleep mode is selected via the SPI (MC = 100 or MC = 001)
- the device is forced to [Off](#) or [Overload](#) mode

Remark: When the UJA113xA enters Normal mode, the following features are activated after a short delay ($t_{d(act)norm}$; see [Table 105](#)): CAN and LIN transceivers, battery monitoring, HVIO low side drivers.



7.1.1.4 Sleep mode

Sleep mode is a low-power mode similar to Standby mode. However, V1 is switched off in Sleep mode.

Sleep mode is selected from Normal or Standby mode via an SPI command (MC = 001). The SBC switches to Sleep mode when this command is received, provided there are no pending interrupts or wake-up events and at least one regular wake-up source is enabled (see [Section 7.12.2](#)). Any attempt to enter Sleep mode while one of these conditions has not been met will trigger a system reset and set the reset source status bits (RSS) to 10100 ('illegal Sleep mode command received'; see [Table 5](#)).

Sleep mode can be deactivated by setting the Sleep control bit (SLPC) in the SBC configuration register to 1 (see [Table 11](#)). This register is located in the non-volatile memory area of the device. When this bit is set to 1, the Sleep mode command is ignored. No other SBC functions are affected.

If the reset counter overflows when the SBC is in Reset mode, it switches to Forced Sleep Preparation (FSP) mode. The reset counter is cleared and limp home activated in FSP mode. The SBC then switches automatically to Sleep mode, provided SLPC = 0 (if SLPC = 1, it returns to Reset mode).

Since V1 is off in Sleep mode, the only way the SBC can exit Sleep mode is via a wake-up event. This can be a regular or a diagnostic wake-up event (see [Section 7.12](#)).

7.1.1.5 Overload mode

Overload mode is provided to prevent the device being damaged in critical situations.

The SBC switches to Overload mode:

- from any mode other than Off mode as soon as the global chip temperature rises above the overtemperature protection activation threshold, $T_{th(otp)}$
- after the overvoltage shutdown delay time, $t_{d(sd)ov}$, if the battery voltage has been above the overvoltage detection threshold ($V_{th(det)ov}$) for longer than the overvoltage detection time, $t_{det(ov)}$ (see [Section 7.7.3](#))

The SBC generates overtemperature and overvoltage shutdown warning interrupts to help prevent the loss of data in the microcontroller memory in the event of a critical overtemperature/overload event (see [Section 7.6](#) and [Section 7.7.3](#)).

In Overload mode, the voltage regulators are switched off, pin RSTN is driven LOW and the limp home control bit, LHC, is set to 1 so that the LIMP pin is driven LOW (see [Section 7.5](#)). In addition, the SMPS is off, the bus systems are in a high-resistive state and the HVIOs are in a fail-safe state (see [Section 7.10.4](#)).

The SBC exits Overload mode when,

- the event that triggered the transition to Overload has been reversed (i.e. the global chip temperature has fallen back below $T_{th(rel)otp}$ and/or V_{BAT} has fallen back below $V_{th(rel)ov}$) and no new condition that would trigger a transition to Overload has been detected
- the device is forced to Off mode (supply voltage < $V_{th(det)poff}$)

After leaving Overload mode, the SBC generates a system reset and enters Standby mode.

7.1.1.6 Reset mode

The SBC switches to Reset mode in response to a reset event (see [Section 7.3.3](#)). This ensures that pin RSTN is pulled down for a defined period to allow the microcontroller to start up in a controlled manner. In addition, Reset mode provides a number of fail-safe features including a reset counter and a reset time-out (see [Section 7.3](#)).

The SBC exits Reset mode if:

- the device is forced to Off or Overload mode

- the reset event has been processed and pin RSTN has been switched HIGH again; the SBC then switches to Standby mode
- the reset count causes the SBC to switch to FSP mode

7.1.1.7 Forced Sleep Preparation (FSP) mode

FSP mode is an intermediate state that is activated in the event of a serious system failure.

The SBC switches to FSP mode from Reset mode when the reset counter overflows or if RCC = 3 on entering Reset mode (see [Section 7.3](#)). In FSP mode, all control settings are reset to safe values to avoid deadlocks and to ensure that the system starts up correctly once the failure condition has been eliminated. All pending interrupts are cleared and all regular interrupt sources are activated (see [Table 81](#)). In addition, bit LHC bit is set to 1 to activate the limp home function (see [Table 16](#)). The SBC then returns to Reset mode if Sleep mode is disabled (SLPC = 1). Otherwise, it switches to Sleep mode.

7.1.1.8 Forced Normal mode

Forced Normal mode is a test mode intended for initial prototyping and device evaluation in the laboratory. It simplifies SBC testing, is useful for failure detection and can be used for first factory flashing of the microcontroller during production.

The CAN and LIN transceivers, the SMPS, V1 and V2 are on in Forced Normal mode. The HVIOs and the watchdog are disabled and there is limited access to the SPI registers. Only the Main status register (address 0x03), the Watchdog status register (address 0x05), the Identification registers (addresses 0x7E and 0x7F) and the registers in non-volatile memory (addresses 0x70 and 0x75) can be read. The non-volatile memory can be reprogrammed provided the SBC is in the factory preset state (see [Section 7.13](#) for details).

The SBC switches to Forced Normal mode after power-on if bit FNMC in the SBC configuration control register ([Table 11](#)) is set to 1. After the initial power-on reset sequence has been completed, system reset is disabled. So the SBC cannot force a reset and will not react to external reset events.

The SBC exits Forced Normal mode if:

- the non-volatile memory is (re-)programmed
- the SBC switches to Overload or Off mode

A system reset is performed when the SBC exits Forced Normal mode.

7.1.2 System control and status registers

The operating mode is selected via bits MC in the Mode control register. The Mode control register is accessed via SPI address 0x01 (see also [Section 7.16.4](#)).

Table 4. Mode control register (address 01h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R/W	-	always write 00000; ignore on read
2:0	MC	R/W	001	Sleep mode
			100	Standby mode
			111	Normal mode

The Main SBC status register can be accessed to monitor the status of the overtemperature warning flag and to determine whether the SBC has entered Normal mode after power-up. It also indicates the source of the most recent reset event.

Table 5. Main SBC status register (address 03h)

Bit	Symbol	Access	Value	Description
7	reserved	R	-	ignore on read
6	OTWS	R	0	IC temperature below overtemperature warning threshold
			1	IC temperature above overtemperature warning threshold
5	NMS	R	0	SBC has been in Normal mode at least once (after leaving Off mode)
			1	SBC powered up but has not yet switched to Normal mode
4:0	RSS	R		source of most recent reset event:
			00000	exited Off mode (power-on)
			00001	CAN wake-up detected in Sleep mode
			00010	LIN1 wake-up detected in Sleep mode
			00011	LIN2 wake-up detected in Sleep mode (if LIN2 is available)
			00100	HVIO1 wake-up detected in Sleep mode (if dedicated HVIO is available)
			00101	HVIO2 wake-up detected in Sleep mode (if dedicated HVIO is available)
			00110	HVIO3 wake-up detected in Sleep mode (if dedicated HVIO is available)
			00111	HVIO4 wake-up detected in Sleep mode (if dedicated HVIO is available)
			01000	HVIO5 wake-up detected in Sleep mode (if dedicated HVIO is available)
			01001	HVIO6 wake-up detected in Sleep mode (if dedicated HVIO is available)
			01010	HVIO7 wake-up detected in Sleep mode (if dedicated HVIO is available)
			01011	HVIO8 wake-up detected in Sleep mode (if dedicated HVIO is available)
			01100	watchdog overflow in Sleep mode
			01101	diagnostic wake-up in Sleep mode
			01110	watchdog triggered too early
			01111	watchdog overflow
			10000	illegal watchdog mode control access
			10001	RSTN pulled down externally

Table 5. Main SBC status register (address 03h)...continued

Bit	Symbol	Access	Value	Description
			10010	leaving Overload mode
			10011	V1 undervoltage event
			10100	illegal Sleep mode command received
			10101	wake-up after leaving FSP mode

An interrupt status bit is associated with each interrupt source. The system interrupt status bits are located in the System interrupt status register, [Table 6](#).

The interrupt mechanism is described in [Section 7.12](#).

Table 6. System interrupt status register (address 61h)

Bit	Symbol	Access	Value	Description
7:6	reserved	R/W	-	always write 00; ignore on read
5	OVSDI ^[1]	R/W	0	no overvoltage shut-down interrupt pending
			1	overvoltage shut-down interrupt pending
4	POSI ^[1]	R/W	0	no power-on status interrupt pending
			1	power-on status interrupt pending
3	reserved	R/W	-	always write 0; ignore on read
2	OTWI	R/W	0	no overtemperature warning interrupt pending
			1	overtemperature warning interrupt pending
1	SPIFI	R/W	0	no SPI failure interrupt pending
			1	SPI failure interrupt pending
0	WDI ^[1]	R/W	0	no watchdog failure interrupt pending
			1	watchdog failure interrupt pending

[1] Interrupt always enabled.

System interrupts are enabled/disabled via the System interrupt enable register, [Table 7](#).

Table 7. System interrupt enable register (address 04h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R/W	-	always write 00000; ignore on read
2	OTWIE	R/W	0	overtemperature warning interrupt disabled
			1	overtemperature warning interrupt enabled
1	SPIFIE	R/W	0	SPI failure interrupt disabled
			1	SPI failure interrupt enabled
0	reserved	R/W	-	always write 0; ignore on read

System control and status bit values, when predictable according to the SBC operating mode, are given in [Table 8](#). Bits SPIFI and SPIFIE are not included here; they can be found in [Table 93](#) in [Section 7.16.3](#). Bits RSS can be found in [Table 15](#) in [Section 7.3.3](#).

Control/configuration bits (writable via SPI) and interrupt bits are (re-)initialized to the default values for the SBC mode. For status bits, the expected value for the SBC mode is indicated.

Table 8. Influence of SBC operating modes on system control and status registers

Bit(s)	Off (power-on default)	Forced Normal	Standby	Normal	Sleep	Reset	Overload	FSP
MC	100	[1]	100	111	001	100	100	001 if SLPC = 0
NMS	1	1	-	0	-	-	-	-
OTWI	0	[1]	-	-	-	-	-	0
OTWIE	0	[1]	-	-	-	-	-	0
OTWS	0	-	-	-	-	-	-	-
OVSDI	0	[1]	-	-	-	-	-	0
POSI	1	[1]	-	-	-	-	-	0
SLPC	located in one of the non-volatile configuration registers (see Section 7.13)							

[1] Register not accessible; reading returns 0.

7.1.3 Exceptional start-up behavior

If V_{BAT} ramps up from 3 V to 5.5 V in less than 0.25 ms, the system controller may not start up if, after ramping up, V_{BAT} is between 5.5 V and 7.7 V. The device will be off (Off mode), even though V_{BAT} has risen above $V_{th(det)pon}$. It will remain off until V_{BAT} exits this voltage window, when it will start up as described in [Section 7.1.1](#) and [Section 7.7.1](#). See also application note AN13928.

Once running, the system controller remains active until the voltage on both the BAT and VSMPs pins falls below the power off detection threshold $V_{th(det)poff}$.

7.2 Watchdog

The UJA113xA contains a watchdog that supports three operating modes: Window, Timeout and Autonomous. In Window mode (available only in SBC Normal mode), a watchdog trigger event within a closed watchdog window resets the watchdog timer. In Timeout mode, the watchdog runs continuously and can be reset at any time within the time-out time by a watchdog trigger. Watchdog Timeout mode can also be used for cyclic wake-up of the microcontroller. In Autonomous mode, the watchdog can be off or in Timeout mode (see [Section 7.2.2](#) to [Section 7.2.4](#) for further details).

The watchdog mode and watchdog period are selected via the Watchdog control register ([Table 9](#)) and can only be changed when the SBC is in Standby mode.

The watchdog mode is selected via bits WMC. If Window mode is selected (WMC = 100), the watchdog remains in (or switches to) Timeout mode until the SBC enters Normal mode. Any attempt to change the watchdog operating mode (via WMC) while the SBC is in Normal mode will cause the UJA113xA to switch to Reset mode and the reset source status bits (RSS) will be set to 10000 ('illegal watchdog mode control access'; see [Table 5](#)).

Eight watchdog periods are supported, from 8 ms to 4096 ms. The watchdog period is programmed via bits NWP. The selected period is valid for both Window and Timeout modes. The default watchdog period is 128 ms.

A watchdog trigger event resets the watchdog timer. A watchdog trigger event is any valid write access to the Watchdog control register. If the watchdog mode or the watchdog period have changed as a result of the write access, the new values are valid immediately.

Table 9. Watchdog control register (address 00h)

Bit	Symbol	Access	Value	Description
7:5	WMC	R/W		watchdog mode control:
			001 ^[1]	Autonomous mode
			010 ^[2]	Timeout mode
			100 ^[3]	Window mode
4	reserved	R/W	-	always write 0; ignore on read
3:0	NWP	R/W		nominal watchdog period
			1000	8 ms
			0001	16 ms
			0010	32 ms
			1011	64 ms
			0100 ^[2]	128 ms
			1101	256 ms
			1110	1024 ms
			0111	4096 ms

[1] Default value if SDMC = 1 (see [Section 7.2.1](#))

[2] Default value.

[3] Selected in Standby mode but only activated when the SBC switches to Normal mode.

The watchdog is a valuable safety mechanism, so it is critical that it is configured correctly. Two features are provided to prevent watchdog parameters being changed by mistake:

- redundant states associated with configuration bits WMC and NWP
- reconfiguration protection in Normal mode

Redundant states associated with control bits WMC and NWP ensure that a single bit error cannot cause the watchdog to be configured incorrectly (at least 2 bits must be changed to reconfigure WMC or NWP). If an attempt is made to write an invalid code to WMC or NWP (e.g. 011 or 1001 respectively), the SPI operation is abandoned and an SPI failure interrupt is generated, if enabled (see [Section 7.12](#)).

Two operating modes have a major impact on the operation of the watchdog: Forced Normal mode and Software Development mode (Software Development mode is provided for test purposes and is not an SBC operating mode; the UJA113xA can be in any mode with Software Development mode enabled; see [Section 7.2.1](#)). These modes are enabled and disabled via bits FNMC and SDMC respectively in the SBC configuration control register (see [Table 11](#)). This register is located in the non-volatile memory area (see [Section 7.13](#)). In Forced Normal mode (FNM), the watchdog is disabled. In Software Development mode (SDM), the watchdog can be disabled or activated for test purposes.

Information on the status of the watchdog is available from the Watchdog status register ([Table 12](#)). This register also indicates whether Forced Normal and Software Development modes are active.

Table 10. Summary of watchdog settings

System controller state	Watchdog configuration			
	SDMC = x	SDMC = x	SDMC = 0	SDMC = 1
	WMC = 100 (Window)	WMC = 010 ^[1] (Timeout)	WMC = 001 (Autonomous)	WMC = 001 ^[2] (Autonomous)
Normal mode	Window	Timeout	Timeout	off

Table 10. Summary of watchdog settings...continued

System controller state	Watchdog configuration			
Standby mode (INTN1 HIGH)	Timeout	Timeout	off	off
Standby mode (INTN1 LOW)	Timeout	Timeout	Timeout	off
Sleep mode	Timeout	Timeout	off	off
Forced Normal mode	off	off	off	off
Other modes	off	off	off	off

[1] Default value if SDMC = 0

[2] Default value if SDMC = 1

Table 11. SBC configuration control register (address 74h)

This table is located in non-volatile memory with restricted write access.

Bit	Symbol	Access	Value	Description
7:6	reserved	R/W	-	always write 00, ignore on read
5:4	V1RTSUC	R/W		V1 reset threshold (defined by bit V1RTC) at start-up:
			00 ^[1]	V1 undervoltage detection at 90 % of nominal value at start-up (V1RTC = 00)
			01	V1 undervoltage detection at 80 % of nominal value at start-up (V1RTC = 01)
			10	V1 undervoltage detection at 70 % of nominal value at start-up (V1RTC = 10)
			11	V1 undervoltage detection at 60 % of nominal value at start-up (V1RTC = 11)
3	FNMC	R/W	0	Forced Normal mode disabled
			1 ^[1]	Forced Normal mode enabled
2	SDMC	R/W	0 ^[1]	Software development mode disabled
			1	Software development mode enabled
1	VEXTAC	R/W	0 ^[1]	regulator V2 can be used as a sensor supply via pin VEXT, provided pin V2 is left floating
			1	regulator V2 not protected against shorts to higher voltages; pin V2 must be shorted to pin VEXT
0	SLPC	R/W	0 ^[1]	Sleep mode supported
			1	Sleep mode not supported

[1] Factory preset value.

Table 12. Watchdog status register (address 05h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	-	ignore on read
3	FNMS	R	0	SBC is not in Forced Normal mode
			1	SBC is in Forced Normal mode

Table 12. Watchdog status register (address 05h)...continued

Bit	Symbol	Access	Value	Description
2	SDMS	R	0	SBC is not in Software Development mode
			1	SBC is in Software Development mode
1:0	WDS	R		watchdog status:
			00	watchdog is off
			01	watchdog is in first half of window
			10	watchdog is in second half of window
			11	reserved

The influence of SBC operating modes on the general functionality of the watchdog is summarized in [Table 13](#). It also lists the values of watchdog-related register bits when these values are predictable according to the SBC operating mode.

Control/configuration bits (writable via SPI) and interrupt bits are (re-)initialized to the default values for the SBC mode. For status bits, the expected value for the SBC mode is indicated.

Table 13. Influence of SBC operating modes on Watchdog mode and on related register bits

Bit(s)	Off (power-on default)	Forced Normal	Standby	Normal	Sleep	Reset	Overload	FSP
Watchdog	off	off	WMC ^[1]	WMC ^[1]	WMC ^[1]	off	off	off
FNMC	located in one of the non-volatile configuration registers (see Section 7.13)							
FNMS	-	1	0	0	-	-	-	-
NWP	0100	^[2]	-	-	-	0100	0100	0100
SDMC	located in one of the non-volatile configuration registers (see Section 7.13)							
SDMS	-	-	-	-	-	-	-	-
WDI	0	^[2]	-	-	-	-	-	0
WDS	-	00	-	-	-	01 or 00 if watchdog off	-	-
WMC	001 if SDMC = 1; otherwise 010	^[2]	-	-	-	001 if SDMC = 1; otherwise 010	-	001 (Autonomous mode)

[1] Determined by the setting of bits WMC in the Watchdog control register.

[2] Register not accessible; reading returns 0.

7.2.1 Software development mode

Software Development mode is provided to simplify the software design process. When Software Development mode is enabled, the watchdog starts up in Autonomous mode (WMC = 001) and is inactive after a system reset, overriding the default value (see [Table 9](#)). The watchdog is always off in Autonomous mode if Software Development mode is enabled (SDMC = 1; see [Table 11](#)).

Software can be run without a watchdog in Software Development mode. However, it is possible to activate and deactivate the watchdog for test purposes by selecting Window or Timeout mode via bits WMC while the SBC is in Standby mode (note that Window mode will only be activated once the SBC switches to Normal mode). Software Development mode is activated via bits SDMC in non-volatile memory (see [Table 11](#)).

7.2.2 Watchdog behavior in Window mode

The watchdog runs continuously in Window mode. The watchdog is in Window mode when WMC = 100 and the UJA113xA is in Normal mode.

In Window mode, the watchdog can only be triggered during the second half of the watchdog period. If the watchdog overflows, or is triggered in the first half of the watchdog period (before $t_{\text{trig(wd)1}}$), a system reset is performed. If the watchdog is triggered in the second half of the watchdog period (after $t_{\text{trig(wd)1}}$ but before $t_{\text{trig(wd)2}}$), the watchdog timer is restarted.

7.2.3 Watchdog behavior in Timeout mode

The watchdog runs continuously in Timeout mode. The watchdog is in Timeout mode when WMC = 010 and the UJA113xA is in Normal, Standby or Sleep mode. The watchdog will also be in Timeout mode if WMC = 100 and the UJA113xA is in Standby or Sleep mode. If Autonomous mode is selected (WMC = 001), the watchdog will be in Timeout mode if one of the conditions for Timeout mode listed in [Table 10](#) has been satisfied.

In Timeout mode, the watchdog can be triggered at any time up to $t_{\text{trig(wd)2}}$ after the start of the watchdog period. If the watchdog overflows ($t > t_{\text{trig(wd)2}}$), the watchdog interrupt bit (WDI) in the System interrupt status register ([Table 6](#)) is set. If a WDI is already pending, a system reset is performed. In Timeout mode, the watchdog can be used as a cyclic wake-up source for the microcontroller when the UJA113xA is in Standby or Sleep mode. In Sleep mode, a watchdog overflow generates a wake-up event.

7.2.4 Watchdog behavior in Autonomous mode

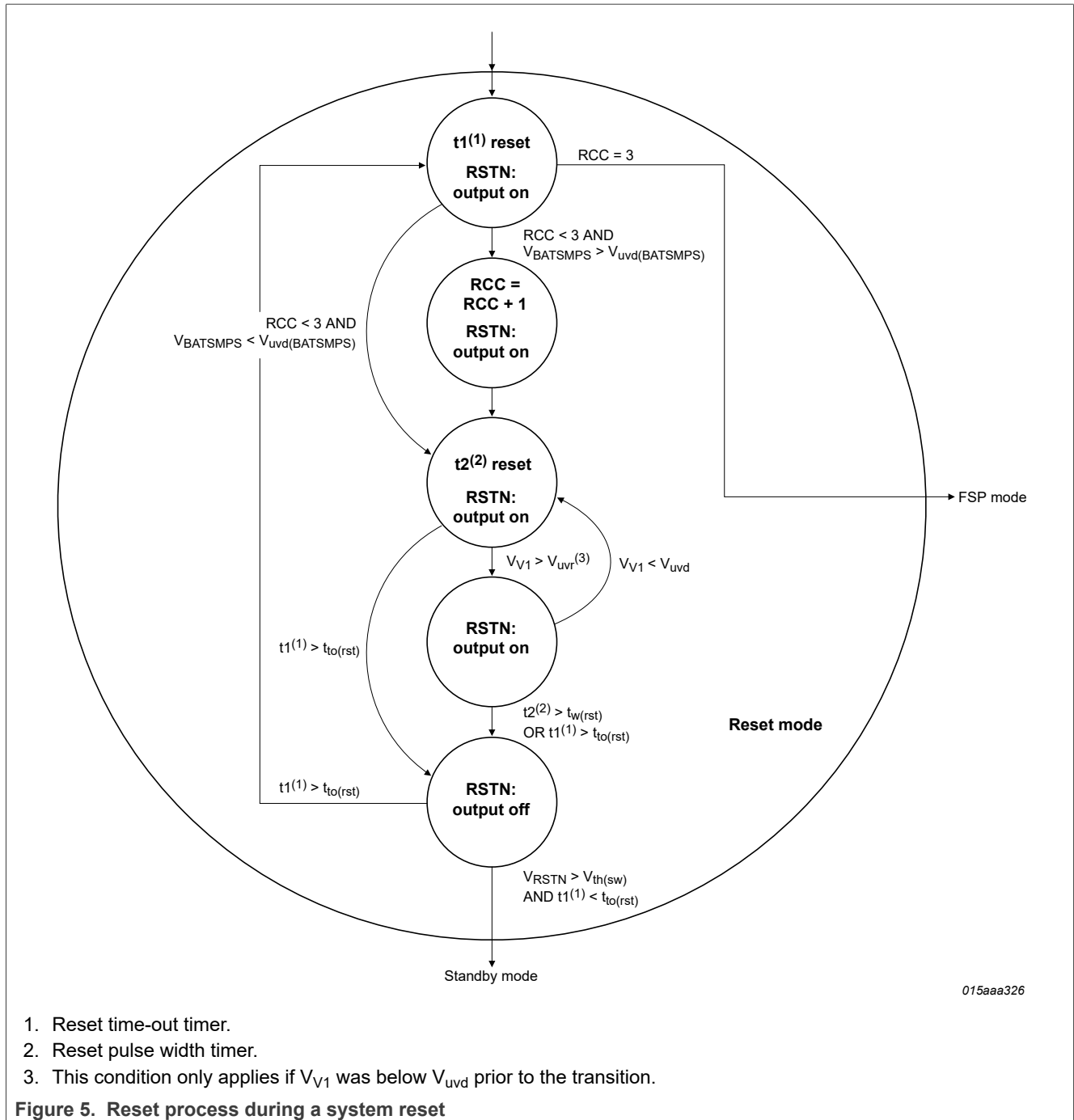
Autonomous mode is selected when WMC = 001. In Autonomous mode, the watchdog is either off or in Timeout mode, according to the conditions detailed in [Table 10](#).

When Autonomous mode is selected, the watchdog will be in Timeout mode if the SBC is in Normal mode and Software Development mode is disabled (SDMC = 0). If the SBC is in Standby mode, the watchdog will be in Timeout mode if INTN1 is LOW and SDMC = 0. Otherwise the watchdog will be off.

7.3 System reset

When a system reset occurs, the SBC switches to Reset mode and initiates a process that generates a low-level pulse on pin RSTN. The reset process is illustrated in [Figure 5](#).

When the UJA113xA enters Reset mode, the value stored in the reset counter (RCC) is checked. If $RCC < 3$, the reset counter is incremented (bits $RCC = RCC + 1$; see [Table 16](#)). Pin RSTN is then pulled LOW for the selected reset length ($t_{w(rst)}$) to begin the reset process (a reset pulse width timer is started to monitor the reset length, which is determined by bits RLC in the Start-up control register; see [Table 14](#)). When the reset pulse width timer expires, RSTN is released and the SBC switches to Standby mode.



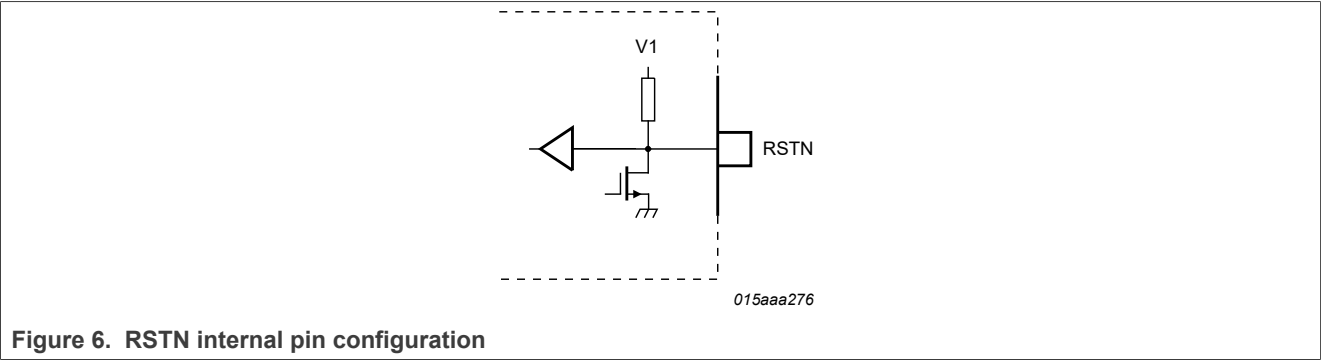
The reset counter ensures that repeated reset events are detected. If $RCC = 3$ when the UJA113xA enters Reset mode, the SBC assumes that a serious failure has occurred and switches to FSP mode, enabling the limp home function (see [Section 7.5](#)).

When the system is running correctly, it is expected that the reset counter will be reset ($RCC = 00$) periodically by the system software to ensure that routine reset events do not cause it to overflow. When the battery supply voltage is low ($V_{BATSMPS} < V_{uvd}(BATSMPS)$), the reset counter is not incremented. This precaution ensures that the system starts up properly when the supply voltage is low.

The voltage on V1 is monitored throughout the reset process. If a V1 undervoltage is detected, the reset pulse width timer is restarted. The reset process is also monitored by a reset time-out timer. The reset time-out timer ensures that deadlock is avoided in Reset mode, e.g. due to a permanently low V1 supply. If the reset process has not been completed by the time the reset time-out timer expires (after $t_{to(rst)}$), the reset process is restarted with the RSTN output released for typically 16 μ s. If $RCC < 3$ and $V_{BATSMPS} > V_{uvd(BATSMPS)}$, the reset counter is incremented. If $RCC = 3$, the SBC switches to FSP mode.

7.3.1 Characteristics of pin RSTN

Pin RSTN is a bidirectional open-drain low-side driver with integrated pull-up resistance, as shown in [Figure 6](#). With this configuration, the SBC can detect the pin being pulled down externally, e.g. by the microcontroller. The input reset pulse width must be at least $t_{w(rst)}$.



7.3.2 Selecting the output reset pulse width

The duration of the output reset pulse is selected via bits RLC in the Start-up control register ([Table 14](#)), which is located in non-volatile memory. The SBC distinguishes between a cold start and a warm start. A cold start is performed on start-up if the reset event was generated by a V1 undervoltage event (the V1 undervoltage threshold is defined by bits V1RTC; see [Table 34](#)). This happens when the SBC exits Off, Overload and Sleep modes. The output reset pulse width for a cold start is determined by the setting of bits RLC. If the reset event was not triggered by a V1 undervoltage (e.g by a warm start of the microcontroller), the SBC always uses the shortest reset length ($t_{w(rst)} = 1$ ms to 1.5 ms).

Table 14. Start-up control register (address 73h)
This table is located in non-volatile memory with restricted write access.

Bit	Symbol	Access	Value	Description
7:6	reserved	R/W	-	always write 00, ignore on read
5:4	RLC	R/W		RSTN output reset pulse width:
			00 ^[1]	$t_{w(rst)} = 20$ ms to 25 ms
			01	$t_{w(rst)} = 10$ ms to 12.5 ms
			10	$t_{w(rst)} = 3.6$ ms to 5 ms
			11	$t_{w(rst)} = 1$ ms to 1.5 ms
3	V2SUC	R/W		V2 start-up control:
			0 ^[1]	bits V2C set to 00 at power-up (default)
			1	bits V2C set to 11 at power-up
2	IO4SFC	R/W		HVIO4 configuration control:

Table 14. Start-up control register (address 73h)...*continued*

This table is located in non-volatile memory with restricted write access.

Bit	Symbol	Access	Value	Description
			0 ^[1]	pin HVIO4 configured as a standard I/O pin
			1	HVIO4 limp home function enabled
1	IO3SFC	R/W		HVIO3 configuration control:
			0 ^[1]	pin HVIO3 configured as a standard I/O pin
			1	HVIO3 limp home function enabled
0	IO2SFC	R/W		HVIO2 configuration control:
			0 ^[1]	pin HVIO2 configured as a standard I/O pin
			1	HVIO2 limp home function enabled

[1] Factory preset value.

7.3.3 Reset sources

The following events cause the SBC to switch to Reset mode:

- V_{V1} drops below the selected V1 undervoltage threshold defined by bits V1RTC
- pin RSTN is pulled down externally
- the watchdog overflows in Window mode
- the watchdog is triggered too early in Window mode (before $t_{trig(wd)1}$)
- the watchdog overflows in Timeout mode while a watchdog interrupt (WDI) is pending
- an attempt is made to reconfigure the Watchdog control register while the SBC is in Normal mode
- the SBC leaves Off mode
- the SBC leaves Overload mode
- the SBC leaves Sleep mode (local or bus wake-up)
- a Sleep mode command is received while an interrupt is pending (INTN1 LOW; see [Section 7.12.3](#))
- a Sleep mode command is received while no regular interrupt is selected (see [Section 7.12.3](#))

The reset source can be identified by reading bits RSS in the Main SBC status register ([Table 5](#)).

The influence of SBC operating modes on the RSTN pin level is summarized in [Table 15](#). It also lists the values of related register bits when these values are predictable according to the SBC's operating mode.

Control/configuration bits (writable via SPI) are (re-)initialized to the default values for the SBC mode. For status bits, the expected value for the SBC mode is indicated.

Table 15. Influence of SBC operating modes on the RSTN pin and on related register bits

Pin/bit(s)	Off (power-on default)	Forced Normal	Standby	Normal	Sleep	Reset	Overload	FSP
RSTN pin	LOW	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW
RCC	00	^[1]	-	-	-	RCC++ if $V_{BAT} > V_{uvd}(BATSMPs)$	-	00
RLC	located in one of the non-volatile configuration registers (see Section 7.13)							
RSS	00000		-	-	-	reset source	10010	10101

[1] Register not accessible; reading returns 0.

7.4 EN output

The EN pin can be used to control external hardware, such as power components, or as a general-purpose output when the system is running properly.

The EN pin is a V1-based digital output driver. It can be configured via bit ENDC in the Fail-safe control register as a push-pull output driver or as an open-drain low side driver. The functionality is identical in both configurations. The only difference is that the pin is left floating if the open-drain option is selected and pulled up otherwise.

The output signal on pin EN is configured via bit ENC as follows:

- ENC = 00: EN is permanently LOW
- ENC = 01: EN is HIGH when the SBC is in Normal, Reset and Standby modes
- ENC = 10: EN is HIGH when the SBC is in Normal mode
- ENC = 11: EN is controlled by Timer 2

If the high-side driver is deactivated (ENDC = 1), a pull-up resistor is needed from EN to V1, regardless of the value of ENC.

The EN pin can be used to deactivate external hardware in the event of a battery over- or undervoltage when the SBC is in Normal mode (see also [Section 7.7.2](#)). This function is enabled/disabled via bits ENSC (see [Table 16](#)). When this function is enabled, the EN pin is driven low when the battery supply is outside its specified operating range (see [Table 16](#)). When this happens, the settings of bits ENC are ignored.

7.4.1 Fail-safe control register

The Fail-safe control register contains the reset counter along with EN and limp home control settings.

Table 16. Fail-safe control register (address 02h)

Bit	Symbol	Access	Value	Description
7:6	ENSC	R/W		EN shut-down control:
			00	EN pin not influenced by battery over- or undervoltage
			01	EN pin driven LOW when battery undervoltage detected
			10	EN pin driven LOW when battery overvoltage detected
			11	EN pin driven LOW when battery over- or undervoltage detected
5	ENDC	R/W		EN high-side driver activation:
			0	EN high-side driver enabled; push-pull output
			1	EN high-side driver disabled; pin configured as an open-drain low-side driver
4:3	ENC	R/W		EN output configuration:
			00	EN is driven permanently LOW
			01	EN is HIGH (or floating if ENDC = 1) when the SBC is in Normal, Reset and Standby modes
			10	EN is HIGH (or floating if ENDC = 1) when the SBC is in Normal mode
			11	EN is controlled by Timer 2
2	LHC	R/W		LIMP output configuration:
			0	LIMP pin is floating
			1	LIMP pin is driven LOW

Table 16. Fail-safe control register (address 02h)...continued

Bit	Symbol	Access	Value	Description
1:0	RCC	R/W	xx	reset counter; incremented at every system reset if $V_{BATSMPS} > V_{uvd}(BATSMPS)$; maximum value is 3

The influence of SBC operating modes on the EN pin is summarized in [Table 17](#). It also lists the values of related register bits when they are (re-)initialized at power-on.

Table 17. Influence of SBC operating modes on the EN pin and on related register bits

Pin/bit(s)	Off (power-on default)	Forced Normal	Standby	Normal	Sleep	Reset	Overload	FSP
EN pin	off	off	ENC/ENDC ^[1]	ENC/ENDC ^[1]	ENC/ENDC ^{[1][2]}	ENC/ENDC ^[1]	off	ENC/ENDC ^[1]
ENC	00	[3]	-	-	-	-	-	-
ENDC	0	[3]	-	-	-	-	-	-
ENSC	00	[3]	-	-	-	-	-	-

[1] Determined by the settings of bits ENC and ENDC in the Fail-safe control register.

[2] Since V1 is off, EN can only operate as an open-drain output in Sleep mode.

[3] Register not accessible; reading returns 0.

7.5 Limp home function

The LIMP pin can be used to enable so called 'limp home' hardware in the event of an ECU failure. Detectable failure conditions include SBC overtemperature events, loss of watchdog service, short circuits on pins RSTN or V1 and user-initiated or external reset events. The LIMP pin is a battery-related, active-LOW, open-drain output.

The LIMP pin is activated automatically (via bit LHC in the Fail-Safe control register; [Table 16](#)) as soon as the SBC enters Overload Mode or switches to FSP mode after multiple reset events. Alternatively, the host controller can activate the LIMP output directly by setting bit LHC via the SPI.

Bit LHC is cleared automatically when the SBC enters Off mode. In SBC active modes, it is assumed that the host controller will clear bit LHC via the SPI. When bit LHC is cleared, the LIMP pin is immediately released.

In addition to the LIMP pin, an advanced limp home function has been implemented via pins HVIO2, HVIO3 and HVIO4 (see [Section 7.10.6](#)). These pins can be configured individually as 'limp home' or standard I/O pins via the Start-up control register (see [Table 14](#)), which is located in the non-volatile memory area.

Pin HVIO2 can be used as an additional static LIMP signal. The difference between this pin and the LIMP pin is that HVIO2 activates its high-side driver to allow the dedicated limp home hardware to be supplied directly.

The high-side driver of HVIO3 can be used to drive a PWM signal with a 10 % duty cycle and a period of 100 Hz when configured as a limp home output. HVIO4 provides a slow 1.25 Hz clock with a 50 % duty cycle that can be used for hazard light control.

The influence of SBC operating modes on the LIMP pin is summarized in [Table 18](#). It also indicates the value of bit LHC when the Fail-safe control register is (re-)initialized.

Table 18. Influence of SBC operating modes on the LIMP pin and on related register bits

Pin/bit(s)	Off (power-on default)	Forced Normal	Standby	Normal	Sleep	Reset	Overload	FSP
LIMP pin	floating	floating	LHC ^[1]	LHC ^[1]	LHC ^[1]	LHC ^[1]	LOW	LOW
LHC	0	[2]	-	-	-	-	1	1

[1] Determined by the setting of bit LHC in the Fail-safe control register (see [Table 16](#)).

[2] Register not accessible; reading returns 0.

7.6 Global temperature protection

The temperature of the UJA113xA is monitored continuously. The SBC switches to Overload mode when the global chip temperature rises above the overtemperature protection activation threshold, $T_{th(act)otp}$. When this event happens, pin RSTN is driven LOW and limp home is activated (pin LIMP is driven low; HVIO2/HVIO3/HVIO4 limp home functionality is triggered if enabled). In addition, the SMPS, the CAN and LIN transceivers and all voltage regulators are switched off. The HVIO pins are set to fail-safe state (see [Section 7.10.4](#)). When the global chip temperature falls below the overtemperature protection release threshold, $T_{th(rel)otp}$, the SBC switches to Standby mode via Reset mode.

The SBC can be configured to issue an overtemperature warning. When the global chip temperature rises above the overtemperature warning threshold ($T_{th(warn)otp}$), the SBC generates an OTWI interrupt, if enabled. It can also lower the output voltage of the SMPS to reduce power dissipation (see [Section 7.7.4.6](#)).

7.7 Power supplies

7.7.1 Battery supply pins

The UJA113xA contains a number of supply pins for supplying different SBC modules:

- BATSMPS supplies the SMPS and regulator V1
- BATV2 supplies regulator V2
- BATHS1 supplies HVIO1, HVIO2, HVIO3 and HVIO4 (if available)
- BATHS2 supplies HVIO5, HVIO6, HVIO7 and HVIO8 (if available)
- BAT supplies the LIN transceiver and is an input to the A/D converters

An external diode is needed in series between the battery and any supply pin connected directly to the battery to protect the device against negative voltages. The battery pins can be supplied via different paths. A loss of supply at one or more of the battery pins will not damage the device.

The internal circuitry is supplied via pin BAT or pin VSMPS. If both V_{BAT} and V_{VSMPS} fall below the power-off detection threshold, $V_{th(det)poff}$, the SBC switches immediately to Off mode. The voltage regulators and the internal logic are shut down in Off mode. The SBC switches from Off mode to Standby mode as soon as V_{BAT} rises above the power-on detection threshold, $V_{th(det)pon}$ (for exceptions, see [Section 7.1.3](#)). This event generates a power-on status interrupt (POSI) to inform the microcontroller that the UJA113xA has left Off mode.

7.7.2 Battery monitor

The SBC contains a two-channel 10-bit ADC covering the 20 V full-scale range for monitoring the battery voltage. The ADC is used to measure the supply voltages on pins BAT and BATSENSE. Note that this function is only available in SBC Normal mode. If a series resistor and a capacitor are connected as shown in [Figure 7](#), the supply voltage connected to the anode of the reverse polarity diode can be monitored via pin BATSENSE. The ADC conversion results are stored in bits BMBCD and BMSCD in, respectively, the V_{BAT} and $V_{BATSENSE}$ conversion results registers ([Table 23/Table 24](#) and [Table 25/Table 26](#)).

An under- or overvoltage event on a selected ADC channel generates a battery monitor undervoltage (BMUI) or overvoltage (BMOI) interrupt (and optionally deactivates the CAN transceiver and peripheral loads connected to HVIO_n/V2/VEXT or EN). The channel is selected via the battery monitor source control bit (BMSC) in the Battery monitor trigger source control register ([Table 19](#)). If BMSC = 0, an under- or overvoltage on pin BAT triggers an interrupt. If BMSC = 1, an under- or overvoltage on pin BATSENSE triggers an interrupt.

The battery monitor under- and overvoltage thresholds are set via bits BMUTC and BMOTC (see [Table 20](#) and [Table 21](#)). With BMUTC = 00h, undervoltage detection is turned off. With BMOTC = FFh, an overvoltage event is triggered with a 10-bit conversion result > 3FCh. Under- and overvoltage threshold hysteresis levels are set

via bits BMHUC and BMHOC (see Table 22). The under- and overvoltage status can be monitored via bits BMUVS and BMOVS in the Supply status register (Table 27).

In order to minimize quiescent current consumption, battery monitoring is only enabled when the SBC is in Normal mode. When battery monitoring is deactivated, all related functions are unavailable.

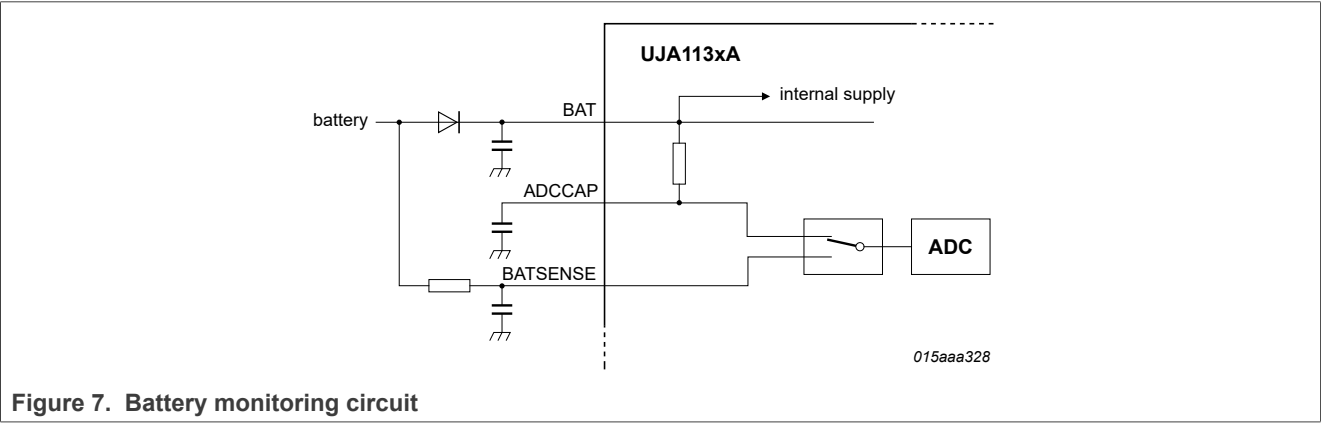


Table 19. Battery monitor event trigger source control register (address 11h)

Bit	Symbol	Access	Value	Description
7:1	reserved	R/W	-	always write all 0s, ignore on read
0	BMSC	R/W		trigger source for generating battery monitoring/overvoltage/ undervoltage/ shutdown events:
			0	voltage on BAT triggers an event
			1	voltage on BATSENSE triggers an event

Table 20. Battery monitor undervoltage threshold control register (address 12h)

Bit	Symbol	Access	Value	Description
7:0	BMUTC	R/W	xxxxxxx	threshold for triggering a battery undervoltage event and BMUI interrupt; threshold = BMUTC[7:0]/255 × 20 V

Table 21. Battery monitor overvoltage threshold control register (address 13h)

Bit	Symbol	Access	Value	Description
7:0	BMOTC	R/W	xxxxxxx	threshold for triggering a battery overvoltage event and BMOI interrupt; threshold = BMOTC[7:0]/255 × 20 V

Table 22. Battery monitor hysteresis control register (address 14h)

Bit	Symbol	Access	Value	Description
7:4	BMHOC	R/W	xxxx	battery monitor overvoltage threshold release level; release level = BMHOC[7:4] × 4/255 × 20 V below threshold defined by BMOTC
3:0	BMHUC	R/W	xxxx	battery monitor undervoltage threshold release level; release level = BMHUC[3:0] × 4/255 × 20 V above threshold defined by BMUTC

Table 23. ADC conversion results for V_{BAT} register 1 (address 15h)

Bit	Symbol	Access	Value	Description
7:0	BMBCD	R	xxxxxxx	ADC conversion results for voltage measured on pin BAT; 8 most significant bits

Table 24. ADC conversion results for V_{BAT} register 2 (address 16h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	ignore on read
2	BMBCS	R		ADC conversion results for V _{BAT} read out via SPI:
			0	8 MSBs of BMBCD not read out via SPI
			1	8 MSBs of BMBCD read out via SPI
1:0	BMBCD	R	xx	ADC conversion results for voltage measured on pin BAT; 2 least significant bits

Table 25. ADC conversion results for V_{BATSENSE} register 1 (address 17h)

Bit	Symbol	Access	Value	Description
7:0	BMSCD	R	xxxxxxx	ADC conversion results for voltage measured on pin BATSENSE; 8 most significant bits

Table 26. ADC conversion results for V_{BATSENSE} register 2 (address 18h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	ignore on read
2	BMSCS			ADC conversion results for V _{BATSENSE} read out via SPI:
			0	8 MSBs of BMSCD not read out via SPI
			1	8 MSBs of BMSCD read out via SPI
1:0	BMSCD	R	xx	ADC conversion results for voltage measured on pin BATSENSE; 2 least significant bits

Table 27. Supply voltage status register (address 1Bh)

Bit	Symbol	Access	Value	Description
7:6	reserved	R	-	ignore on read
5	BMOVS	R		overvoltage status of voltage on selected (via BMSC) event trigger source (BAT or BATSENSE):
			0	voltage below overvoltage threshold (defined by BMOTC)
			1	voltage above overvoltage threshold (defined by BMOTC)
4	BMUVS	R		undervoltage status of voltage on selected (via BMSC) event trigger source (BAT or BATSENSE):
			0	voltage above undervoltage threshold (defined by BMUTC)
			1	voltage below undervoltage threshold (defined by BMUTC)

Table 27. Supply voltage status register (address 1Bh)...continued

Bit	Symbol	Access	Value	Description
3	SMPSS	R		status of voltage on pin VSMPS:
			0	V_{VSMPS} is within the regulation window
			1	V_{VSMPS} is outside the regulation window
2:1	VEXTS	R		status of VEXT pin:
			00	V_{VEXT} ok (above undervoltage and below overvoltage thresholds)
			01	V_{VEXT} below undervoltage threshold
			10	V_{VEXT} above overvoltage threshold
			11	V_{VEXT} disabled
0	V1S	R		V1 status:
			0	V1 output voltage above 90 % undervoltage threshold
			1	V1 output voltage below 90 % undervoltage threshold

Table 28 lists the values of bits related to the battery monitor when they are (re-)initialized at power-on. Status bit values in brackets are default values that may not represent the actual status. The battery monitor is only enabled in Normal mode.

Table 28. Influence of SBC operating modes on the battery monitor and on related register bits

Symbol	Off (power-on default)	Forced Normal	Standby	Normal	Sleep	Reset	Overload	FSP
Battery monitor	disabled	disabled	disabled	active	disabled	disabled	disabled	disabled
BMBCD ^[1]	-	[2]	(0000000000)	-	-	-	-	-
BMBCS	0	[2]	-	-	-	-	-	-
BMSCD ^[1]	-	[2]	(0000000000)	-	-	-	-	-
BMSCS	0	[2]	-	-	-	-	-	-
BMHOC	0000	[2]	-	-	-	-	-	-
BMHUC	0000	[2]	-	-	-	-	-	-
BMOI	0	[2]	-	-	-	-	-	0
BMOIE	0	[2]	-	-	-	-	-	0
BMOTC	11111111	[2]	-	-	-	-	-	-
BMOVS	-	[2]	-	-	-	-	-	-
BMSC	0	[2]	-	-	-	-	-	-
BMUI	0	[2]	-	-	-	-	-	0
BMUIE	0	[2]	-	-	-	-	-	0
BMUTC	00000000	[2]	-	-	-	-	-	-
BMUVS	-	[2]	-	-	-	-	-	-

[1] Note that battery monitoring is only enabled in Normal mode.

[2] Register not accessible; reading returns 0.

7.7.3 Overvoltage shut-down

If the supply voltage remains above the overvoltage detection threshold ($V_{th(det)ov}$) for longer than $t_{det(ov)}$, the SBC triggers an Overvoltage shut-down interrupt (OVSDI; see [Table 81](#)). Once the interrupt has been generated, the overvoltage shut-down timer is started and the SBC enters Overload mode after $t_{d(sd)ov}$.

If the supply voltage falls below the overvoltage release threshold ($V_{th(rel)ov}$) while the overvoltage shut-down timer is running, a system reset is generated when the timer expires and the SBC switches to Standby mode (via Reset mode; see [Figure 4](#)).

A system reset is generated every time the SBC exits Overload mode. In all cases, the reset source is recorded as 'leaving Overload mode' (RSS = 10010; see [Table 5](#)).

7.7.4 Buck and Boost converter (SMPS)

All the active components of a SMPS are included in the UJA113xA (only a single external coil and some capacitors are needed to obtain a functional SMPS). Three bootstrap capacitors are needed between pins CAPA and CAPB, BOOTH1 and L1 and between BOOTH2 and L2 (see [Figure 31](#)). The converter operating mode, Boost, Buck or Auto, is selected automatically and depends on the supply voltage and load conditions. The SMPS configuration is shown in [Figure 8](#).

The SMPS is used as a pre-regulator for linear regulator V1. It can also be used as a pre-regulator for V2 or to supply an external load such as an LED chain.

7.7.4.1 SMPS parameter selection and status monitoring

The SMPS output voltage (between 5 V and 8 V) is selected via bits SMPSOC in the SMPS output voltage control register ([Table 30](#)). Since the SMPS is intended to operate as a pre-regulator for linear regulators V1 and/or V2, the output voltage must be set to a voltage higher than the output voltage(s) of V1 and/or V2. At power-on and when a pulse is detected on RSTN, the SMPS is enabled with the output voltage set to 6.0 V (the default value; see [Table 1](#)).

The SMPS status can be monitored via bit SMPSS in the Supply voltage status register ([Table 27](#)). A regulation window is defined from $V_{VSMPS(act)} - 60 \text{ mV}$ to $V_{VSMPS(act)} + 60 \text{ mV}$. $V_{VSMPS(act)}$ is the actual value of the SMPS output voltage at DC load. SMPSS is set to 0 when V_{VSMPS} is within the regulation window. SMPSS is set to 1 when V_{VSMPS} is outside the regulation window for longer than $t_{to(reg)}$. This time-out is added because load transients may cause a short excursion of V_{VSMPS} outside the 60 mV window while the SMPS is still in regulation and inside its specified limits. An SMPSSI interrupt is generated, if enabled (SMPSSIE = 1; see [Table 32](#)), when V_{VSMPS} moves outside the regulation window.

The SMPSS flag will be set/cleared when V_{VSMPS} leaves/enters the regulation window because of a transition between switched mode and Pass-through mode. This includes transitions requested via SPI, automatic transitions caused by a too-low or too-high supply voltage, and automatic transitions caused by a too-high output current. The SMPSS flag is disabled when the SMPS is in Pass-through mode and cannot trigger an SMPSSI interrupt.

Table 29. SMPS control register (address 19h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R/W	-	always write 0000; ignore on read
3	SMPSOTC	R/W		SMPS overtemperature control:
			0	V_{VSMPS} not modified when an overtemperature warning received (OTWI interrupt)
			1	V_{VSMPS} automatically reduced to 5 V when the chip temperature is above the overtemperature warning threshold, $T_{th(warn)otp}$

Table 29. SMPS control register (address 19h)...continued

Bit	Symbol	Access	Value	Description
2	reserved	R/W	-	always write 0; ignore on read
1:0	SMPSC	R/W		SMPS on/off control:
			00	the SMPS is on in Normal, Standby and Reset modes and shut down in all other modes
			01	the SMPS is on in Normal, Standby, Reset and Sleep modes and shut down in all other modes
			10	reserved
			11	Pass-through mode is requested in Normal, Standby and Sleep modes

Table 30. SMPS output voltage control register (address 1Ah)

Bit	Symbol	Access	Value	Description
7:4	reserved	R/W	-	always write 0000; ignore on read
3:0	SMPSOC	R/W		SMPS output voltage (V_{VSMPS}):
			0000	5.0 V
			0001	5.2 V
			0010	5.4 V
			0011	5.6 V
			0100	5.8 V
			0101	6.0 V
			0110	6.2 V
			0111	6.4 V
			1000	6.6 V
			1001	6.8 V
			1010	7.0 V
			1011	7.2 V
			1100	7.4 V
			1101	7.6 V
			1110	7.8 V
			1111	8.0 V

The supply interrupt status bits are located in the Supply interrupt status register, [Table 31](#). The interrupt mechanism is described in [Section 7.12](#).

Table 31. Supply interrupt status register (address 62h)

Bit	Symbol	Access	Value	Description
7:6	reserved	R/W	-	always write 00; ignore on read
5	SMPSSI	R/W	0	no SMPS status interrupt pending

Table 31. Supply interrupt status register (address 62h)...continued

Bit	Symbol	Access	Value	Description
			1	SMPS status interrupt pending (value of bit SMPSS has changed; see Section 7.7.4.1)
4	BMOI	R/W	0	no battery monitor overvoltage interrupt pending
			1	battery monitor overvoltage interrupt pending
3	BMUI	R/W	0	no battery monitor undervoltage interrupt pending
			1	battery monitor undervoltage interrupt pending
2	VEXTOI	R/W	0	no VEXT overvoltage interrupt pending
			1	VEXT overvoltage interrupt pending
1	VEXTUI	R/W	0	no VEXT undervoltage interrupt pending
			1	VEXT undervoltage interrupt pending
0	V1UI	R/W	0	no V1 undervoltage interrupt pending
			1	V1 undervoltage interrupt pending

Supply interrupts are enabled/disabled via the Supply interrupt enable register, [Table 32](#).

Table 32. Supply interrupt enable register (address 1Ch)

Bit	Symbol	Access	Value	Description
7:6	reserved	R	-	always write 00, ignore on read
5	SMPSSIE	R/W	0	SMPS status interrupt disabled
			1	SMPS status interrupt enabled
4	BMOIE	R/W	0	battery monitor overvoltage interrupt disabled
			1	battery monitor overvoltage interrupt enabled
3	BMUIE	R/W	0	battery monitor undervoltage interrupt disabled
			1	battery monitor undervoltage interrupt enabled
2	VEXTOIE	R/W	0	VEXT overvoltage interrupt disabled
			1	VEXT overvoltage interrupt enabled
1	VEXTUIE	R/W	0	VEXT undervoltage interrupt disabled
			1	VEXT undervoltage interrupt enabled
0	V1UIE	R/W	0	V1 undervoltage interrupt disabled
			1	V1 undervoltage interrupt enabled

SMPS control and status bit values, when predictable according to the SBC operating mode, are given in [Table 33](#).

Control/configuration bits (writable via SPI) and interrupt bits are (re-)initialized to the default values for the SBC mode. For status bits, the expected value for the SBC mode is indicated.

Table 33. Influence of SBC operating modes on SMPS control and interrupt status registers

Block/bit(s)	Off (power-on default)	Forced Normal	Standby	Normal	Sleep	Reset	Overload	FSP
SMPS	off	on (default voltage)	SMPS control register ^[1]	SMPS control register ^[1]	SMPS control register ^[1]	on	off	on
SMPSC	00	^[2]	-	-	-	00	00	00
SMPSOC	0101	^[2]	-	-	0101	0101	0101	0101
SMPSOTC	0	^[2]	-	-	-	0	0	0
SMPSS	0	^[2]	-	-	-	-	-	-
SMPSSI	0	^[2]	-	-	-	-	-	0
SMPSSIE	0	^[2]	-	-	-	-	-	0

[1] Determined by the bit settings in the SMPS control register.

[2] Register not accessible; reading returns 0.

7.7.4.2 Automatic up/down principle

The SMPS features an integrated up/down converter. The switching control mechanism implemented in the SMPS switches automatically and seamlessly between three operating modes, without affecting the performance.

Buck mode

The converter will be in Buck mode when the required output voltage is significantly lower than the input voltage. In this mode, the coil terminal connected to pin L2 is permanently connected to the output, VSMPS, via internal switch S3 (see [Figure 8](#)). S1 and S2 are the buck converter switches.

A buck converter uses significantly less energy than a linear regulator because the average input current is lower than the average output current.

Boost mode

The converter will be in Boost mode when the required output voltage is higher than the input voltage. In this mode, the coil terminal connected to pin L1 is permanently connected to the input, pin BATSMPS, via internal switch S1. S3 and S4 are the boost converter switches. In Boost mode, the average input current is higher than the average output current.

At very low input voltages, the load can be too great to maintain a constant output voltage, causing the output voltage to fall. Note that the boost current capability of the UJA1131A/UJA1132A is higher than that of the UJA1135A/UJA1136A.

Auto mode

The converter will be in Auto mode when the required output voltage is in the same range as the input voltage. In this mode, all four switches operate to maintain the output voltage at the correct level, independently of the input voltage.

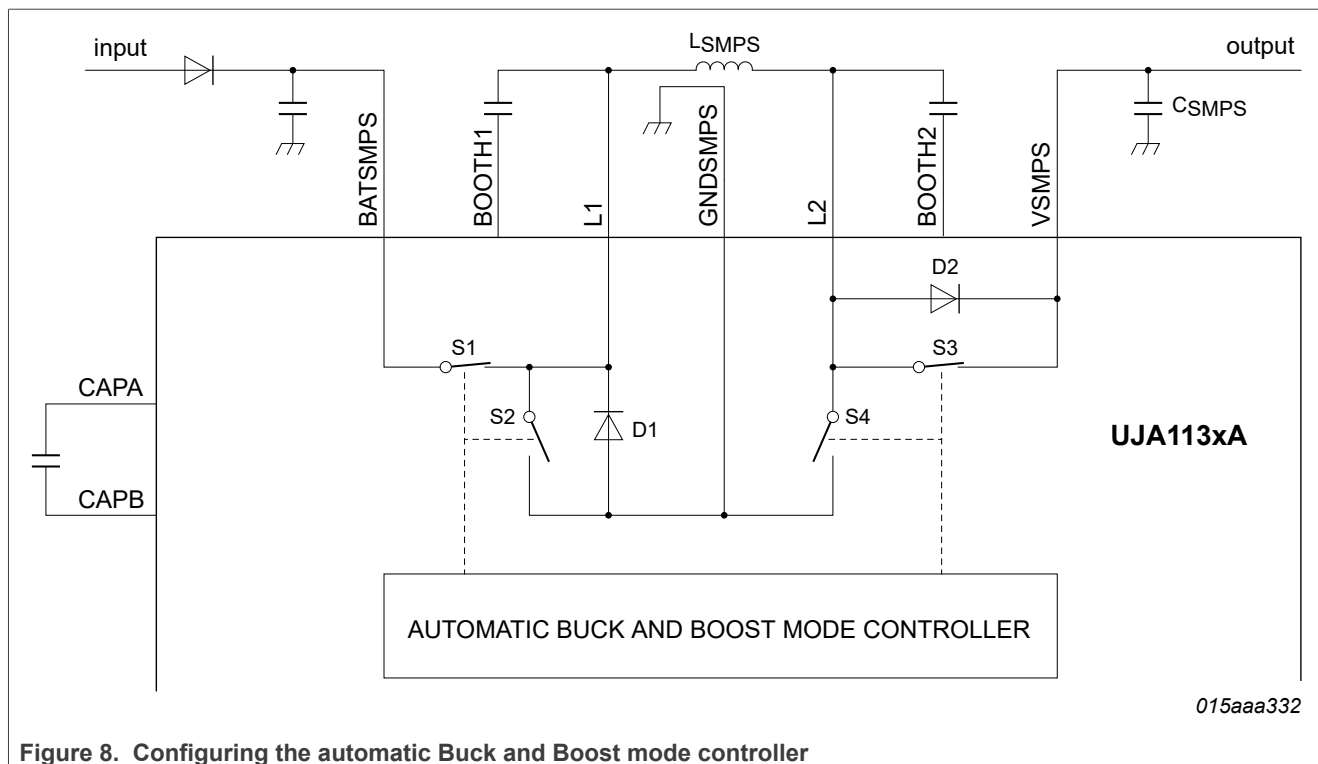


Figure 8. Configuring the automatic Buck and Boost mode controller

Bootstrap cycle

In Buck, Boost and Auto modes, a bootstrap capacitor charge cycle is inserted after every 32nd PWM cycle. The duration of the charge cycle is 1/4 of a PWM cycle. During the bootstrap charge cycle, both sides of the coil are connected to ground.

In Pass-through mode (see [Section 7.7.4.4](#)), a bootstrap charge cycle only occurs if one of the bootstrap voltages drops below the minimum voltage required to keep S1 and S3 switched on properly. The bootstrap charge cycle frequency is automatically reduced to minimize quiescent current.

7.7.4.3 Start-up and inrush currents

The SMPS can start up at any battery voltage above the power-on level. It switches automatically to Boost, Buck or Auto mode as required by the battery voltage level and output voltage setting. The auto up/down mechanism allows for a controlled start-up, even when the input voltage is lower than the desired output voltage. Unlike a conventional boost-converter, the SMPS does not require a voltage at the output to start up.

To avoid excessive inrush currents and coil saturation at start-up, the rate of increase of the coil current is limited by the switching control mechanism when the SMPS is starting up (see NXP application note AN13928 'UJA113xA series application note'). This function also prevents overshoot at the output voltage during start-up.

7.7.4.4 Pass-through mode operation

When the output load is light, it may not be necessary to use the SMPS as a pre-regulator for V1 and/or V2 since the internal power dissipation will be relatively low, even when using linear regulators. For example, the microcontroller still needs to be supplied when the SBC is in Standby mode, even though it may be switched to a low-current mode. Pass-through mode is provided for such situations.

In Pass-through mode, switches S1 and S3 are closed. The internal power consumption of the SMPS is negligible. The output voltage mirrors the input voltage, less the voltage drop across the coil and the switches.

Pass-through mode is selected via bits SMPSC in the SMPS control register (Table 29). When SMPSC is set to 11, the UJA113xA switches to Pass-through mode provided no over- or under-voltage is detected and the load current is below the pass-through overcurrent threshold, $I_{th(ocd)}(V_{SMPS})$. The transition from a switching mode to Pass-through mode is made gradually to avoid overshoots and oscillations on VSMPS (see Section 7.7.4.5).

Pass-through mode is automatically disabled and the SMPS is reactivated under any of the following conditions:

- undervoltage detected ($V_{BATSMPS} < V_{uvd}(BATSMPS)$)
- overvoltage detected ($V_{BATSMPS} > V_{ovd}(BATSMPS)$)
- the chip temperature rises above the overtemperature warning threshold ($T_{th(warn)otp}$)
- the load current exceeds the pass-through overcurrent threshold, $I_{th(ocd)}(V_{SMPS})$

Undervoltage protection prevents a system reset being generated by a falling battery supply voltage.

Overvoltage protection ensures that loads connected to the SMPS output are not exposed to the high voltages that could be generated during a jump start or load dump. Overvoltage protection also allows 16 V ceramic capacitors to be used at the SMPS output.

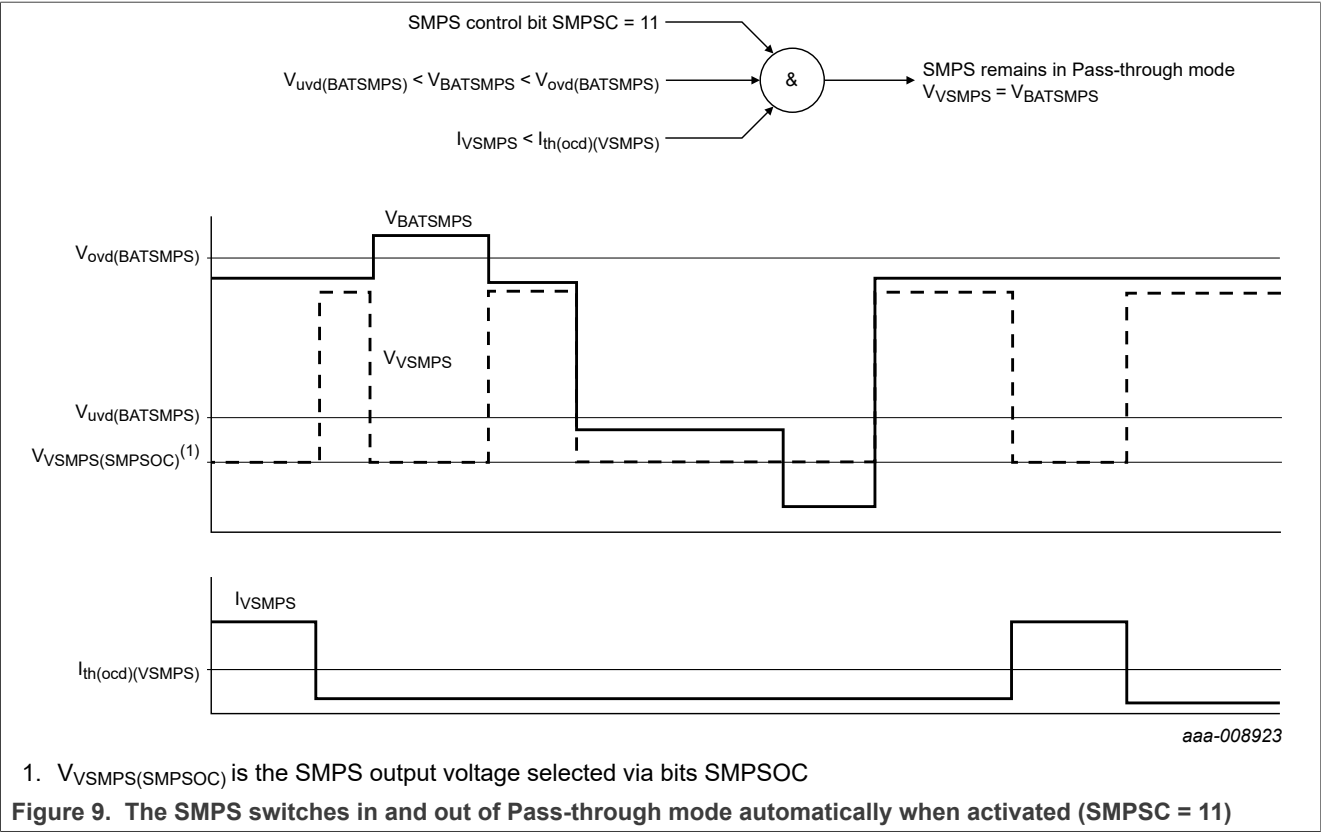
When the chip temperature exceeds the overtemperature warning threshold, the SMPS is reactivated to reduce internal dissipation. If the load current exceeds the pass-through overcurrent threshold, $I_{th(ocd)}(V_{SMPS})$, the SMPS is reactivated to limit the output current in the event of a short-circuit condition on the VSMPS pin.

A timer is started as soon as the SMPS is activated. If the condition that caused the SMPS to leave Pass-through mode is removed before the timer expires (after $t_{d(act)}$), the return to Pass-through mode is postponed until the timer has expired ($t_{d(act)}$ is the minimum time the SMPS spends in switched mode before a transition to Pass-through mode can be attempted).

When the SMPS is active, it is not possible to determine if an overcurrent would be detected in Pass-through mode. So the SMPS will attempt to return to Pass-through mode after $t_{d(act)}$ if Pass-through mode is still selected (SMPSC = 11) and no over- or under-voltage is present. If an overcurrent is detected, the SMPS will be activated again (after $t_{t(sw-pt)}$). So a continuous overcurrent causes the SMPS to cycle through active and Pass-through modes with a period of $t_{d(act)} + t_{t(sw-pt)}$.

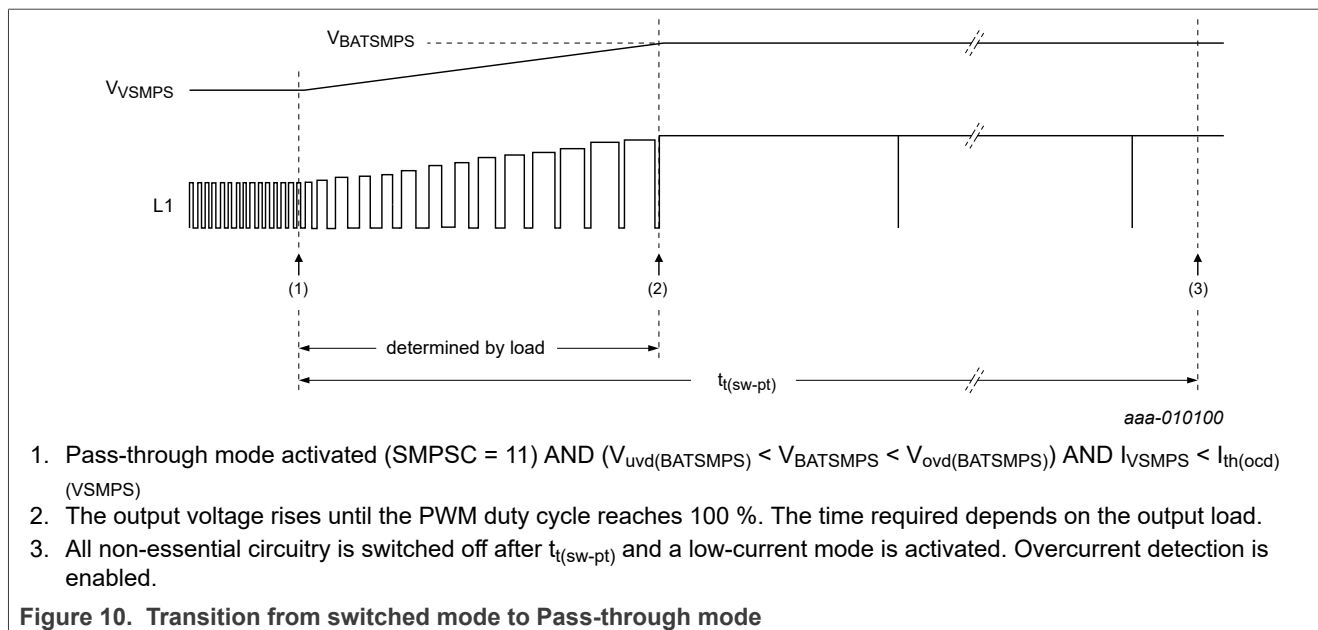
Automatic transition in and out of Pass-through mode is illustrated in Figure 9.

During the transition from Pass-through to an active SMPS operating mode, the voltage on the VSMPS pin remains above the selected output voltage. This precaution guarantees that the voltage regulator(s) remains in regulation and within specification. It also ensures that the system can withstand load current transients on the V1 regulator output from 0 mA to 500 mA in Standby mode.



7.7.4.5 Transitions to and from Pass-through mode

When switching to Pass-through mode, the SMPS cannot simply close the two high-side switches (S1 and S3) as this would generate very large transient currents in the coil and a large output voltage overshoot. Instead, the SMPS controller slowly increase the duty cycle. As soon as the controller detects a 100% duty cycle it stops switching and only generates filling pulses to keep the bootstrap capacitors charged. The time required to reach 100% duty cycle depends on the output load. The transition is always completed within $t_{\text{t(sw-pt)}}$. This behavior is illustrated in [Figure 10](#).

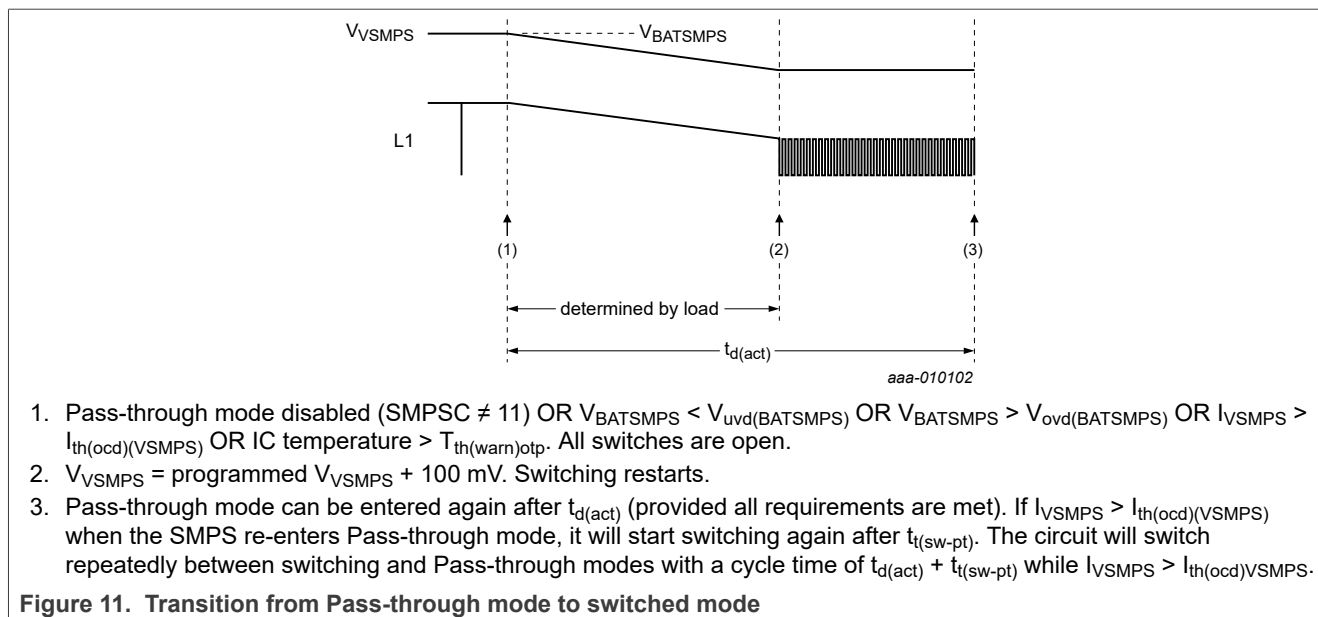


After the fixed transition time ($t_{\text{t(sw-pt)}}$), all analog modules involved in SMPS switching are switched off to conserve current. The pass-through control module will remain active to provide regular filler pulses to keep the bootstrap supply capacitors charged. It will also monitor the over- and under voltage indicator signals. The SMPS will meet Standby mode current requirements.

The transition time is inserted to allow the system (microcontroller) some time to switch to a sleep mode after switching on Pass-through mode.

When the SMPS is triggered to leave Pass-through mode, V_{VSMPS} is likely to be much greater than the programmed value. To achieve a smooth transition, all analog circuits are started up and all switching is suspended. This will cause V_{VSMPS} to fall. Once V_{VSMPS} falls below the programmed output voltage level plus 100 mV, normal switching is resumed. The time between disabling Pass-through mode and the SMPS starting switching is determined by the output load.

To prevent the SMPS rapidly oscillating between switching and Pass-through mode, it will remain in switching mode for at least $t_{\text{d(act)}}$ before attempting to return to Pass-through mode.



7.7.4.6 Overload protection

Output current limiting protects the SMPS and the control module against short circuits at the output.

Under normal operating conditions, the SMPS minimizes internal power dissipation. However, if the input voltage is low when the SMPS is required to supply a heavy load in Boost mode, the input current can significantly exceed the output current. When this happens, the power dissipated in the internal switches and diodes can lead to thermal overload. Thermal shutdown can be avoided by reducing the load current and/or the SMPS output voltage. An overtemperature warning (status bit OTWS = 1; see [Table 5](#)) can be interpreted as a request to take appropriate action.

The UJA113xA provides an option to reduce the SMPS output voltage to 5 V automatically while the temperature is above the overtemperature warning threshold. This option is enabled by setting bit SMPSTC in the SMPS control register ([Table 29](#)) to 1. When this option is activated, the linear regulators fed by the SMPS are no longer able to supply 5 V. However the output voltage of the regulator supplying the microcontroller may still be high enough for it to remain operational. This depends on the supply voltage range of the microcontroller. Automatic output voltage reduction is disabled (SMPSTC = 0) at power-up and when a pulse is received on RSTN.

7.7.5 Linear regulators

The UJA113xA contains two independent voltage regulators, V1 and V2.

7.7.5.1 V1 regulator

Regulator V1 is intended to supply the microcontroller, its periphery and additional CAN transceivers and delivers up to 500 mA at 3.3 V or 5 V. It is supplied internally from the output of the SMPS.

The output voltage on V1 is monitored continuously. A system reset is generated if the voltage on V1 falls below the undervoltage threshold for longer than $t_{det(uv)}V1$.

For the 5 V versions of the UJA113xA (UJA113xA/5V0), the undervoltage threshold (60 %, 70 %, 80 % or 90 % of the nominal V1 voltage) is selected via bits V1RTC in the Regulator control register ([Table 34](#)). The default value of the undervoltage threshold at power-up is determined by the value of bits V1RTSUC in the

SBC configuration control register (Table 11). The SBC configuration control register is in non-volatile memory, allowing the user to define the undervoltage threshold (V1RTC) at start-up.

For the 3.3 V versions (UJA113xAHW/3), the 90 % threshold always applies (regardless of the V1RTC and V1RTSUC setting).

In addition, a warning is issued (a V1UI interrupt) if V1 drops below 90 % of the nominal value (provided the interrupt is enabled; V1UIE = 1). The UJA113xAHW/5 can use this information to warn the microcontroller that the level on V1 is outside the nominal supply range when the 60 %, 70 % or 80 % threshold is selected. The status of V1, whether the output voltage is above or below the 90 % undervoltage threshold, can be read via bit V1S in the Supply voltage status register (Table 27).

In reverse supply situations (e.g. when the attached microcontroller is in low-power mode and current is injected via its port pins to its supply pins), internal clamp circuitry ensures that the voltage on pin V1 remains below 6 V.

7.7.5.2 Voltage regulator V2

Voltage regulator V2 is a 5 V regulator with two outputs V2 and VEXT.

If the regulator is intended to supply external components that require protection against shorts to battery and shorts to ground, the VEXT output should be selected, leaving pin V2 open. Bit VEXTAC must be set to 0 (see Table 11). In this configuration, the output current flows through a transistor connected between V2 and VEXT (see Figure 1). This transistor is automatically deactivated if an overvoltage is detected at pin VEXT. The transistor is re-enabled when the overvoltage condition is removed, reactivating VEXT.

Pins V2 and VEXT should be shorted together when the regulator is being used to supply internal loads (e.g. the CAN transceiver and other peripheral loads). In this case, bit VEXTAC should be set to 1 (VEXTAC is located in non-volatile memory).

The V2 output pin is not protected against shorts to the battery, but connecting V2 to VEXT reduces the supply voltage needed on BATV2 to generate 5 V at the output at low battery voltages. The configuration options are illustrated in Figure 12.

V2 is enabled and disabled via bits V2C in the Regulator control register (Table 34). The value of bits V2SUC in the Start-up control register (Table 14) determine the default value at power-up. The Start-up control register is in non-volatile memory (see Section 7.13), allowing the user to define the configuration of V2 at start-up.

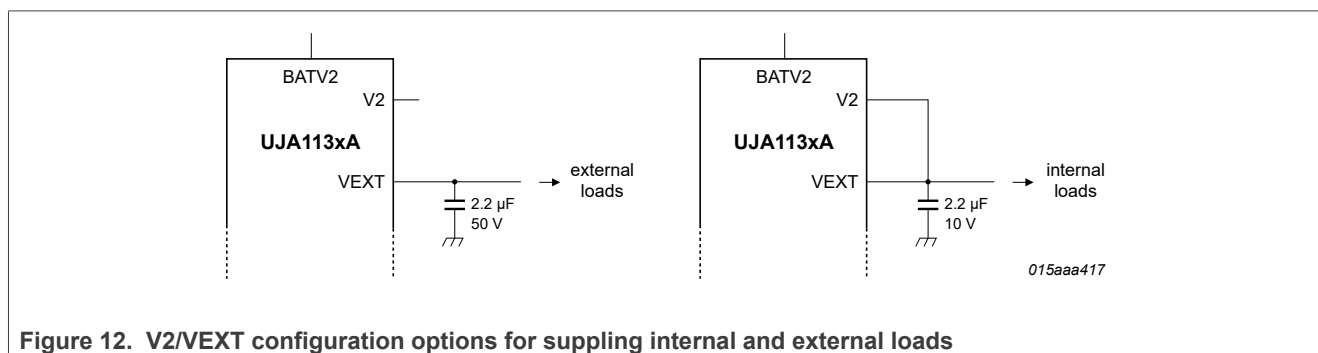


Figure 12. V2/VEXT configuration options for supplying internal and external loads

The output voltage on VEXT is monitored continuously. Warnings are issued when the voltage drops below 90 % of the nominal value (VEXTUI interrupt) for longer than $t_{\text{det(ov)}}V_{\text{EXT}}$ or rises to 110 % of the nominal value (VEXTOI interrupt) for longer than $t_{\text{det(ov)}}V_{\text{EXT}}$. This information can be used to warn the microcontroller that the level on VEXT is outside the nominal supply range or that a failure has occurred. The status of V_{VEXT} can be read via bits VEXTS in the Supply voltage status register (Table 27).

The UJA113xA can be configured to shut down V2 automatically when the battery monitor detects an under- or overvoltage on the battery supply (via bits V2SC; see Table 34).

7.7.5.3 Regulator control register

Table 34. Regulator control register (address 10h)

Bit	Symbol	Access	Value	Description
7:6	reserved	R/W	-	always write 00; ignore on read
5:4	V2SC	R/W		V2 shutdown response to a battery over- or undervoltage:
			00	no shut-down in response to under- or overvoltage
			01	shut-down in response to an undervoltage
			10	shut-down in response to an overvoltage
			11	shut-down in response to under- and overvoltage
3:2	V2C	R/W	^[1]	V2 control:
			00	V2 off in all modes
			01	V2 on in Normal mode
			10	V2 on in Normal, Standby and Reset modes
			11	V2 on in Normal, Standby, Sleep, Reset and FSP modes
1:0	V1RTC	R/W	^[2]	V1 undervoltage reset threshold:
			00	reset threshold set to 90 % of V1 nominal output voltage
			01	reset threshold set to 80 % of V1 nominal output voltage
			10	reset threshold set to 70 % of V1 nominal output voltage
			11	reset threshold set to 60 % of V1 nominal output voltage

[1] Default value at power-up defined by setting of bits V2SUC (see [Table 14](#)).

[2] Valid for the UJA113xA/5V0 versions only; for the UJA113xA/3V3 versions, the V1 undervoltage reset threshold is always 90 % of the nominal value. Default value at power-up defined by setting of bits V1RTSUC. (see [Table 11](#)).

See also [Table 11](#) in [Section 7.2](#), [Table 14](#) in [Section 7.3.2](#), [Table 27](#) in [Section 7.7.2](#) and [Table 32](#) and [Table 31](#) in [Section 7.7.4.1](#).

The influence of SBC operating modes on the linear regulators is summarized in [Table 35](#). It also lists the values of associated register bits when these values are predictable according to the SBC operating mode.

Control/configuration bits (writable via SPI) and interrupt bits are (re-)initialized to the default values for the SBC mode. For status bits, the expected value for the SBC mode is indicated.

Table 35. Influence of SBC operating modes on the linear regulators and on related register bits

Symbol	Off (power-on default)	Forced Normal	Standby	Normal	Sleep	Reset	Overload	FSP
V1	off	on	on	on	off	on	off	on
V2/VEXT	off	on	V2C ^[1]	V2C ^[1]	V2C ^[1]	V2C ^[1]	off	V2C ^[1]
V1RTC	defined by V1RTSUC	^[2]	-	-	-	-	-	V1RTSUC
V1RTSUC	located in one of the non-volatile configuration registers (see Section 7.13)							
V1S	-	^[2]	-	-	-	-	-	-
V1UI	0	^[2]	-	-	-	-	-	0
V1UIE	0	^[2]	-	-	-	-	-	0

Table 35. Influence of SBC operating modes on the linear regulators and on related register bits...continued

Symbol	Off (power-on default)	Forced Normal	Standby	Normal	Sleep	Reset	Overload	FSP
V2C	defined by V2SUC	[2]	-	-	-	-	-	-
VEXTOI	0	[2]	-	-	-	-	-	0
VEXTOIE	0	[2]	-	-	-	-	-	0
VEXTS	-	[2]	-	-	-	-	-	-
V2SC	00	[2]	-	-	-	-	-	-
V2SUC	located in one of the non-volatile configuration registers (see Section 7.13)							
VEXTAC	located in one of the non-volatile configuration registers (see Section 7.13)							
VEXTUI	0	[2]	-	-	-	-	-	0
VEXTUIE	0	[2]	-	-	-	-	-	0

[1] Determined by the setting of bits V2C in the Regulator control register.

[2] Register not accessible; reading returns 0.

7.8 High-speed CAN transceiver

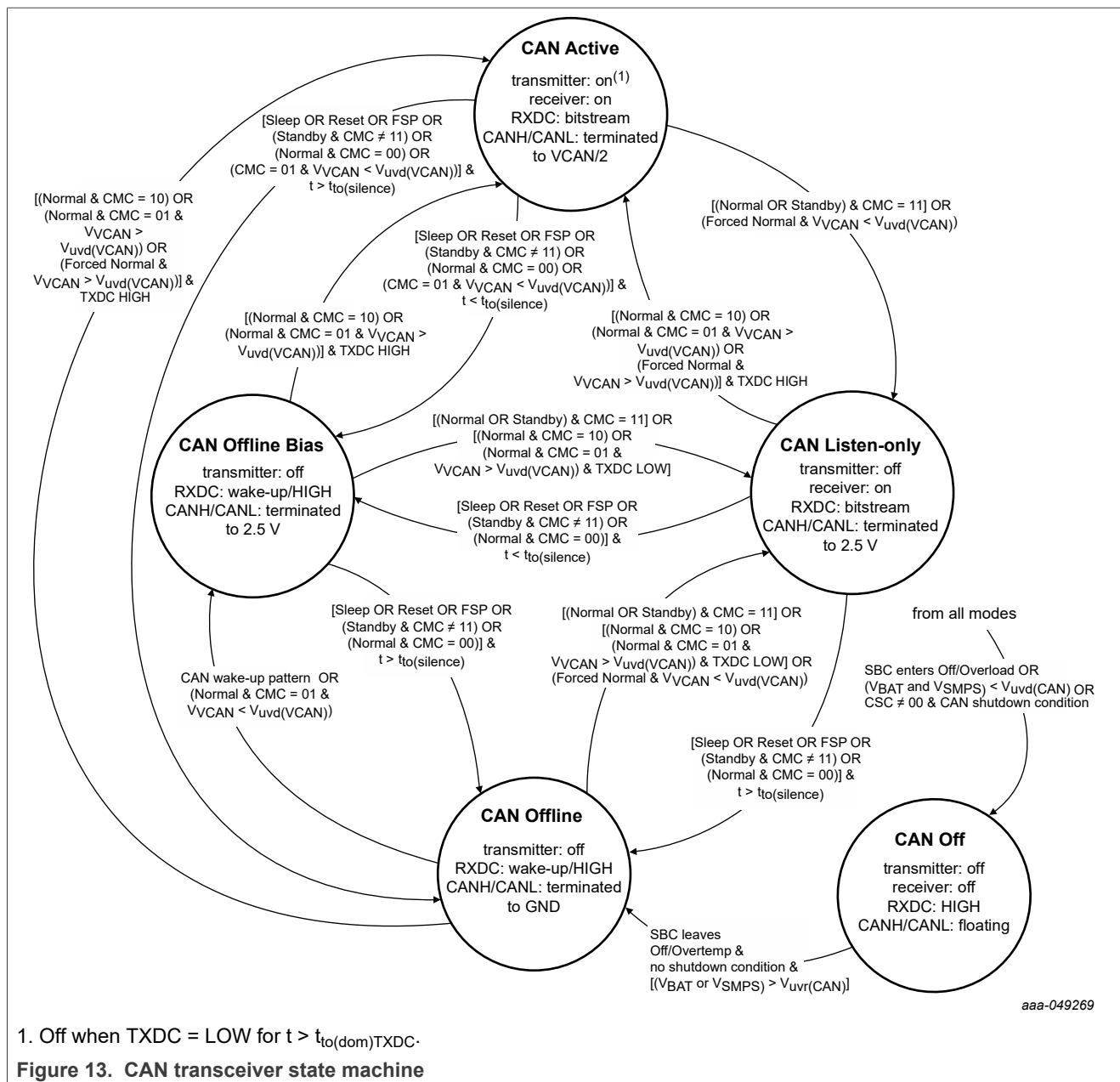
The integrated high-speed CAN transceiver is designed for active communication at bit rates up to 1 Mbit/s (up to 5 Mbit/s in the CAN FD data field), providing differential transmit and receive capability to a CAN protocol controller. The transceiver is ISO 11898-2:2016 compliant. It is supplied via pin VCAN, which can be connected to the output of V2, for example, or to V1 in the 5 V version (UJA113xAHW/5).

The CAN transceiver supports autonomous CAN biasing. When the SBC detects activity on the CAN-bus, it activates autonomous CAN biasing if the CAN transceiver is inactive. This is useful when the node is disabled due to a malfunction in the microcontroller. The SBC ensures that the CAN-bus is correctly biased so that communication is not disturbed by a disabled ECU. The autonomous CAN bias voltage is derived directly from the battery, so it is active even if VCAN is not supplied.

7.8.1 CAN operating modes

The integrated CAN transceiver supports five operating modes: Active, Listen-only, Offline, Offline Bias and Off (see [Figure 13](#)). The CAN transceiver operating mode depends on the UJA113xA operating mode and on the setting of bits CMC in the CAN control register ([Table 1](#)).

When the UJA113xA is in Normal mode, the CAN transceiver operating mode (Active, Listen-only or Offline) can be selected via bits CMC. When the UJA113xA is in Standby or Sleep modes, the transceiver is forced to Offline or Offline Bias mode (depending on bus activity).



7.8.1.1 CAN Active mode

In CAN Active mode, the transceiver can transmit and receive data via CANH and CANL. The differential receiver converts the analog data on the bus lines into digital data, which is output on pin RXDC. The transmitter converts digital data generated by the CAN controller (input on pin TXDC) into analog signals suitable for transmission over the CANH and CANL bus lines.

CAN Active mode is selected when CMC = 01 or 10. When CMC = 01, VCAN undervoltage detection is enabled and the transceiver will go to CAN Offline or CAN Offline Bias mode when the voltage on VCAN drops below the undervoltage detection threshold ($V_{CAN} < V_{uvd}(VCAN)$) for longer than $t_{det(uv)VCAN}$. When CMC = 10, VCAN undervoltage detection is disabled. The transmitter turns off when the SBC leaves Normal mode, e.g. when V1 drops below the V1 reset threshold (selected via bits V1RTC). The SBC will then switch to Reset mode and the transceiver will switch to CAN Offline or CAN Offline Bias mode.

Provided no condition exists to force a transition to CAN off mode (see [Section 7.8.1.4](#)), the CAN transceiver enters and remains in Active mode if:

- the UJA113xA is in Normal mode (MC = 111) and:
 - CMC = 10 (see [Table 36](#)) or
 - CMC = 01 with $V_{VCAN} > V_{uvd(VCAN)}$
- or the UJA113xA is in Forced Normal mode with $V_{VCAN} > V_{uvd(VCAN)}$

If pin TXDC is held LOW (e.g. by a short-circuit to GND) when CAN Active mode is selected via bits CMC, the transceiver will not enter CAN Active mode but will switch to or remain in CAN Listen-only mode. It will remain in Listen-only mode until pin TXDC goes HIGH in order to prevent a hardware and/or software application failure from driving the bus lines to an unwanted dominant state.

In CAN Active mode, the CAN bias voltage is derived from the supply voltage on VCAN.

The application can determine whether the CAN transceiver is ready to transmit/receive data or is disabled by reading the CAN Transceiver Status (CTS) bit in the Transceiver Status Register ([Table 37](#)).

7.8.1.2 CAN Listen-only mode

Listen-only mode enables basic selective wake-up using the CAN protocol controller in the host microcontroller. In Listen-only mode the CAN transmitter is disabled, reducing current consumption. The CAN receiver and CAN biasing remain active. This enables the host microcontroller to switch to a low-power mode in which an embedded CAN protocol controller remains active, waiting for a signal to wake up the microcontroller.

The CAN transceiver is in Listen-only mode when:

- the UJA113xA is in Normal or Standby mode and CMC = 11 OR
- the UJA113xA is in Forced Normal mode and $V_{VCAN} < V_{uvd(VCAN)}$

Note that V_{VCAN} does not need to remain active ($> V_{uvd(VCAN)}$) in CAN Listen-only mode. However, the CAN transceiver will not leave Listen-only mode while TXDC is LOW or if CAN Active mode is selected by setting CMC = 01 while $V_{VCAN} < V_{uvd(VCAN)}$.

7.8.1.3 CAN Offline and Offline Bias modes

In CAN Offline mode, the transceiver monitors the CAN bus for a wake-up event, provided CAN wake-up detection is enabled (CWIE = 1; see [Table 39](#)). CANH and CANL are biased to GND.

CAN Offline Bias mode is the same as CAN Offline mode, with the exception that the CAN bus is biased to 2.5 V. This mode is activated automatically when activity is detected on the CAN bus while the transceiver is in CAN Offline mode. The transceiver will return to CAN Offline mode if the CAN bus is silent (no CAN bus edges) for longer than $t_{to(silence)}$.

The CAN transceiver switches to CAN Offline mode from CAN Active or CAN Listen only mode if:

- the SBC switches to Sleep, Reset or FSP mode OR
- the SBC is in Normal mode and CMC = 00 OR
- the SBC is in Standby mode and CMC = 00, 01 or 10

provided the CAN-bus has been inactive for at least $t_{to(silence)}$. If the CAN-bus has been inactive for less than $t_{to(silence)}$, the CAN transceiver switches first to CAN Offline Bias mode and then to CAN Offline mode once the bus has been silent for $t_{to(silence)}$.

The CAN transceiver switches to CAN Offline/Offline Bias mode from CAN Active mode if CMC = 01 and $V_{VCAN} < V_{uvd(VCAN)}$ or CMC = 10 and the voltage on V1 drops below the V1 reset threshold.

The CAN transceiver switches to CAN Offline mode:

- from CAN Offline Bias mode if no activity is detected on the bus (no CAN edges) for $t > t_{to(silence)}$ OR
- when the SBC switches from Off or Overtemp mode to Reset mode

The CAN transceiver switches from CAN Offline mode to CAN Offline Bias mode if:

- a standard wake-up pattern is detected on the CAN bus OR
- the SBC is in Normal mode, CMC = 01 and $V_{VCAN} < V_{uvd(VCAN)}$

Bit CBSS in the Transceiver status register (Table 37) represents the status of bus activity/silence detection. A timer is started when the CAN transceiver leaves CAN Offline mode. While bus bias is active (i.e. in CAN Offline Bias, CAN Listen-only or CAN Active mode) the timer is (re-)started at each edge of the bus signal. While the timer is running, CBSS is 0. When the timer reaches $t_{to(silence)}$, it stops and CBSS is set to 1

7.8.1.4 CAN Off mode

The CAN transceiver is switched off completely with the bus lines floating when:

- the SBC switches to Off or Overload mode OR
- $CSC \neq 00$ AND CAN shut down condition true OR
- V_{BAT} and V_{SMPS} fall below the CAN receiver undervoltage detection threshold, $V_{uvd(CAN)}$

It is switched on again on entering CAN Offline mode when V_{BAT} or V_{SMPS} is above the undervoltage release threshold ($V_{uvr(CAN)}$) and the SBC is no longer in Off/Overload mode. CAN Off mode prevents reverse currents flowing from the bus when the battery supply to the SBC is lost.

7.8.2 CAN standard wake-up (partial networking not enabled)

If the CAN transceiver is in Offline or Offline Bias mode and CAN wake-up is enabled ($CWIE = 1$), but CAN selective wake-up is disabled ($CPNC = 0$ or $PNCOK = 0$), the UJA113xA will monitor the bus for a wake-up pattern.

A filter at the receiver input prevents unwanted wake-up events occurring due to automotive transients or EMI. A dominant-recessive-dominant wake-up pattern must be transmitted on the CAN bus within the wake-up timeout time ($t_{to(wake)}$) to pass the wake-up filter and trigger a wake-up event (see Figure 14; note that additional pulses may occur between the recessive/dominant phases). The recessive and dominant phases must last at least $t_{wake(busrec)}$ and $t_{wake(busdom)}$, respectively.

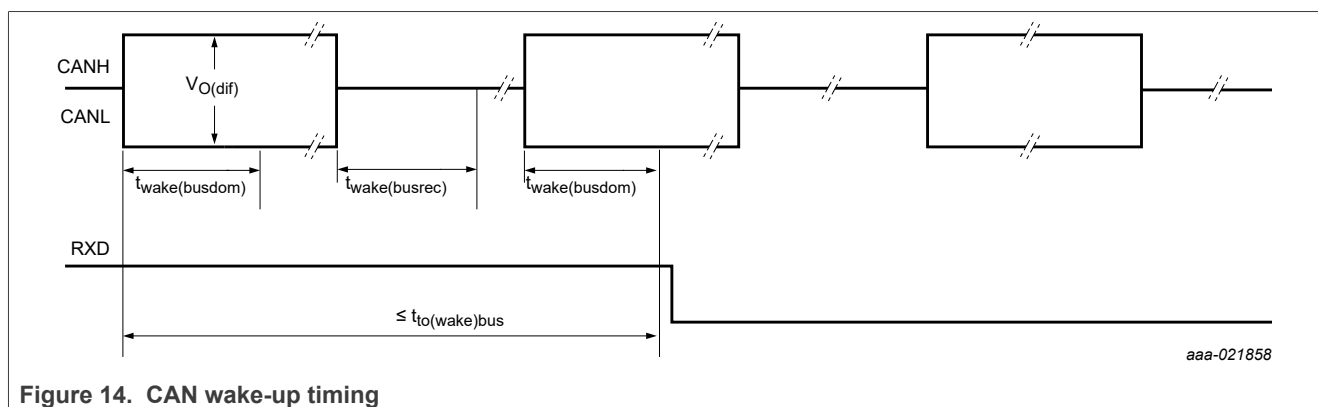


Figure 14. CAN wake-up timing

When a valid CAN wake-up pattern is detected on the bus, CAN wake-up interrupt bit CWI in the Transceiver interrupt status register is set (see Table 38) and pin RXDC is driven LOW. If the SBC was in Sleep mode when the wake-up pattern was detected, V1 is enabled to supply the microcontroller and the SBC switches to Standby mode via Reset mode.

7.8.3 CAN partial networking (UJA113xAHW/xFx only)

Partial networking allows nodes in a CAN network to be selectively activated in response to dedicated wake-up frames (WUF). Only nodes that are functionally required are active on the bus while the other nodes remain in a low-power mode until needed.

If both CAN wake-up detection (CWIE = 1) and CAN selective wake-up (CPNC = 1) are enabled, and the partial networking registers are configured correctly (PNCOK = 1), the transceiver monitors the bus for dedicated CAN wake-up frames.

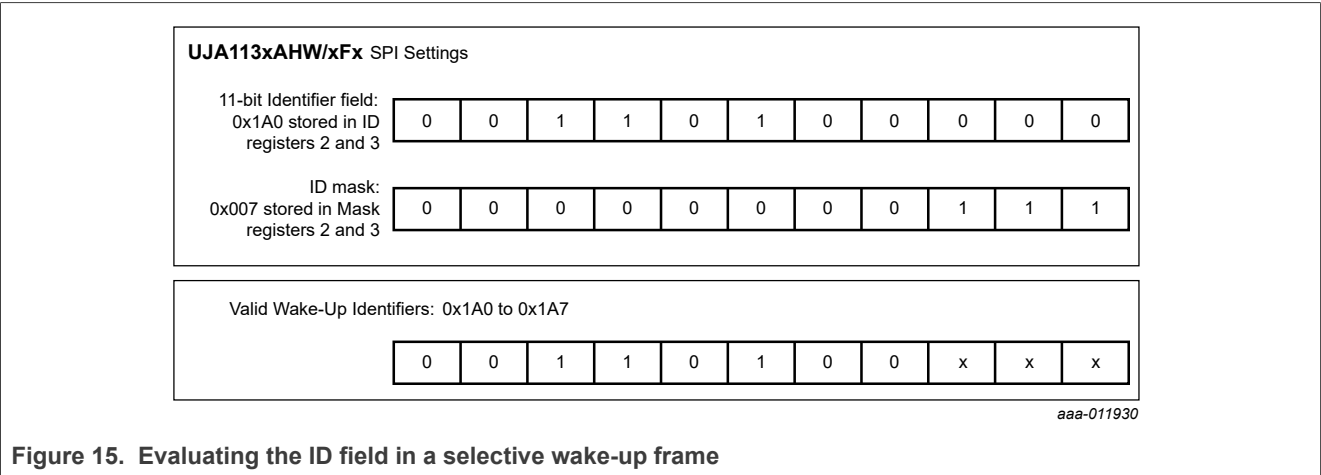
7.8.3.1 Wake-up frame

A wake-up frame is a CAN frame according to ISO11898-1:2003, consisting of an identifier field (ID), a Data Length Code (DLC), a data field and a Cyclic Redundancy Check (CRC) code including the CRC delimiter.

The wake-up frame format, standard (11-bit) or extended (29-bit) identifier, is selected via bit IDE in the Frame control register (Table 44).

A valid WUF identifier is defined and stored in the ID registers (Table 42). An ID mask can be defined to allow a group of identifiers to be recognized as valid by an individual node. The identifier mask is defined in the mask registers (Table 43), where a 1 means ‘don’t care’.

In the example illustrated in Figure 15, based on the standard frame format, the 11-bit identifier is defined as 0x1A0. The identifier is stored in ID registers 2 (0x29) and 3 (0x2A). The three least significant bits of the ID mask, bits 2 to 4 of Mask register 2 (0x2D), are set to 1, which means that the corresponding identifier bits are ‘don’t care’. This means that any of eight different identifiers will be recognized as valid in the received WUF (from 0x1A0 to 0x1A7).



The data field indicates which nodes are to be woken up. Within the data field, groups of nodes can be predefined and associated with bits in a data mask. By comparing the incoming data field with the data mask, multiple groups of nodes can be woken up simultaneously with a single wake-up message.

The data length code (bits DLC in the Frame control register; Table 44) determines the number of data bytes (between 0 and 8) expected in the data field of a CAN wake-up frame. If one or more data bytes are expected (DLC ≠ 0000), at least one bit in the data field of the received wake-up frame must be set to 1 and at least one equivalent bit in the associated data mask register in the transceiver (see Table 45) must also be set to 1 for a successful wake-up. Each matching pair of 1s indicates a group of nodes to be activated (since the data field is up to 8 bytes long, up to 64 groups of nodes can be defined). If DLC = 0, a data field is not expected.

In the example illustrated in Figure 16, the data field consists of a single byte (DLC = 1). This means that the data field in the incoming wake-up frame is evaluated against data mask 7 (stored at address 6Fh; see Table 45

and [Figure 17](#)). Data mask 7 is defined as 10101000 in the example. This means the node is assigned to three groups (Group1, Group 3 and Group 5).

The received message shown in [Figure 16](#) could, potentially, wake up four groups of nodes: groups 2, 3, 4 and 5. Two matches are found (groups 3 and 5) when the message data bits are compared with the configured data mask (DM7).

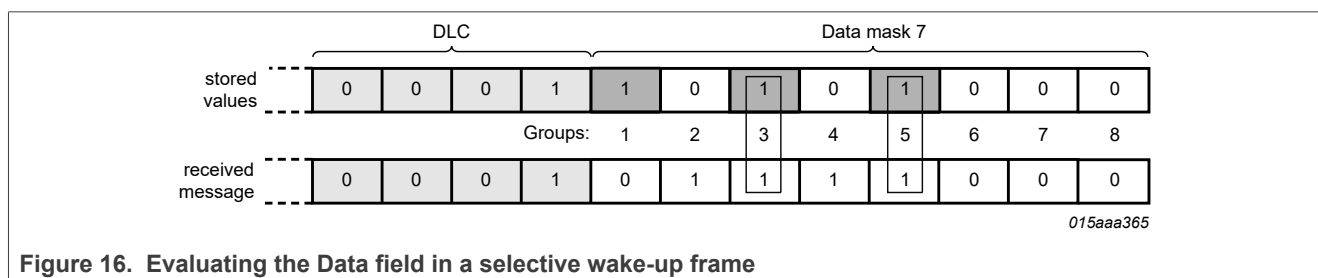


Figure 16. Evaluating the Data field in a selective wake-up frame

Optionally, the data length code and the data field can be excluded from the evaluation of the wake-up frame. If bit PNDM = 0, only the identifier field is evaluated to determine if the frame contains a valid wake-up message. If PNDM = 1 (the default value), the data field is included for wake-up filtering.

When PNDM = 0, a valid wake-up message is detected and a wake-up event is captured (and CW is set to 1) when:

- the identifier field in the received wake-up frame matches the pattern in the ID registers after filtering AND
- the CRC field in the received frame (including a recessive CRC delimiter) was received without error

When PNDM = 1, a valid wake-up message is detected when:

- the identifier field in the received wake-up frame matches the pattern in the ID registers after filtering AND
- the frame is not a Remote frame AND
- the data length code in the received message matches the configured data length code (bits DLC) AND
- if the data length code is greater than 0, at least one bit in the data field of the received frame is set and the corresponding bit in the associated data mask register is also set AND
- the CRC field in the received frame (including a recessive CRC delimiter) was received without error

If the UJA113xAHW/xFx receives a CAN message containing errors (e.g. a 'stuffing' error) that are transmitted in advance of the ACK field, an internal error counter is incremented. If a CAN message is received without any errors appearing in front of the ACK field, the counter is decremented. Data received after the CRC delimiter and before the next Start of Frame (SOF) is ignored by the partial networking module. If the counter overflows (counter > 31), a frame detect error is captured (PNFDEI = 1) and the device wakes up; the counter is reset to zero when the bias is switched off and partial networking is re-enabled.

Partial networking is assumed to be configured correctly when PNCOK is set to 1 by the application software. The UJA113xAHW/xFx clears PNCOK after a write access to any of the CAN partial networking configuration registers (see [Section 7.8.6](#)).

If selective wake-up is disabled (CPNC = 0) or partial networking is not configured correctly (PNCOK = 0), and the CAN transceiver is in Offline mode with wake-up enabled (CWIE = 1), then any valid wake-up pattern according to ISO 11898-2:2016 will trigger a wake-up event.

If the CAN transceiver is not in Offline or Offline Bias mode (CMC ≠ 00) or CAN wake-up is disabled (CWIE = 0), all wake-up patterns on the bus will be ignored.

7.8.3.2 CAN FD frames

CAN FD stands for 'CAN with Flexible Data-Rate'. It is based on the CAN protocol as defined in ISO 11898-1:2015.

CAN FD is being gradually introduced into automotive market. In time, all CAN controllers will be required to comply with the new standard (enabling 'FD-active' nodes) or at least to tolerate CAN FD communication (enabling 'FD-passive' nodes). The UJA113xAHW/xFx supports FD-passive features by means of a dedicated implementation of the partial networking protocol.

The UJA113xAHW/xFx can be configured to recognize CAN FD frames as valid CAN frames. When CFDC = 1, the error counter is decremented every time the control field of a CAN FD frame is received. The UJA113xAHW/xFx remains in low-power mode (CAN FD-passive) with partial networking enabled. CAN FD frames are never recognized as valid wake-up frames, even if PNDM = 0 and the frame contains a valid ID. After receiving the control field of a CAN FD frame, the UJA113xAHW/xFx ignores further bus signals until idle is again detected.

CAN FD passive is supported up to a ratio of one-to-eight between arbitration and data bit rates, without unwanted wake-ups. The CAN FD filter parameter defined in ISO11898-2:2016 and SAE J2284 is supported up to a ratio of one-to-four, with a maximum supported data bit rate of 2 Mbit/s and a maximum arbitration speed of 500 kbit/s.

CAN FD frames are interpreted as frames with errors by the partial networking module when CFDC = 0. So the error counter is incremented when a CAN FD frame is received. If the ratio of CAN FD frames to valid CAN frames exceeds the threshold that triggers error counter overflow, bit PNFDEI is set to 1 and the device wakes up.

7.8.4 Fail-safe features

TXDC dominant time-out

A TXDC dominant time-out timer is started when pin TXDC is forced LOW while the transceiver is in Active Mode. If the LOW state on pin TXDC persists for longer than the TXDC dominant time-out time ($t_{to(dom)TXDC}$), the transmitter is disabled, releasing the bus lines to recessive state. A CAN failure interrupt (CFI) is generated, if enabled (CFIE = 1; see [Table 39](#)).

This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXDC dominant time-out timer is reset when pin TXDC goes HIGH or when the transceiver leaves CAN Active mode. The status of the TXDC dominant time-out can be read via bit CFS in the Transceiver status register ([Table 37](#)). The TXDC dominant time-out time also defines the minimum possible bit rate of 40 kbit/s.

Pull-up on TXDC pin

Pin TXDC has an internal pull-up towards V1 to ensure a safe defined state in case the pin is left floating.

CAN failure interrupt

A CAN failure interrupt is triggered (CFI = 1), if enabled, when status bit VCS (indicating that $V_{VCAN} < V_{uvd}(VCAN)$) or status bit CFS (indicating that pin TXDC is clamped LOW) is set to 1.

CAN shut down in response to a battery under- or overvoltage

The CAN transceiver can be configured to shut down if the battery monitor detects an under- or overvoltage on the battery supply (see [Section 7.7.2](#)). The response of the CAN transceiver (to a BMUI and/or BMOI interrupt) is configured via bits CSC in the CAN control register ([Table 36](#)). This feature makes it possible to reduce current consumption very quickly when the battery supply voltage drops below the undervoltage threshold, and/or to limit power consumption when the battery supply voltage rises above the overvoltage threshold.

7.8.5 CAN transceiver control and status registers

Table 36. CAN control register (address 20h)

Bit	Symbol	Access	Value	Description
7	reserved	R/W	-	always write 0; ignore on read
6	CFDC	R/W	^[1]	CAN FD control:
			0	CAN FD tolerance disabled
			1	CAN FD tolerance enabled
5	PNCOK	R/W	^[1]	CAN partial networking configuration OK:
			0	partial networking register configuration invalid (wake-up via standard wake-up pattern only)
			1	partial networking registers configured successfully
4	CPNC	R/W	^[1]	CAN partial networking control:
			0	disable CAN selective wake-up
			1	enable CAN selective wake-up
3:2	CSC	R/W		CAN shut-down control:
			00	CAN transceiver is not shut down when a battery monitor under- or overvoltage interrupt is generated
			01	CAN transceiver shuts down in response to a battery monitor undervoltage (BMUI) interrupt (SBC in Normal mode)
			10	CAN transceiver shuts down in response to a battery monitor overvoltage (BMOI) interrupt (SBC in Normal mode)
			11	CAN transceiver shuts down in response to a BMUI or BMOI interrupt (SBC in Normal mode)
1:0	CMC	R/W		CAN transceiver operating mode selection (see Section 7.8.1):
			00	Offline/Offline Bias mode
			01	Active mode (when the SBC is in Normal mode); VCAN undervoltage enabled
			10	Active mode (when the SBC is in Normal mode); VCAN undervoltage disabled
			11	Listen-only mode

[1] Valid for UJA113xAHW/xFx variants only; otherwise reserved.

Table 37. Transceiver status register (address 22h)

Bit	Symbol	Access	Value	Description
7	CTS	R		CAN transmitter status:
			0	CAN transmitter disabled
			1	CAN transmitter ready to transmit data

Table 37. Transceiver status register (address 22h)...continued

Bit	Symbol	Access	Value	Description
6	CPNERR	R	[1]	CAN partial networking error:
			0	no CAN partial networking error detected (PNFDEI = 0 AND PNCOK = 1)
			1	CAN partial networking error detected (PNFDEI = 1 OR PNCOK = 0; wake-up via standard wake-up pattern only)
5	CPNS	R	[1]	CAN partial networking status:
			0	CAN partial networking configuration error detected (PNCOK = 0)
			1	CAN partial networking configuration ok (PNCOK = 1)
4	COSCS	R	[1]	CAN oscillator status:
			0	CAN partial networking oscillator not running at target frequency
			1	CAN partial networking oscillator running at target frequency
3	CBSS	R		CAN-bus silence status:
			0	CAN bus silence timer is running (see section Section 7.8.1.3)
			1	CAN bus silence timer is not running (see section Section 7.8.1.3)
2	VLINS	R		LIN supply status:
			0	LIN supply ok in Normal mode or SBC not in Normal mode
			1	LIN switched to Offline mode due to a LIN undervoltage event in Normal mode
1	VCS	R		CAN supply status:
			0	VCAN undervoltage detection is deactivated or the CAN supply is above the undervoltage threshold ($V_{VCAN} > V_{UVD(VCAN)}$) with VCAN undervoltage detection active (it is only active when the SBC is in Normal mode and CMC = 01 or CMC = 11)
			1	CAN supply is below the undervoltage threshold ($V_{VCAN} < V_{UVD(VCAN)}$) with the SBC in Normal mode and CMC = 01 or CMC = 11
0	CFS	R		CAN failure status:
			0	no failure detected or transceiver is not in CAN Active mode
			1	CAN transmitter disabled due to a TXDC dominant time-out event

[1] Valid for UJA113xAHW/xFx variants only; otherwise reserved.

The CAN and LIN (see [Section 7.9](#)) transceiver interrupt status bits are located in the Transceiver interrupt status register, [Table 38](#). The interrupt mechanism is described in [Section 7.12](#).

Table 38. Transceiver interrupt status register (address 63h)

Bit	Symbol	Access	Value	Description
7:6	reserved	R/W	-	always write 00; ignore on read
5	PNFDEI	R/W	0	no partial networking frame detection error detected
			1	partial networking frame detection error detected
4	CBSI	R/W	0	no CAN-bus silence interrupt pending
			1	CAN-bus silence interrupt pending

Table 38. Transceiver interrupt status register (address 63h)...continued

Bit	Symbol	Access	Value	Description
3	LWI2 ^[1]	R/W	0	no LIN2 wake-up interrupt pending
			1	LIN2 wake-up interrupt pending
2	LWI1	R/W	0	no LIN1 wake-up interrupt pending
			1	LIN1 wake-up interrupt pending
1	CFI	R/W	0	no CAN failure interrupt pending
			1	CAN failure interrupt pending
0	CWI	R/W	0	no CAN wake-up interrupt pending
			1	CAN wake-up interrupt pending

[1] UJA1132A and UJA1136A only; bit 3 is reserved in the UJA1131A and UJA1135A.

Transceiver interrupts are enabled/disabled via the Transceiver interrupt enable register, [Table 39](#).

Table 39. Transceiver interrupt enable register (address 23h)

Bit	Symbol	Access	Value	Description
7:5	reserved	R/W	-	always write 000; ignore on read
4	CBSIE	R/W	0	CAN-bus silence interrupt disabled
			1	CAN-bus silence interrupt enabled
3	LWI2E ^[1]	R/W	0	LIN2 wake-up interrupt disabled
			1	LIN2 wake-up interrupt enabled
2	LWI1E	R/W	0	LIN1 wake-up interrupt disabled
			1	LIN1 wake-up interrupt enabled
1	CFIE	R/W	0	CAN failure interrupt disabled
			1	CAN failure interrupt enabled
0	CWIE	R/W	0	CAN wake-up interrupt disabled
			1	CAN wake-up interrupt enabled

[1] UJA1132A and UJA1136A only; bit 3 is reserved in the UJA1131A and UJA1135A.

The influence of SBC operating modes on the CAN transceiver and on the RXDC pin is summarized in [Table 40](#). It also lists the values of associated register bits when these values are predictable according to the SBC operating mode.

Control/configuration bits (writable via SPI) and interrupt bits are (re-)initialized to the default values for the SBC mode. For status bits, the expected value for the SBC mode is indicated. Status bit values in brackets are default values that may not represent the actual status.

Table 40. Influence of SBC operating modes on the CAN transceiver, RXDC pin and on related register bits

Symbol	Off (power-on default)	Forced Normal	Standby	Normal	Sleep	Reset	Overload	FSP
CAN	CAN off	CAN Active/ CAN Listen-only	CAN Offline/ CAN Offline Bias/ CAN	CAN Active/ CAN Offline/ CAN Offline Bias/ CAN	CAN Offline/ CAN Offline Bias	CAN Offline/ CAN Offline Bias	CAN off	CAN Offline/ CAN Offline Bias

Table 40. Influence of SBC operating modes on the CAN transceiver, RXDC pin and on related register bits...continued

Symbol	Off (power-on default)	Forced Normal	Standby	Normal	Sleep	Reset	Overload	FSP
			Listen-only ^[1]	Listen-only/ CAN Off if CAN shut down condition true ^[1]				
RXDC pin	pull-up to V1	CAN status	pull-up to V1; LOW if CAN wake-up; CAN status if CMC = 11	CAN status if CMC = 01/10; otherwise same as Standby	pull-up to V1	pull-up to V1/LOW if CAN wake-up	pull-up to V1	pull-up to V1
CBSI	0	^[2]	-	-	-	-	-	0
CBSIE	0	^[2]	-	-	-	-	-	0
CBSS	1	^[2]	-	-	-	-	-	-
CFI	0	^[2]	-	-	-	-	-	0
CFIE	0	^[2]	-	-	-	-	-	0
CFS	-	^[2]	(0)	-	-	-	-	-
CMC	00	^[2]	-	-	-	-	-	00
CSC	01	^[2]	-	-	-	-	-	-
CTS	-	^[2]	0	-	-	-	-	-
CWI	0	^[2]	-	-	-	-	-	0
CWIE	0	^[2]	-	-	-	-	-	1
VCS	-	^[2]	(0)	-	-	-	-	-

[1] Determined by the setting of bits CMC in the CAN control register.

[2] Register not accessible; reading returns 0.

7.8.6 CAN partial networking configuration registers

Dedicated registers are provided for configuring CAN partial networking.

Table 41. Data rate register (address 26h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R/W	-	always write 00000; ignore on read
2:0	CDR	R/W		CAN data rate selection:
			000	50 kbit/s
			001	100 kbit/s
			010	125 kbit/s
			011	250 kbit/s
			100	reserved (intended for future use; currently selects 500 kbit/s)
			101	500 kbit/s
			110	reserved (intended for future use; currently selects 500 kbit/s)
			111	1000 kbit/s

Table 42. ID registers 0 to 3 (addresses 27h to 2Ah)

Addr.	Bit	Symbol	Access	Value	Description
27h	7:0	ID7:ID0	R/W	-	bits ID7 to ID00 of the extended frame format
28h	7:0	ID15:ID8	R/W	-	bits ID15 to ID8 of the extended frame format
29h	7:2	ID23:ID18	R/W	-	bits ID23 to ID18 of the extended frame format bits ID5 to ID0 of the standard frame format
	1:0	ID17:ID16	R/W	-	bits ID17 to ID16 of the extended frame format
2Ah	7:5	reserved	R/W	-	always write 000; ignore on read
	4:0	ID28:ID24	R/W	-	bits ID28 to ID24 of the extended frame format bits ID10 to ID6 of the standard frame format

Table 43. ID mask registers 0 to 3 (addresses 2Bh to 2Eh)

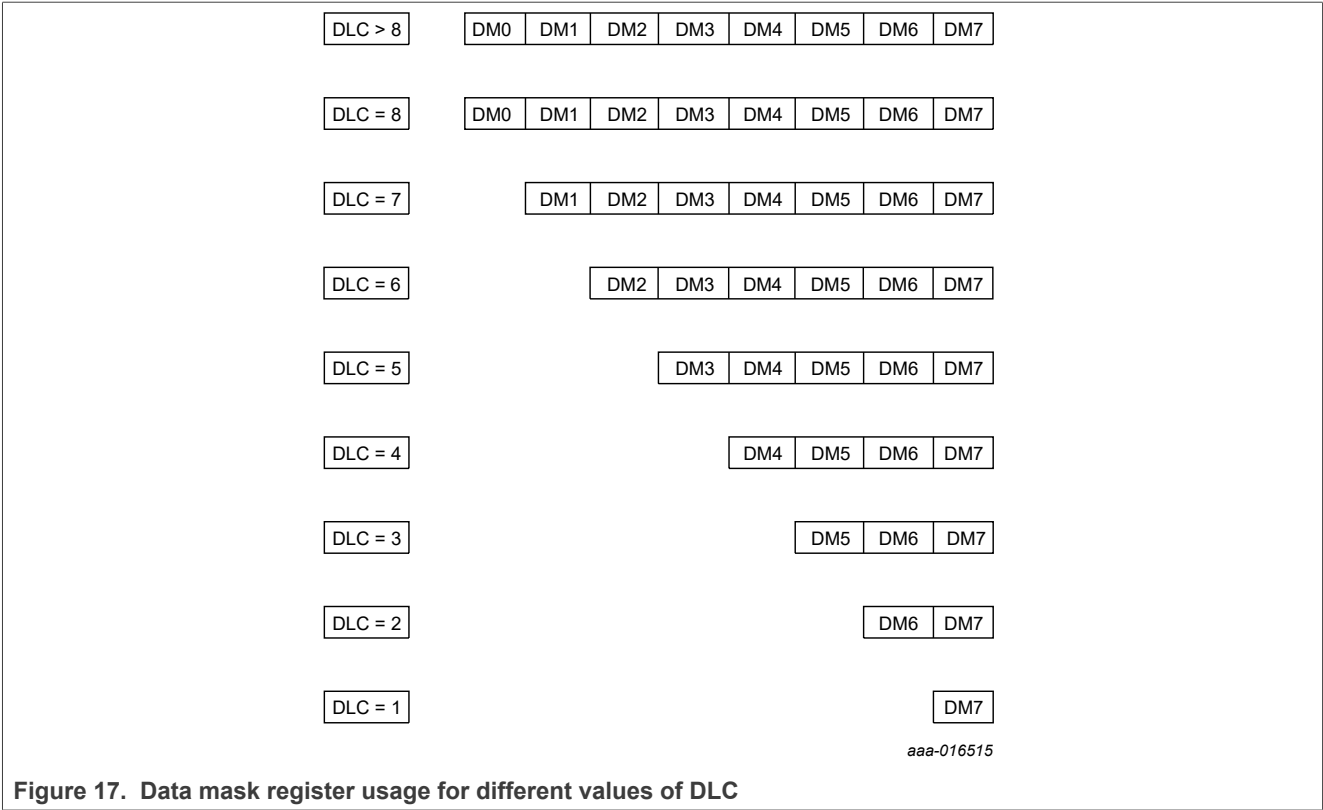
Addr.	Bit	Symbol	Access	Value	Description
2Bh	7:0	IDM7:IDM0	R/W	-	ID mask bits 7 to 0 of extended frame format
2Ch	7:0	IDM15:IDM8	R/W	-	ID mask bits 15 to 8 of extended frame format
2Dh	7:2	IDM23:IDM18	R/W	-	ID mask bits 23 to 18 of extended frame format ID mask bits 5 to 0 of standard frame format
	1:0	IDM17:IDM16	R/W	-	ID mask bits 17 to 16 of extended frame format
2Eh	7:5	reserved	R/W	-	always write 000; ignore on read
	4:0	IDM28:IDM24	R/W	-	ID mask bits 28 to 24 of extended frame format ID mask. bits 10 to 6 of standard frame format

Table 44. Frame control register (address 2Fh)

Bit	Symbol	Access	Value	Description
7	IDE	R/W	-	identifier format:
			0	standard frame format (11-bit)
			1	extended frame format (29-bit)
6	PNDM	R/W	-	partial networking data mask:
			0	data length code and data field are 'don't care' for wake-up
			1	data length code and data field are evaluated at wake-up
5:4	reserved	R/W	-	always write 00; ignore on read
3:0	DLC	R/W		number of data bytes expected in a CAN frame:
			0000	0
			0001	1
			0010	2
			0011	3
			0100	4
			0101	5
			0110	6
			0111	7
			1000	8
			1001 to 1111	tolerated, 8 bytes expected

Table 45. Data mask registers (addresses 68h to 6Fh)

Addr.	Bit	Symbol	Access	Value	Description
68h	7:0	DM0	R/W	-	data mask 0 configuration
69h	7:0	DM1	R/W	-	data mask 1 configuration
6Ah	7:0	DM2	R/W	-	data mask 2 configuration
6Bh	7:0	DM3	R/W	-	data mask 3 configuration
6Ch	7:0	DM4	R/W	-	data mask 4 configuration
6Dh	7:0	DM5	R/W	-	data mask 5 configuration
6Eh	7:0	DM6	R/W	-	data mask 6 configuration
6Fh	7:0	DM7	R/W	-	data mask 7 configuration



Se also [Table 36](#) and [Table 37](#) in [Section 7.8.5](#).

[Table 46](#) lists the values of associated register bits when these values are predictable according to the SBC operating mode.

Control/configuration bits (writable via SPI) and interrupt bits are (re-)initialized to the default values for the SBC mode. For status bits, the expected value for the SBC mode is indicated.

Table 46. Influence of SBC operating modes on register bits related to CAN partial networking.

Symbol	Off (power-on default)	Forced Normal	Standby	Normal	Sleep	Reset	Overload	FSP
CDR	101	[1]	-	-	-	-	-	-
CFDC	0	[1]	-	-	-	-	-	-
COSCS	0	[1]	-	-	-	-	-	-
CPNC	0	[1]	-	-	-	-	-	0
CPNERR	1	[1]	-	-	-	-	-	1
CPNS	0	[1]	-	-	-	-	-	0
DLC	0000	[1]	-	-	-	-	-	-
DMn	11...11	[1]	-	-	-	-	-	-
IDn	00...00	[1]	-	-	-	-	-	-
IDE	0	[1]	-	-	-	-	-	-
IDMn	00...00	[1]	-	-	-	-	-	-
PNDM	1	[1]	-	-	-	-	-	-

Table 46. Influence of SBC operating modes on register bits related to CAN partial networking....continued

Symbol	Off (power-on default)	Forced Normal	Standby	Normal	Sleep	Reset	Overload	FSP
PNFDEI	0	[1]	-	-	-	-	-	0
PNCOK	0	[1]	-	-	-	-	-	0

[1] Register not accessible; reading returns 0.

7.9 LIN transceiver(s)

The LIN transceiver(s) provides the interface between a Local Interconnect Network (LIN) commander/responder protocol controller and the physical bus in a LIN network. It is primarily intended for in-vehicle sub-networks using baud rates from 1 kBd up to 20 kBd.

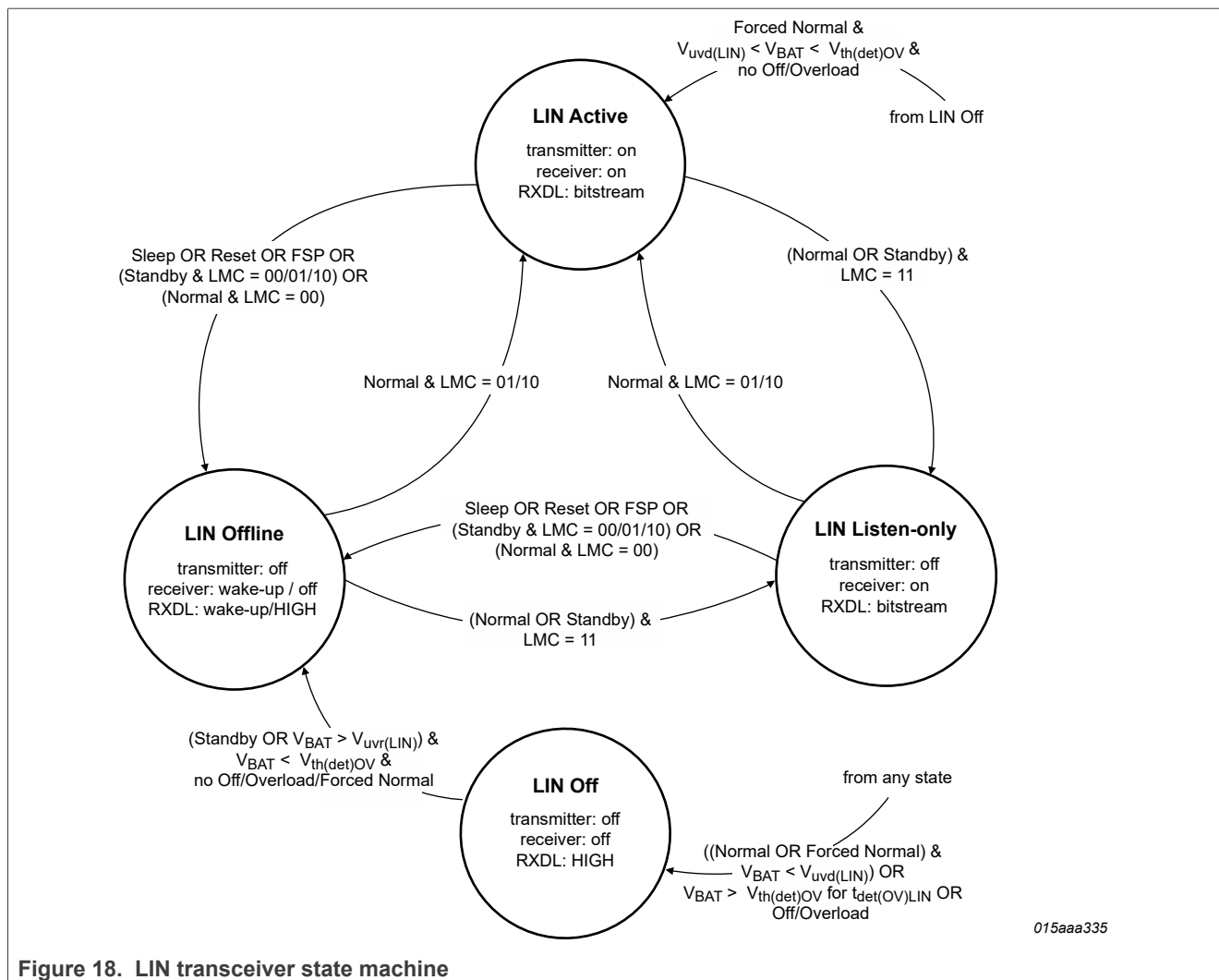
For optimum support of LIN responder applications, the transceiver(s) contains an integrated LIN responder termination resistor (connected between the LIN pin and pin BAT).

7.9.1 LIN2.x/ISO 17987-4:2016 (12 V)/SAE J2602 compliance

The UJA113xA is fully LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, ISO 17987-4:2016 (12 V) and SAE J2602 compliant. The LIN physical layer is independent of higher OSI model layers (e.g. the LIN protocol). Consequently, nodes containing an ISO 17987-4:2016 (12 V) compliant physical layer can be combined, without restriction, with LIN physical layer nodes that comply with earlier revisions (LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3, LIN 2.0, LIN 2.1, LIN 2.2 and LIN 2.2A)

7.9.2 LIN operating modes

The integrated LIN transceiver(s) supports three operating modes: Active, Offline and Listen only. In the UJA1132A and UJA1136A, the dual LIN transceivers can be controlled independently, so one can be active while the other is off.



7.9.2.1 LIN Active mode

In LIN Active mode, the transceiver can transmit and receive data via the LIN bus pins.

The receiver detects data streams on the LIN bus (via pin LINn) and transfers the input data to the microcontroller via pin RXDLn. LIN recessive is represented by a HIGH level on RXDLn; LIN dominant is represented by a LOW level.

Transmit data streams from the protocol controller on the TXDLn input are converted by the transmitters into optimized bus signals shaped to minimize EME.

The LIN transceiver is in Active mode when:

- the SBC is in Normal mode (MC = 111) and the LIN transceiver has been enabled by setting bit LMCn in the LIN mode control register to 01 or 10 (see [Table 2](#)) and the supply voltage on pin BAT is between the LIN undervoltage detection threshold $V_{uvd(LIN)}$ and the SBC overvoltage detection threshold $V_{th(det)OV}$ OR
- the SBC is in Forced Normal mode (FNMC = 1) and the supply voltage on pin BAT is above the LIN undervoltage detection threshold ($V_{BAT} > V_{uvd(LIN)}$)

7.9.2.2 LIN Offline mode

In Offline mode, the LIN transceiver monitors the LIN bus for a remote wake-up event, provided LIN wake-up detection is enabled ($LWInE = 1$; see [Table 39](#)) and $V_{BAT} > V_{uvd(LIN)}$.

A filter at the receiver input prevents automotive transients or EMI triggering invalid wake-up events. A LOW level on the LIN bus lasting at least $t_{wake(dom)LIN}$ followed by a rising edge triggers a remote wake-up event (see [Figure 19](#)). Pin RXDLx is driven LOW and an LWIn interrupt is generated to signal to the microcontroller that a remote wake-up event has been detected. If the SBC is in Sleep mode when the remote-wake up event is triggered, it switches to Standby mode, enabling the microcontroller supply on V1.

The LIN transceiver switches to LIN Offline mode from LIN Active or LIN Listen-only mode when:

- the SBC is in Sleep, Reset or FSP mode OR
- the SBC is in Normal mode with $LMCn = 00$ OR
- the SBC is in Standby mode with $LMCn = 00, 01$ or 10 OR

and from LIN Off mode when:

- the supply voltage on pin BAT is above the LIN undervoltage detection threshold ($V_{BAT} > V_{uvd(LIN)}$) and the SBC is not in Off or Overload mode.

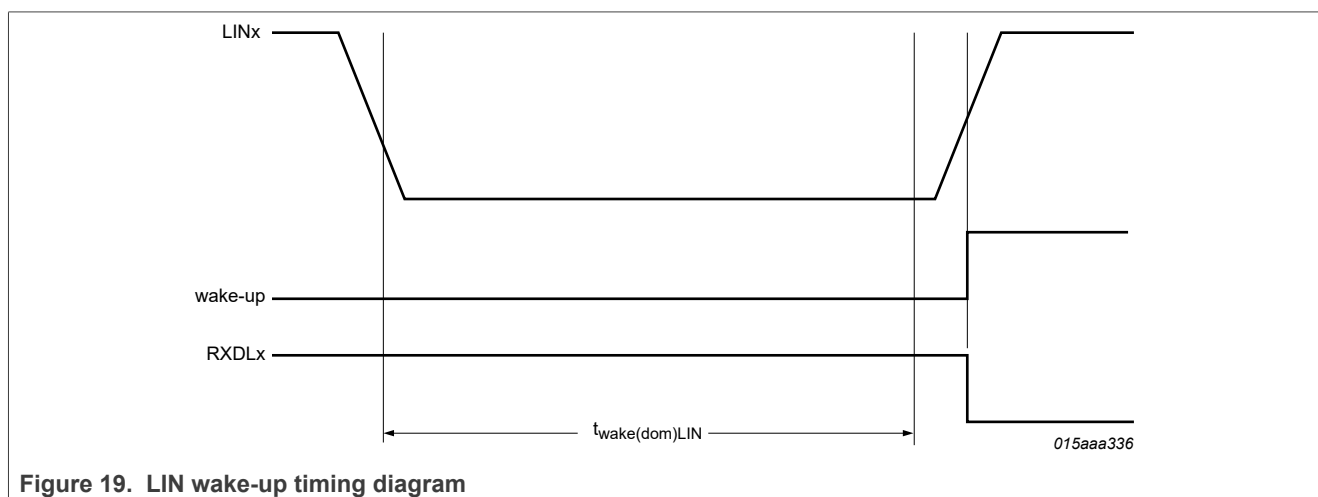


Figure 19. LIN wake-up timing diagram

7.9.2.3 LIN Listen-only mode

In Listen-only mode, the LIN transmitter is disabled. The LIN receiver remains active, allowing the microcontroller to monitor activity on the bus while not transmitting.

The LIN transceiver is in Listen-only mode when:

- the SBC is in Normal or Standby mode AND
- $LMCn = 11$ AND
- the supply voltage on pin BAT is above the LIN undervoltage detection threshold ($V_{BAT} > V_{uvd(LIN)}$)

7.9.2.4 LIN Off mode

The LIN transceiver is switched off completely in LIN Off mode. The bus lines are released and remain in recessive state. The receiver is deactivated and unable to respond to a wake-up pattern. The transceiver switches to LIN Off mode when:

- the SBC switches to Off or Overload mode OR
- $V_{BAT} > V_{th(det)ov}$ for longer than the overvoltage detection time ($t_{det(ov)LIN}$) OR

- V_{BAT} falls below the LIN undervoltage detection threshold, $V_{uvd(LIN)}$, while the SBC is in Normal mode (undervoltage monitoring is switched off in Standby, Sleep and Reset modes)

7.9.3 Fail-safe features

7.9.3.1 General fail-safe features

The following fail-safe features have been implemented:

- Pin TXDLn has an internal pull-up towards V1 to guarantee safe, defined states if this pin is left floating
- The transmitter output stage current is limited in order to protect the transmitter against short circuits to pin BAT
- A loss of power (pins BAT and GND) has no impact on the bus lines or on the microcontroller. No reverse currents flow from the bus.

7.9.3.2 TXDL dominant time-out

A TXDL dominant time-out timer circuit prevents the bus lines being driven to a permanent dominant state (blocking all network communications) if pin TXDLn is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on TXDLn. If the pin remains LOW for longer than the TXDL dominant time-out time ($t_{to(dom)TXDL}$), the transmitter is disabled, driving the bus line to a recessive state. The timer is reset by a positive edge on TXDLn.

This function can be disabled (via bits LSCn; see [Table 47](#)) to allow the UJA113xA to be used in applications requiring the transmission and/or reception of long LOW sequences.

7.9.4 LIN slope control

Automatic slope control has been incorporated into the LIN transmitter, so it is not necessary to select the bit rate.

7.9.5 Operation when supply voltage is outside specified operating range

If $V_{BAT} > 18\text{ V}$ or $V_{BAT} < 5\text{ V}$, the LIN transceiver may remain operational, but parameter values cannot be guaranteed to remain within the operating ranges specified in [Table 104](#) and [Table 105](#).

In LIN Active mode:

- If the input level on pin TXDLn is HIGH, the LIN transmitter output on pin LINn will be recessive.
- If the input level on pin LINn is recessive, the receiver output on pin RXDLn will be HIGH.
- If the voltage on pin V_{BAT} rises to 28 V (e.g. during an automotive jump-start), reliable LIN data transfer is still supported
- If $V_{BAT} < V_{uvd(LIN)}$, the LIN transceiver switches to Off mode (note that LIN undervoltage detection is only active while the SBC is in Normal mode).

7.9.6 LIN transceiver control and status registers

Table 47. LIN control register (address 21h)

Bit	Symbol	Access	Value	Description
7:6	LSC2	R/W	[1]	LIN2 slope control:
			00	slope control active
			01	slope control active

Table 47. LIN control register (address 21h)...continued

Bit	Symbol	Access	Value	Description
			10	slope control active and TXDL dominant time-out deactivated
			11	reserved
5:4	LMC2	R/W	[1]	LIN2 transceiver operating mode selection:
			00	Offline
			01	Active mode (when the SBC is in Normal mode)
			10	Active mode (when the SBC is in Normal mode)
			11	Listen-only mode
3:2	LSC1	R/W		LIN/LIN1 slope control:
			00	slope control active
			01	slope control active
			10	slope control active and TXDL dominant time-out deactivated
			11	reserved
1:0	LMC1	R/W		LIN/LIN1 transceiver operating mode selection:
			00	Offline
			01	Active mode (when the SBC is in Normal mode)
			10	Active mode (when the SBC is in Normal mode)
			11	Listen-only mode

[1] UJA1132A and UJA1136A only; bits 7:4 are reserved in the UJA1131A and UJA1135A and should remain cleared.

See also [Table 37](#), [Table 38](#) and [Table 39](#) in [Section 7.8.5](#).

The influence of SBC operating modes on the LIN transceiver and on the RXDL1/RXDL2 pins is summarized in [Table 48](#). It also lists the values of associated register bits when these values are predictable according to the SBC operating mode.

Control/configuration bits (writable via SPI) and interrupt bits are (re-)initialized to the default values for the SBC mode. For status bits, the expected value for the SBC mode is indicated. Status bit values in brackets are default values that may not represent the actual status.

Table 48. Influence of SBC operating modes on the LIN transceiver, the RXDL1/RXDL2 pins and on related register bits

Symbol	Off (power-on default)	Forced Normal	Standby	Normal	Sleep	Reset	Overload	FSP
LIN1/ LIN2 ^[1]	LIN Off	LIN Active/ LIN Off	LIN Offline/ LIN Listen-only ^[2]	LIN Active/ LIN Listen-only/ LIN Offline ^[3]	LIN Offline	LIN Offline	LIN Off	LIN Offline
RXDL1/ RXDL2 ^[1]	pull-up to V1	LIN status	pull-up to V1; LOW if LIN wake-up; LIN status if LMC = 11	LIN status if LMC = 01/10; otherwise same as Standby	pull-up to V1	pull-up to V1/LOW if LIN wake-up	pull-up to V1	pull-up to V1
LMCn	00	[4]	-	-	-	-	-	-

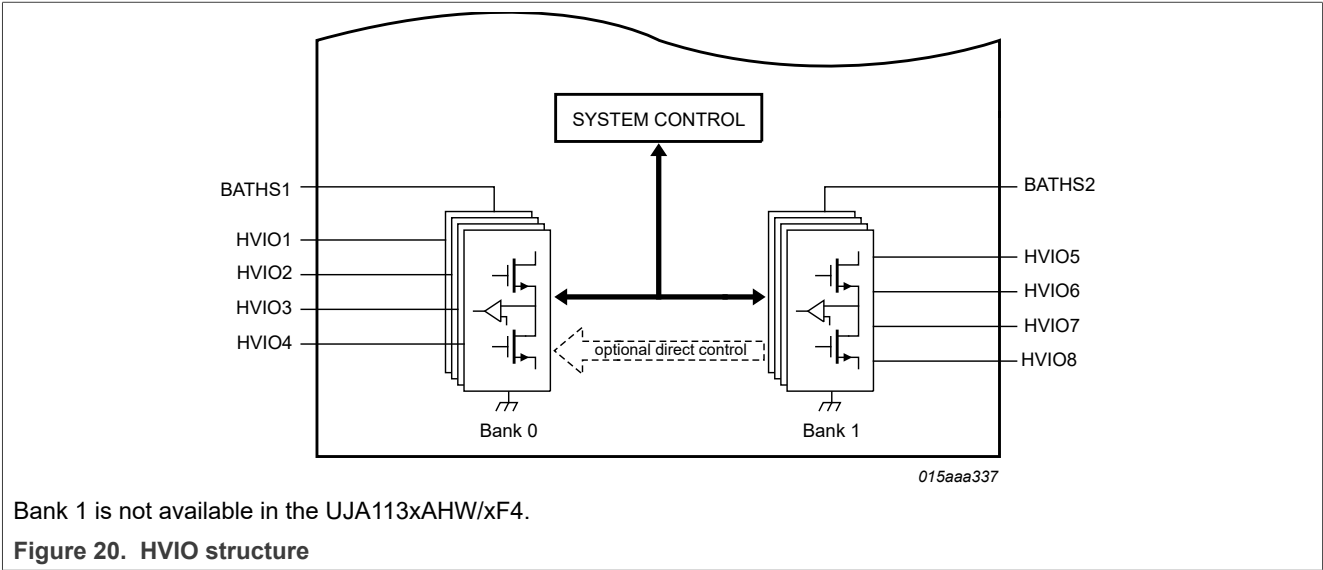
Table 48. Influence of SBC operating modes on the LIN transceiver, the RXDL1/RXDL2 pins and on related register bits...continued

Symbol	Off (power-on default)	Forced Normal	Standby	Normal	Sleep	Reset	Overload	FSP
LSCn	00	[4]	-	-	-	-	-	-
LWIn	0	[4]	-	-	-	-	-	0
LWInE	0	[4]	-	-	-	-	-	1
VLINS	-	[4]	(0)	-	-	-	-	-

[1] Availability of LIN2 depends on the device variant (see Table 1).
[2] Determined by the setting of bits LMCn in the LIN control register (see Table 47).
[3] Determined by the setting of bits LMCn in the LIN control register (see Table 47) or LIN Off.
[4] Register not accessible; reading returns 0.

7.10 High-voltage input/output pins (HVIOs; not available in UJA113xAHW/xF0)

The UJA113xA contains 4 or 8 high-voltage input/output pins (HVIO) that can be configured via the SPI as high- or low-side drivers or as wake-up inputs. They are clustered in 1 or 2 banks of 4 HVIO pins. HVIO1 to HVIO4 belong to bank 0; HVIO5 to HVIO8 belong to bank 1. Each bank has its own dedicated supply pin (BATHS1 and BATHS2 respectively). The BATHSx pins can be supplied independently from the battery, the SMPS or from one of the voltage regulators, provided the supply voltage remains within the specified range. The structure of the HVIOs is depicted in Figure 20.



The high- and low-side drivers allow the HVIOs to be used, for example, to supply sensors or an LED chain or for biasing switches. The HVIOs could be used in combination with the four integrated timers to synchronously bias and sample switches or to generate PWM signals for adjusting the brightness of LEDs. Two or more HVIOs can be combined to form a single output with increased driver capability. In addition, the HVIOs can be configured to generate limp home signals or to control hazard lights.

7.10.1 HVIO configuration

A dedicated control register is provided for each of the 8 HVIO pins (Table 34). Before it can be used, an HVIO pin must first be configured via bits IOnCC. These control bits are used to assign a high-level function to each

of the HVIO pins. If an HVIO pin is not configured (IONCC = 000), the output drivers are off and the input is deactivated. All other control bits are ignored.

Once an HVIO pin has been configured, it can be activated via bits IONAC. An HVIO can be permanently enabled or disabled, or it can be controlled by one of the four integrated timers. If an HVIO is configured as an output driver, the output is activated by each pulse of the associated timer signal. This allows an output to be cyclically activated or controlled by a PWM signal.

Remark: HVIO outputs configured as low-side drivers are only enabled while the SBC is in Normal mode.

If an HVIO is configured as a wake-up input, control bits IONAC define the sampling scheme. If the HVIO is permanently deactivated, then the wake input is never sampled. If the pin is permanently enabled, it is sampled at a rate of $f_{s(wake)}$. If it is controlled by a timer, the sample rate is determined by the frequency of the timer signal (the sample point is at the end of the timer pulse). HVIO control via a timer is depicted in [Figure 21](#).

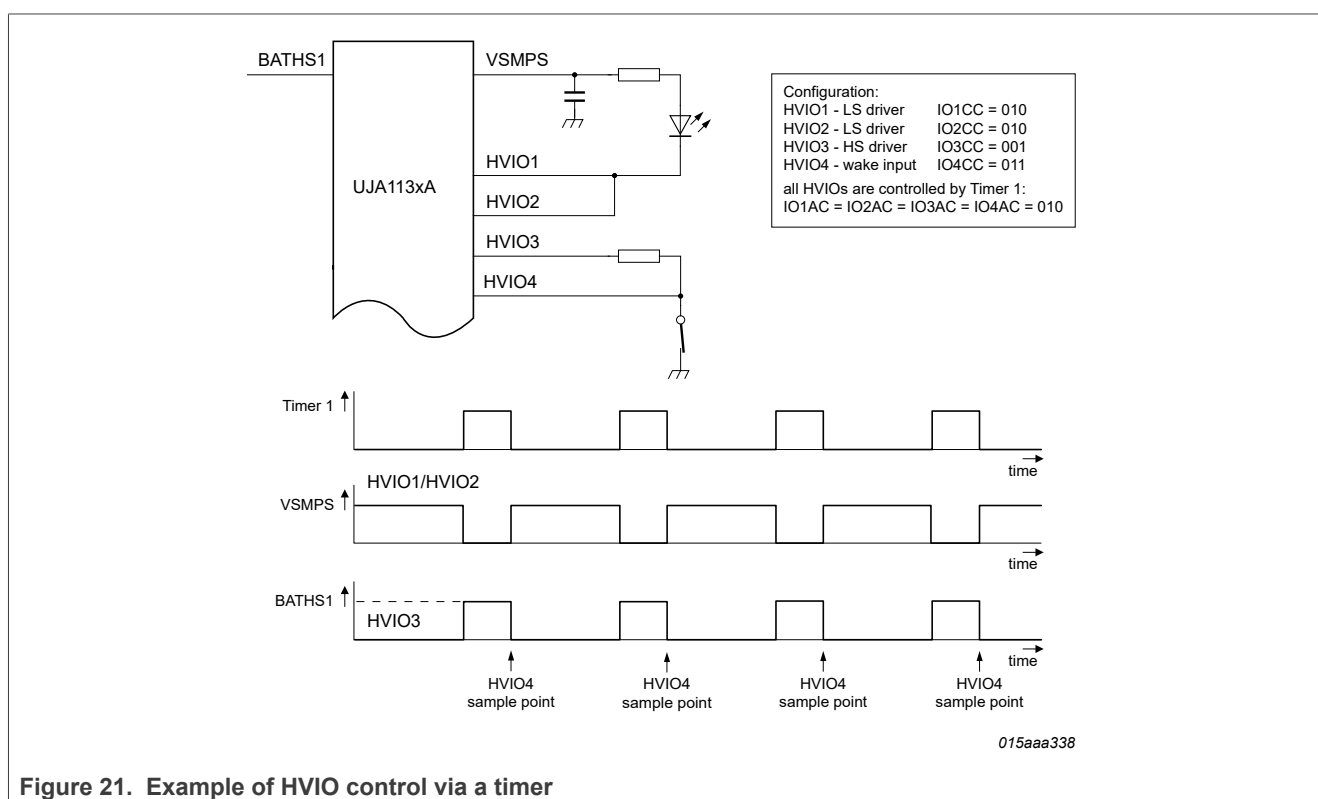


Figure 21. Example of HVIO control via a timer

The wake-up detection threshold can be configured separately for each bank of HVIOs. The threshold can be GND-based or ratiometric to the relevant BATHSx supply voltage. The wake-up thresholds for bank 0 and bank 1 are configured via bits B0WTC and B1WTC, respectively, in the wake-up threshold control registers ([Table 50](#) and [Table 51](#)). Bits IONWLS in the wake-up status registers ([Table 52](#) and [Table 53](#)) can be read to determine whether the input levels on the HVIO pins were above or below the selected threshold when last sampled. Note that the wake-up status information is only valid for HVIOs configured as wake-up inputs.

If the SBC detects a rising or falling edge on an HVIO that is configured as a wake-up input, it generates a wake-up interrupt (IONREI or IONFEI), if enabled (see [Table 66](#) and [Table 68](#)).

7.10.1.1 HVIO slope control

The HVIO output drivers are equipped with a slope control mechanism that can be activated via the IONCC control bits. The purpose of slope control is to minimize electro-magnetic emissions, when necessary.

Low-side driver slope control

When slope control is disabled, the LS-driver behaves as a regular switch: when activated, the on-resistance immediately changes from infinite to $R_{on(HVIO_{n-GND})}$. When slope control is enabled, the LS-driver behaves as a current source: when activated, the output sink current goes from zero to $I_{sink(alt)HVIO}$. The on resistance changes to $R_{on(HVIO_{n-GND})}$ after a fixed delay of $t_{d(on)HVIO}$. This allows the user to adjust the dV/dt on the HVO output by selecting the output capacitance.

HIGH-side driver slope control

When slope control is disabled, the HS-driver behaves as a regular switch: when activated, the on-resistance immediately changes from infinite to $R_{on(BATHSx-HVIO_{n})}$. When slope control is enabled, the HS-driver initially acts as a slope-controlled voltage source. After a fixed time, $t_{d(on)HVIO}$, the HS-driver on-resistance changes to $R_{on(BATHSx-HVIO_{n})}$. This behavior helps to limit the dV/dt on the HVIO output.

7.10.2 Direct control of HVIOs (only valid for variants with 8 HVIO pins)

The direct control feature allows an HVIO on bank 0 to be controlled directly from an HVIO on bank 1 (without involving the SPI interface). The controlled HVIO on bank 0 must be configured as a high- or low-side driver and the 'direct control' option must be selected ($IONAC = 110$ for inverted control or $IONAC = 111$ for non-inverted control). Input and output assignment is fixed - HVIO_n of bank 0 is assigned to HVIO_(n+4) of bank 1.

The 'controlling' HVIO on bank 1 does not need to be activated. It only needs an input configuration (wake-up input or HS-driver and wake-up input). However, it will need to be activated before its status can be read or associated interrupts enabled.

The direct control pairings can be individually enabled and the configuration of one HVIO pair has no impact on other HVIO functions.

Note that the direct control option is not available for HVIO2, HVIO3 or HVIO4 if they are configured as limp home outputs in MTPNV memory (see [Section 7.10.6](#)).

7.10.3 Short-circuit and open load detection

The HVIO output drivers are protected against short circuits and open loads.

When a short circuit is detected on an HVIO, the output driver is automatically deactivated. A short-circuit failure is reported via the driver status register (bits $IONDS = 10$; see [Table 54](#) and [Table 55](#)). To reactivate the HVIO, the associated activation control bits must be reset to 000 (bits $IONAC$; see [Table 34](#)), which clears the driver status bits ($IONDS = 00$; driver is OK). The HVIO can then be reactivated (again via bits $IONAC$, as described in [Section 7.10.1](#)). If the short circuit is still present, the HVIO is again deactivated. The HVIO short-circuit thresholds can be set individually via bits $IONSCTC$ (see [Table 56](#) and [Table 58](#)).

The UJA113xA is also able to detect open-load failures. However, in contrast to the response to a short-circuit, the output driver is not deactivated when an open load is detected. The open-load failure is reported via the driver status register (bits $IONDS = 01$; see [Table 54](#) and [Table 55](#)). The relevant status bit remains set to 01 until the driver current rises above the open-load threshold. The HVIO open-load detection thresholds can be set individually via bits $IONOLTC$ (see [Table 57](#) and [Table 59](#)).

If the SBC detects an HVIO short-circuit or open-load failure, an $IONSCI$ or $IONOLI$ interrupt is generated, if enabled (see [Section 7.12](#)). If the UJA113xA is in Sleep mode, the interrupt triggers a wake-up event.

Note that short-circuit/open-load detection is only enabled when an HVIO driver is switched on. When an HVIO is controlled by a timer, diagnostic status information is updated when the driver switches on.

A minimum HVIO on-time is required for open-load failure detection. A failure may not be detected if the on-time is less than $t_{det(fail)HVIO}$ due to a short duty cycle. Once a failure has been detected, an open load failure

is reported (IONDS = 01). The open load failure is automatically recovered when the current the HVIO pin is driving exceeds the open-load threshold for the HVIO failure recovery time $t_{\text{rec(HVIO)}}$.

Note that positive currents flow into the IC and negative currents flow out of the IC - so both positive and negative thresholds are defined. For a LS-driver, the open-load threshold is exceeded when the driving current is above the positive threshold ($> I_{\text{th(det)open}}$; see [Table 104](#)). For a HS-driver, the open-load threshold is exceeded when the driving current is below the negative threshold ($< I_{\text{th(det)open}}$).

7.10.4 Automatic load shedding

It may be desirable to deactivate the HVIOs as soon as possible in response to a battery under- or overvoltage event. For an overvoltage, this feature can prevent overload conditions in the SBC or in external loads. For an undervoltage, it can help maintain the charge in the battery capacitor to keep the module operational for as long as possible.

The UJA113xA provides the option to deactivate the HVIO ports individually (input or output) in the event of an under- or overvoltage. This option helps to reduce the reaction time without burdening the microcontroller.

The HVIOs are configured via bits IONSC in the HVION control registers (see [Table 34](#)). The under- and overvoltage thresholds are defined by the battery monitor thresholds, BMOTC and BMUTC (see [Section 7.7.2](#)). HVIO ports are automatically reactivated when the under- or overvoltage condition is removed. Note that shutdown control is only active while the SBC is in Normal Mode.

The HVIOs switch to a fail-safe state when the SBC enters Overload mode (see [Section 7.1.1.5](#)). For HVIOs configured as limp-home outputs (HVIO2, HVIO3, and/or HVIO4; see [Section 7.10.6](#)), the selected limp-home functions are activated when the HVIOs switch to fail-safe state. Otherwise, the HVIO drivers are de-activated.

When the SBC enters Overload mode (see [Section 7.1.1.5](#)), the HVIOs switch to a fail-safe state defined as:

- For HVIOs configured as limp-home outputs (HVIO2, HVIO3, and/or HVIO4; see [Section 7.10.6](#)), the selected limp-home functions are activated when the HVIOs switch to fail-safe state.
- Otherwise, the HVIO drivers are de-activated.

7.10.5 Safety features

For certain applications it can be critical to ensure that an HVIO high- or low-side driver is not activated accidentally. To prevent this happening, a driver can be deactivated via bits IONHOC and IONLOC in non-volatile memory (see [Table 60](#) and [Table 61](#)). Non-volatile memory settings have the highest priority. That means that conflicting SPI register settings in standard memory are overruled.

7.10.6 HVIO pins configured as limp home outputs

The LIMP pin is provided to enable 'limp home' hardware in the event of an ECU failure (see [Section 7.5](#)). Pins HVIO2, HVIO3 and HVIO4 can be used to provide additional limp home functionality. When the limp home control bit is set (LHC = 1; see [Table 16](#)), the following functions are supported:

- HVIO2 can be configured as a statically active high-side driver
- HVIO3 can be configured as a high-side switch supplying a 100 Hz PWM signal with a 10 % duty cycle
- HVIO4 can be configured as a high-side switch supplying a 1.25 Hz PWM signal with a 50 % duty cycle

Bit LHC is set automatically in Overload and FSO modes but can also be set via the SPI.

Limp home functionality is enabled for the HVIO pins via the IONSFC control bits in the Start-up control register ([Table 14](#)). The Start-up control register is located in the non-volatile memory bank so this function can be enabled automatically at power-on. When HVIO2, HVIO3 and HVIO4 are configured as limp home outputs, the bit settings in the dedicated control registers are ignored.

Timer 3 and Timer 4 provide the clock signals for HVIO3 and HVIO4, respectively. When these HVIOs are configured as limp home outputs (LHC = 1; IOnSFC = 1), the timers are dedicated to the HVIOs and cannot be used for any other purpose. Timer 3 and Timer 4 control settings are ignored (see [Section 7.11](#)).

Short-circuit and open-load detection is enabled for HVIO2, HVIO3 and HVIO4 when they are configured as limp home outputs. The HVIO output driver is deactivated when a short-circuit is detected. In order to recover from a short-circuit failure, the HVIO must be deactivated and reactivated via the SPI by resetting and then setting bit LHC. The short-circuit and open-load detection thresholds are defined in the corresponding control registers (see [Section 7.10.7](#)).

Note that when an HVIO is configured as a limp home output, its high-side driver should not be deactivated via bit IOnHOC in non-volatile memory (see [Table 60](#)).

7.10.7 HVIO control and status registers

HVIO control and status registers are not available in the UJA113xAHW/xF0. HVIO bank 1 (HVIO5 to HVIO 8) registers are not available in the UJA113xAHW/xFx.

Table 49. HVION control registers^[1]

Bit	Symbol	Access	Value	Description
7:6	IOnSC	R/W		HVION shutdown control:
			00	HVION does not respond to a battery over- or undervoltage
			01	HVION shuts down when battery undervoltage is detected in Normal mode
			10	HVION shuts down when battery overvoltage is detected in Normal mode
			11	HVION shuts down when battery over- or undervoltage is detected in Normal mode
5:3	IOnAC	R/W		HVION activation control:
			000	HVION is deactivated
			001	HVION is enabled
			010	HVION is controlled by Timer 1
			011	HVION is controlled by Timer 2
			100	HVION is controlled by Timer 3
			101	HVION is controlled by Timer 4
			110	HVION is controlled by HVION+4 (inverted control; only available for bank 0)
			111	HVION is controlled by HVION+4 (non-inverted control; only available for bank 0)
2:0	IOnCC	R/W		HVION configuration control:
			000	HVION is off
			001	HVION is configured as a HS-driver with slope control
			010	HVION is configured as a LS-driver with slope control
			011	HVION is configured as a wake-up input
			100	HVION is configured as a HS-driver and wake-up input with slope control
			101	HVION is configured as a HS-driver without slope control
			110	HVION is configured as a LS-driver without slope control

Table 49. HVIO control registers^[1] ...continued

Bit	Symbol	Access	Value	Description
			111	HVIO is configured as a HS-driver and wake-up input without slope control

[1] Addresses 30h to 33h for HVIO1 to HVIO4 respectively; addresses 40h to 43h for HVIO5 to HVIO8.

Table 50. Bank 0 (HVIO1 to HVIO4) wake-up threshold control register (address 34h)

Bit	Symbol	Access	Value	Description
7:1	reserved	R/W	-	always write all 0s; ignore on read
0	B0WTC	R/W		bank 0 wake-up threshold configuration:
			0	threshold is ratiometric to V_{BATHS1}
			1	threshold is absolute

Table 51. Bank 1 (HVIO5 to HVIO8) wake-up threshold control register (address 44h)

Bit	Symbol	Access	Value	Description
7:1	reserved	R/W	-	always write all 0s; ignore on read
0	B1WTC	R/W		bank 1 wake-up threshold configuration:
			0	threshold is ratiometric to V_{BATHS2}
			1	threshold is absolute

Table 52. Bank 0 wake-up status register (address 35h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	-	ignore on read
3	IO4WLS	R		status of input voltage on HVIO4:
			0	the input voltage is below the selected wake-up threshold
			1	the input voltage is above the selected wake-up threshold
2	IO3WLS	R		status of input voltage on HVIO3:
			0	the input voltage is below the selected wake-up threshold
			1	the input voltage is above the selected wake-up threshold
1	IO2WLS	R		status of input voltage on HVIO2:
			0	the input voltage is below the selected wake-up threshold
			1	the input voltage is above the selected wake-up threshold
0	IO1WLS	R		status of input voltage on HVIO1:
			0	the input voltage is below the selected wake-up threshold
			1	the input voltage is above the selected wake-up threshold

Table 53. Bank 1 wake-up status register (address 45h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	-	ignore on read
3	IO8WLS	R		status of input voltage on HVIO8:
			0	the input voltage is below the selected wake-up threshold
			1	the input voltage is above the selected wake-up threshold
2	IO7WLS	R		status of input voltage on HVIO7:
			0	the input voltage is below the selected wake-up threshold
			1	the input voltage is above the selected wake-up threshold
1	IO6WLS	R		status of input voltage on HVIO6:
			0	the input voltage is below the selected wake-up threshold
			1	the input voltage is above the selected wake-up threshold
0	IO5WLS	R		status of input voltage on HVIO5:
			0	the input voltage is below the selected wake-up threshold
			1	the input voltage is above the selected wake-up threshold

Table 54. Bank 0 driver status register (address 36h)

Bit	Symbol	Access	Value	Description
7:6	IO4DS	R		HVIO4 driver status:
			00	HVIO4 driver is ok
			01	open load on HVIO4
			10	short circuit on HVIO4
			11	HVIO4 driver is off
5:4	IO3DS	R		HVIO3 driver status:
			00	HVIO3 driver is ok
			01	open load on HVIO3
			10	short circuit on HVIO3
			11	HVIO3 driver is off
3:2	IO2DS	R		HVIO2 driver status:
			00	HVIO2 driver is ok
			01	open load on HVIO2
			10	short circuit on HVIO2
			11	HVIO2 driver is off
1:0	IO1DS	R		HVIO1 driver status:
			00	HVIO1 driver is ok
			01	open load on HVIO1
			10	short circuit on HVIO1
			11	HVIO1 driver is off

Table 55. Bank 1 driver status register (address 46h)

Bit	Symbol	Access	Value	Description
7:6	IO8DS	R		HVIO8 driver status:
			00	HVIO8 driver is ok
			01	open load on HVIO8
			10	short circuit on HVIO8
			11	HVIO8 driver is off
5:4	IO7DS	R		HVIO7 driver status:
			00	HVIO7 driver is ok
			01	open load on HVIO7
			10	short circuit on HVIO7
			11	HVIO7 driver is off
3:2	IO6DS	R		HVIO6 driver status:
			00	HVIO6 driver is ok
			01	open load on HVIO6
			10	short circuit on HVIO6
			11	HVIO6 driver is off
1:0	IO5DS	R		HVIO5 driver status:
			00	HVIO5 driver is ok
			01	open load on HVIO5
			10	short circuit on HVIO5
			11	HVIO5 driver is off

Table 56. Bank 0 short-circuit detection threshold control register (address 39h)

Bit	Symbol	Access	Value	Description
7:6	IO4SCTC	R/W		HVIO4 short-circuit detection threshold, see Table 104 :
			00	$I_{th(det)sc}$ condition 00
			01	$I_{th(det)sc}$ condition 01
			10	$I_{th(det)sc}$ condition 10
			11	$I_{th(det)sc}$ condition 11
5:4	IO3SCTC	R/W		HVIO3 short-circuit threshold, see Table 104 :
			00	$I_{th(det)sc}$ condition 00
			01	$I_{th(det)sc}$ condition 01
			10	$I_{th(det)sc}$ condition 10
			11	$I_{th(det)sc}$ condition 11
3:2	IO2SCTC	R/W		HVIO2 short-circuit threshold, see Table 104 :
			00	$I_{th(det)sc}$ condition 00
			01	$I_{th(det)sc}$ condition 01

Table 56. Bank 0 short-circuit detection threshold control register (address 39h)...continued

Bit	Symbol	Access	Value	Description
1:0	IO1SCTC	R/W	10	$I_{th(det)sc}$ condition 10
			11	$I_{th(det)sc}$ condition 11
				HVIO1 short-circuit threshold, see Table 104 :
			00	$I_{th(det)sc}$ condition 00
			01	$I_{th(det)sc}$ condition 01
			10	$I_{th(det)sc}$ condition 10
			11	$I_{th(det)sc}$ condition 11

Table 57. Bank 0 open-load detection threshold control register (address 3Ah)

Bit	Symbol	Access	Value	Description
7:6	IO4OLTC	R/W		HVIO4 open-load threshold, see Table 104 :
			00	$I_{th(det)open}$ condition 00
			01	$I_{th(det)open}$ condition 01
			10	$I_{th(det)open}$ condition 10
			11	$I_{th(det)open}$ condition 11
5:4	IO3OLTC	R/W		HVIO3 open-load threshold, see Table 104 :
			00	$I_{th(det)open}$ condition 00
			01	$I_{th(det)open}$ condition 01
			10	$I_{th(det)open}$ condition 10
			11	$I_{th(det)open}$ condition 11
3:2	IO2OLTC	R/W		HVIO2 open-load threshold, see Table 104 :
			00	$I_{th(det)open}$ condition 00
			01	$I_{th(det)open}$ condition 01
			10	$I_{th(det)open}$ condition 10
			11	$I_{th(det)open}$ condition 11
1:0	IO1OLTC	R/W		HVIO1 open-load threshold, see Table 104 :
			00	$I_{th(det)open}$ condition 00
			01	$I_{th(det)open}$ condition 01
			10	$I_{th(det)open}$ condition 10
			11	$I_{th(det)open}$ condition 11

Table 58. Bank 1 short-circuit detection threshold control register (address 49h)

Bit	Symbol	Access	Value	Description
7:6	IO8SCTC	R/W		HVIO8 short-circuit threshold, see Table 104 :
			00	$I_{th(det)sc}$ condition 00

Table 58. Bank 1 short-circuit detection threshold control register (address 49h)...continued

Bit	Symbol	Access	Value	Description
			01	$I_{th(det)sc}$ condition 01
			10	$I_{th(det)sc}$ condition 10
			11	$I_{th(det)sc}$ condition 11
5:4	IO7SCTC	R/W		HVIO7 short-circuit threshold, see Table 104 :
			00	$I_{th(det)sc}$ condition 00
			01	$I_{th(det)sc}$ condition 01
			10	$I_{th(det)sc}$ condition 10
			11	$I_{th(det)sc}$ condition 11
3:2	IO6SCTC	R/W		HVIO6 short-circuit threshold, see Table 104 :
			00	$I_{th(det)sc}$ condition 00
			01	$I_{th(det)sc}$ condition 01
			10	$I_{th(det)sc}$ condition 10
			11	$I_{th(det)sc}$ condition 11
1:0	IO5SCTC	R/W		HVIO5 short-circuit threshold, see Table 104 :
			00	$I_{th(det)sc}$ condition 00
			01	$I_{th(det)sc}$ condition 01
			10	$I_{th(det)sc}$ condition 10
			11	$I_{th(det)sc}$ condition 11

Table 59. Bank 1 open-load detection threshold control register (address 4Ah)

Bit	Symbol	Access	Value	Description
7:6	IO8OLTC	R/W		HVIO8 open-load threshold, see Table 104 :
			00	$I_{th(det)open}$ condition 00
			01	$I_{th(det)open}$ condition 01
			10	$I_{th(det)open}$ condition 10
			11	$I_{th(det)open}$ condition 11
5:4	IO7OLTC	R/W		HVIO7 open-load threshold, see Table 104 :
			00	$I_{th(det)open}$ condition 00
			01	$I_{th(det)open}$ condition 01
			10	$I_{th(det)open}$ condition 10
			11	$I_{th(det)open}$ condition 11
3:2	IO6OLTC	R/W		HVIO6 open-load threshold, see Table 104 :
			00	$I_{th(det)open}$ condition 00
			01	$I_{th(det)open}$ condition 01
			10	$I_{th(det)open}$ condition 10
			11	$I_{th(det)open}$ condition 11

Table 59. Bank 1 open-load detection threshold control register (address 4Ah)...continued

Bit	Symbol	Access	Value	Description
1:0	IO5OLTC	R/W		HVIO5 open-load threshold, see Table 104 :
			00	$I_{th(det)open}$ condition 00
			01	$I_{th(det)open}$ condition 01
			10	$I_{th(det)open}$ condition 10
			11	$I_{th(det)open}$ condition 11

Table 60. HVIO high-side driver control register (address 71h)

This table is located in non-volatile memory with restricted write access.

Bit	Symbol	Access	Value	Description
7	IO8HOC	R/W		HVIO8 high-side driver control:
			0 ^{[1][2]}	HVIO8 high-side driver is controlled by the setting in the HVIO8 control register
			1	HVIO8 high-side driver is off, regardless of the setting in the HVIO8 control register
6	IO7HOC	R/W		HVIO7 high-side driver control:
			0 ^{[1][2]}	HVIO7 high-side driver is controlled by the setting in the HVIO7 control register
			1	HVIO7 high-side driver is off, regardless of the setting in the HVIO7 control register
5	IO6HOC	R/W		HVIO6 high-side driver control:
			0 ^{[1][2]}	HVIO6 high-side driver is controlled by the setting in the HVIO6 control register
			1	HVIO6 high-side driver is off, regardless of the setting in the HVIO6 control register
4	IO5HOC	R/W		HVIO5 high-side driver control:
			0 ^{[1][2]}	HVIO5 high-side driver is controlled by the setting in the HVIO5 control register
			1	HVIO5 high-side driver is off, regardless of the setting in the HVIO5 control register
3	IO4HOC	R/W		HVIO4 high-side driver control:
			0 ^{[1][2]}	HVIO4 high-side driver is controlled by the setting in the HVIO4 control register
			1	HVIO4 high-side driver is off, regardless of the setting in the HVIO4 control register
2	IO3HOC	R/W		HVIO3 high-side driver control:
			0 ^{[1][2]}	HVIO3 high-side driver is controlled by the setting in the HVIO3 control register
			1	HVIO3 high-side driver is off, regardless of the setting in the HVIO3 control register
1	IO2HOC	R/W		HVIO2 high-side driver control:

Table 60. HVIO high-side driver control register (address 71h)...*continued**This table is located in non-volatile memory with restricted write access.*

Bit	Symbol	Access	Value	Description
0	IO1HOC	R/W	0 ^{[1][2]}	HVIO2 high-side driver is controlled by the setting in the HVIO2 control register
			1	HVIO2 high-side driver is off, regardless of the setting in the HVIO2 control register
				HVIO1 high-side driver control:
			0 ^{[1][2]}	HVIO1 high-side driver is controlled by the setting in the HVIO1 control register
			1	HVIO1 high-side driver is off, regardless of the setting in the HVIO1 control register

[1] Factory preset value.

[2] Value should always be 0 for variants without this pin. This is taken into account for CRC calculations.

Table 61. HVIO low-side driver control register (address 72h)*This table is located in non-volatile memory with restricted write access.*

Bit	Symbol	Access	Value	Description
7	IO8LOC	R/W		HVIO8 low-side driver control:
			0 ^[1]	HVIO8 low-side driver is controlled by the setting in the HVIO8 control register
			1	HVIO8 low-side driver is off, regardless of the setting in the HVIO8 control register
6	IO7LOC	R/W		HVIO7 low-side driver control:
			0 ^[1]	HVIO7 low-side driver is controlled by the setting in the HVIO7 control register
			1	HVIO7 low-side driver is off, regardless of the setting in the HVIO7 control register
5	IO6LOC	R/W		HVIO6 low-side driver control:
			0 ^[1]	HVIO6 low-side driver is controlled by the setting in the HVIO6 control register
			1	HVIO6 low-side driver is off, regardless of the setting in the HVIO6 control register
4	IO5LOC	R/W		HVIO5 low-side driver control:
			0 ^[1]	HVIO5 low-side driver is controlled by the setting in the HVIO5 control register
			1	HVIO5 low-side driver is off, regardless of the setting in the HVIO5 control register
3	IO4LOC	R/W		HVIO4 low-side driver control:
			0 ^[1]	HVIO4 low-side driver is controlled by the setting in the HVIO4 control register
			1	HVIO4 low-side driver is off, regardless of the setting in the HVIO4 control register

Table 61. HVIO low-side driver control register (address 72h)...*continued**This table is located in non-volatile memory with restricted write access.*

Bit	Symbol	Access	Value	Description
2	IO3LOC	R/W		HVIO3 low-side driver control:
			0 ^[1]	HVIO3 low-side driver is controlled by the setting in the HVIO3 control register
			1	HVIO3 low-side driver is off, regardless of the setting in the HVIO3 control register
1	IO2LOC	R/W		HVIO2 low-side driver control:
			0 ^[1]	HVIO2 low-side driver is controlled by the setting in the HVIO2 control register
			1	HVIO2 low-side driver is off, regardless of the setting in the HVIO2 control register
0	IO1LOC	R/W		HVIO1 low-side driver control:
			0 ^[1]	HVIO1 low-side driver is controlled by the setting in the HVIO1 control register
			1	HVIO1 low-side driver is off, regardless of the setting in the HVIO1 control register

[1] Factory preset value.

The HVIO_n interrupt status bits are located in the HVIO_n interrupt status registers, [Table 62](#) to [Table 65](#). The interrupt mechanism is described in [Section 7.12](#).

Table 62. Bank 0 wake-up interrupt status register (address 64h)*Not available in UJA113xAHW/xF0.*

Bit	Symbol	Access	Value	Description
7	IO4FEI	R/W	0	no HVIO4 falling edge interrupt pending
			1	HVIO4 falling edge interrupt pending
6	IO4REI	R/W	0	no HVIO4 rising edge interrupt pending
			1	HVIO4 rising edge interrupt pending
5	IO3FEI	R/W	0	no HVIO3 falling edge interrupt pending
			1	HVIO3 falling edge interrupt pending
4	IO3REI	R/W	0	no HVIO3 rising edge interrupt pending
			1	HVIO3 rising edge interrupt pending
3	IO2FEI	R/W	0	no HVIO2 falling edge interrupt pending
			1	HVIO2 falling edge interrupt pending
2	IO2REI	R/W	0	no HVIO2 rising edge interrupt pending
			1	HVIO2 rising edge interrupt pending
1	IO1FEI	R/W	0	no HVIO1 falling edge interrupt pending
			1	HVIO1 falling edge interrupt pending
0	IO1REI	R/W	0	no HVIO1 rising edge interrupt pending
			1	HVIO1 rising edge interrupt pending

Table 63. Bank 0 fail interrupt status register (address 65h)*Not available in UJA113xAHW/xF0.*

Bit	Symbol	Access	Value	Description
7	IO4SCI	R/W	0	no HVIO4 short circuit interrupt pending
			1	HVIO4 short circuit interrupt pending
6	IO4OLI	R/W	0	no HVIO4 open load interrupt pending
			1	HVIO4 open load interrupt pending
5	IO3SCI	R/W	0	no HVIO3 short circuit interrupt pending
			1	HVIO3 short circuit interrupt pending
4	IO3OLI	R/W	0	no HVIO3 open load interrupt pending
			1	HVIO3 open load interrupt pending
3	IO2SCI	R/W	0	no HVIO2 short circuit interrupt pending
			1	HVIO2 short circuit interrupt pending
2	IO2OLI	R/W	0	no HVIO2 open load interrupt pending
			1	HVIO2 open load interrupt pending
1	IO1SCI	R/W	0	no HVIO1 short circuit interrupt pending
			1	HVIO1 short circuit interrupt pending
0	IO1OLI	R/W	0	no HVIO1 open load interrupt pending
			1	HVIO1 open load interrupt pending

Table 64. Bank 1 wake-up interrupt status register (address 66h)*Not available in UJA113xAHW/xFx.*

Bit	Symbol	Access	Value	Description
7	IO8FEI	R/W	0	no HVIO8 falling edge interrupt pending
			1	HVIO8 falling edge interrupt pending
6	IO8REI	R/W	0	no HVIO8 rising edge interrupt pending
			1	HVIO8 rising edge interrupt pending
5	IO7FEI	R/W	0	no HVIO7 falling edge interrupt pending
			1	HVIO7 falling edge interrupt pending
4	IO7REI	R/W	0	no HVIO7 rising edge interrupt pending
			1	HVIO7 rising edge interrupt pending
3	IO6FEI	R/W	0	no HVIO6 falling edge interrupt pending
			1	HVIO6 falling edge interrupt pending
2	IO6REI	R/W	0	no HVIO6 rising edge interrupt pending
			1	HVIO6 rising edge interrupt pending
1	IO5FEI	R/W	0	no HVIO5 falling edge interrupt pending
			1	HVIO5 falling edge interrupt pending
0	IO5REI	R/W	0	no HVIO5 rising edge interrupt pending

Table 64. Bank 1 wake-up interrupt status register (address 66h)...*continued**Not available in UJA113xAHW/xFx.*

Bit	Symbol	Access	Value	Description
			1	HVIO5 rising edge interrupt pending

Table 65. Bank 1 fail interrupt status register (address 67h)*Not available in UJA113xAHW/xFx.*

Bit	Symbol	Access	Value	Description
7	IO8SCI	R/W	0	no HVIO8 short circuit interrupt pending
			1	HVIO8 short circuit interrupt pending
6	IO8OLI	R/W	0	no HVIO8 open load interrupt pending
			1	HVIO8 open load interrupt pending
5	IO7SCI	R/W	0	no HVIO7 short circuit interrupt pending
			1	HVIO7 short circuit interrupt pending
4	IO7OLI	R/W	0	no HVIO7 open load interrupt pending
			1	HVIO7 open load interrupt pending
3	IO6SCI	R/W	0	no HVIO6 short circuit interrupt pending
			1	HVIO6 short circuit interrupt pending
2	IO6OLI	R/W	0	no HVIO6 open load interrupt pending
			1	HVIO6 open load interrupt pending
1	IO5SCI	R/W	0	no HVIO5 short circuit interrupt pending
			1	HVIO5 short circuit interrupt pending
0	IO5OLI	R/W	0	no HVIO5 open load interrupt pending
			1	HVIO5 open load interrupt pending

HVIO_n interrupts are enabled/disabled via the HVIO_n interrupt enable registers, [Table 66](#) to [Table 69](#).

Table 66. Bank 0 wake-up interrupt enable register (address 37h)*Not available in UJA113xAHW/xF0.*

Bit	Symbol	Access	Value	Description
7	IO4FEIE	R/W	0	HVIO4 falling edge interrupt disabled
			1	HVIO4 falling edge interrupt enabled
6	IO4REIE	R/W	0	HVIO4 rising edge interrupt disabled
			1	HVIO4 rising edge interrupt enabled
5	IO3FEIE	R/W	0	HVIO3 falling edge interrupt disabled
			1	HVIO3 falling edge interrupt enabled
4	IO3REIE	R/W	0	HVIO3 rising edge interrupt disabled
			1	HVIO3 rising edge interrupt enabled
3	IO2FEIE	R/W	0	HVIO2 falling edge interrupt disabled

Table 66. Bank 0 wake-up interrupt enable register (address 37h)...continued

Not available in UJA113xAHW/xF0.

Bit	Symbol	Access	Value	Description
			1	HVIO2 falling edge interrupt enabled
2	IO2REIE	R/W	0	HVIO2 rising edge interrupt disabled
			1	HVIO2 rising edge interrupt enabled
1	IO1FEIE	R/W	0	HVIO1 falling edge interrupt disabled
			1	HVIO1 falling edge interrupt enabled
0	IO1REIE	R/W	0	HVIO1 rising edge interrupt disabled
			1	HVIO1 rising edge interrupt enabled

Table 67. Bank 0 fail interrupt enable register (address 38h)

Not available in UJA113xAHW/xF0.

Bit	Symbol	Access	Value	Description
7	IO4SCIE	R/W	0	HVIO4 short circuit interrupt disabled
			1	HVIO4 short circuit interrupt enabled
6	IO4OLIE	R/W	0	HVIO4 open load interrupt disabled
			1	HVIO4 open load interrupt enabled
5	IO3SCIE	R/W	0	HVIO3 short circuit interrupt disabled
			1	HVIO3 short circuit interrupt enabled
4	IO3OLIE	R/W	0	HVIO3 open load interrupt disabled
			1	HVIO3 open load interrupt enabled
3	IO2SCIE	R/W	0	HVIO2 short circuit interrupt disabled
			1	HVIO2 short circuit interrupt enabled
2	IO2OLIE	R/W	0	HVIO2 open load interrupt disabled
			1	HVIO2 open load interrupt enabled
1	IO1SCIE	R/W	0	HVIO1 short circuit interrupt disabled
			1	HVIO1 short circuit interrupt enabled
0	IO1OLIE	R/W	0	HVIO1 open load interrupt disabled
			1	HVIO1 open load interrupt enabled

Table 68. Bank 1 wake-up interrupt enable register (address 47h)

Not available in UJA113xAHW/xFx.

Bit	Symbol	Access	Value	Description
7	IO8FEIE	R/W	0	HVIO8 falling edge interrupt disabled
			1	HVIO8 falling edge interrupt enabled
6	IO8REIE	R/W	0	HVIO8 rising edge interrupt disabled

Table 68. Bank 1 wake-up interrupt enable register (address 47h)...continued

Not available in UJA113xAHW/xFx.

Bit	Symbol	Access	Value	Description
			1	HVIO8 rising edge interrupt enabled
5	IO7FEIE	R/W	0	HVIO7 falling edge interrupt disabled
			1	HVIO7 falling edge interrupt enabled
4	IO7REIE	R/W	0	HVIO7 rising edge interrupt disabled
			1	HVIO7 rising edge interrupt enabled
3	IO6FEIE	R/W	0	HVIO6 falling edge interrupt disabled
			1	HVIO6 falling edge interrupt enabled
2	IO6REIE	R/W	0	HVIO6 rising edge interrupt disabled
			1	HVIO6 rising edge interrupt enabled
1	IO5FEIE	R/W	0	HVIO5 falling edge interrupt disabled
			1	HVIO5 falling edge interrupt enabled
0	IO5REIE	R/W	0	HVIO5 rising edge interrupt disabled
			1	HVIO5 rising edge interrupt enabled

Table 69. Bank 1 fail interrupt enable register (address 48h)

Not available in UJA113xAHW/xFx.

Bit	Symbol	Access	Value	Description
7	IO8SCIE	R/W	0	HVIO8 short circuit interrupt disabled
			1	HVIO8 short circuit interrupt enabled
6	IO8OLIE	R/W	0	HVIO8 open load interrupt disabled
			1	HVIO8 open load interrupt enabled
5	IO7SCIE	R/W	0	HVIO7 short circuit interrupt disabled
			1	HVIO7 short circuit interrupt enabled
4	IO7OLIE	R/W	0	HVIO7 open load interrupt disabled
			1	HVIO7 open load interrupt enabled
3	IO6SCIE	R/W	0	HVIO6 short circuit interrupt disabled
			1	HVIO6 short circuit interrupt enabled
2	IO6OLIE	R/W	0	HVIO6 open load interrupt disabled
			1	HVIO6 open load interrupt enabled
1	IO5SCIE	R/W	0	HVIO5 short circuit interrupt disabled
			1	HVIO5 short circuit interrupt enabled
0	IO5OLIE	R/W	0	HVIO5 open load interrupt disabled
			1	HVIO5 open load interrupt enabled

The influence of SBC operating modes on the HVIO pins is summarized in [Table 70](#). It also lists the values of associated register bits when these values are predictable according to the SBC operating mode.

Control/configuration bits (writable via SPI) and interrupt bits are (re-)initialized to the default values for the SBC mode. For status bits, the expected value for the SBC mode is indicated.

Table 70. Influence of SBC operating modes on HVIO pins and on related register bits

Symbol	Off (power-on default)	Forced Normal	Standby	Normal	Sleep	Reset	Overload	FSP
HVION ^[1]	off	off	HVION control register; low-side drivers disabled ^[2]	HVION control register ^[2]	HVION control register; low-side drivers disabled ^[2]	HVION control register; low-side drivers disabled ^[2]	fail-safe state ^[3]	HVION control register; low-side drivers disabled ^[2]
B0WTC	0	^[4]	-	-	-	-	-	-
B1WTC	0	^[4]	-	-	-	-	-	-
IONAC ^[5]	000	^[4]	-	-	-	-	-	-
IONCC ^[5]	000	^[4]	-	-	-	-	-	-
IONDS	11	^[4]	-	-	-	-	-	-
IONFEI	0	^[4]	-	-	-	-	-	0
IONFEIE	0	^[4]	-	-	-	-	-	1
IONHOC	located in one of the non-volatile configuration registers (see Section 7.13)							
IONLOC	located in one of the non-volatile configuration registers (see Section 7.13)							
IONOLI	0	^[4]	-	-	-	-	-	0
IONOLIE	0	^[4]	-	-	-	-	-	0
IONOLTC	00	^[4]	-	-	-	-	-	-
IONREI	0	^[4]	-	-	-	-	-	0
IONREIE	0	^[4]	-	-	-	-	-	1
IONSC ^[5]	00	^[4]	-	-	-	-	00	00
IONSCI	0	^[4]	-	-	-	-	-	0
IONSCIE	0	^[4]	-	-	-	-	-	0
IONSCTC	00	^[4]	-	-	-	-	-	-
IONSFC	located in one of the non-volatile configuration registers (see Section 7.13)							
IONWLS	0	^[4]	-	-	-	-	-	-

[1] HVIO availability depends on the device variant (see [Table 1](#)).

[2] Determined by the settings in the relevant HVIO control register (see [Section 7.10.7](#)).

[3] See [Section 7.10.4](#).

[4] Register not accessible; reading returns 0.

[5] When Limp-home functionality has been selected via bits IONSFC (n = 2,3,4), register contents is no longer relevant for HVION and/or for associated timers.

7.11 Timer control

The UJA113xA contains 4 timers. Each timer can be assigned to any of the HVIOs. Timer 2 can also be assigned to the EN pin. Up to four configuration options are available: two autonomous options and two synchronous options. If an autonomous option is selected (PWM mode or Timer mode), the timer period is determined by the dedicated timer period control bits TnPC. If a synchronous option is selected (Synchronous

timer mode or Synchronous follower mode), the timer period is inherited from a timer further up the chain, as described in [Table 71](#). Timer 1 acts as a leading timer and, therefore, has no synchronous option.

The timer mode is selected via control bits TnMC (see [Table 72](#) to [Table 78](#)). The options available are described in [Table 71](#). In an Autonomous mode, the duty cycle is determined by the setting of bits TnDCC (see [Table 73](#) to [Table 79](#)). In Timer mode, the activation of an assigned HVIO is delayed by one period to allow for synchronization with other timers.

Remark: When HVIO3 is configured as a limp home output (IO3SFC = 1), Timer 3 provides the clock signal (100 Hz 10 % PWM; see [Section 7.10.6](#)). Timer 3 is not available for any other purpose. Timer 3 control settings are ignored ([Table 76](#) and [Table 77](#)). Similarly, Timer 4 is dedicated to HVIO4 when it is configured as a limp home output and cannot be used for any other purpose (1.25 Hz 50 % PWM signal).

Table 71. Timer configuration options

Mode	Mode type	TnMC	Description
PWM	Autonomous	00	The duty cycle set via TnDCC is relative to the timer period. The period is determined by the dedicated timer period control bits (TnPC). This configuration option can be used for LED dimming.
Timer	Autonomous	01	The pulse width is a multiple of 100 μ s regardless of the selected period. If the on-time is longer than the selected period, the timer is always on. The period is determined by the dedicated timer period control bits (TnPC). This option is useful for generating short pulses with long periods, e.g. for switch biasing or safety heartbeat signals.
Synchronous timer	Synchronous	10	The pulse length is a multiple of 100 μ s. The pulse is triggered synchronously with the pulse of Timer 1. So the timer period is inherited from Timer 1, regardless of the setting of TnPC. If the pulse length is longer than the period of Timer 1, the timer is always on. This mode can be used for generating synchronized pulses of different lengths. Since Timer 1 is the leading timer, this option is only available for Timers 2 to 4. Note that the synchronous timer is triggered even when Timer 1 is operating at a duty cycle of 0 %.
Synchronous follower	Synchronous	11	The pulse length is a multiple of 100 μ s. The pulse of Timer n is triggered at the end of the pulse of Timer n - 1. The period is also inherited from Timer n - 1 (if Timer n - 1 is also running in a synchronous mode, the period is inherited from Timer n - 2, and so on). So the pulse of Timer 3 is triggered at the end of the Timer 2 pulse and the period is also inherited from Timer 2 (assuming Timer 2 is not running in a synchronous mode). This mode is useful for generating consecutive pulses. This option is only available for Timers 2 to 4. Note that the synchronous timer is triggered even when Timer 1 is operating at a duty cycle of 0 %.

7.11.1 Timer control and status registers

Table 72. Timer 1 control register (address 50h)

Bit	Symbol	Access	Value	Description
7:6	reserved	R/W	-	always write 00; ignore on read
5:2	T1PC	R/W		Timer 1 period:
			0000	4 ms
			0001	8 ms
			0010	20 ms
			0011	30 ms
			0100	50 ms
			0101	100 ms
			0110	200 ms
			0111	400 ms
			1000	800 ms
			1001	1 s
			1010	2 s
			1011	4 s
1	reserved	R/W	-	always write 0; ignore on read
0	T1MC	R/W		Timer 1 mode control:
			0	Timer 1 is in PWM mode; on-time = $T1DCC \times T1PC / 255$
			1	Timer 1 is in Timer mode; on-time = $T1DCC \times t_{w(base)tmr} \mu s$; period defined by T1PC

Table 73. Timer 1 duty cycle control register (address 51h)

Bit	Symbol	Access	Value	Description
7:0	T1DCC	R/W	xxxxxxx	duty cycle = $T1DCC / 255$

Table 74. Timer 2 control register (address 52h)

Bit	Symbol	Access	Value	Description
7:6	reserved	R/W	-	always write 00; ignore on read
5:2	T2PC	R/W		Timer 2 period:
			0000	4 ms
			0001	8 ms
			0010	20 ms
			0011	30 ms
			0100	50 ms
			0101	100 ms
			0110	200 ms
			0111	400 ms
			1000	800 ms
			1001	1 s
			1010	2 s
			1011	4 s
0:1	T2MC	R/W		Timer 2 mode control:
			00	Timer 2 is in PWM mode; on-time = $T2DCC \times T2PC / 255$
			01	Timer 2 is in Timer mode; on-time = $T2DCC \times t_{w(base)tmr} \mu s$; period defined by T2PC
			10	Timer 2 pulse is triggered at the start of Timer 1 pulse (Synchronous mode); on-time = $T2DCC \times t_{w(base)tmr} \mu s$
			11	Timer 2 pulse is triggered at the end of Timer 1 pulse (Synchronous follower mode); on-time = $T2DCC \times t_{w(base)tmr} \mu s$

Table 75. Timer 2 duty cycle control register (address 53h)

Bit	Symbol	Access	Value	Description
7:0	T2DCC	R/W	xxxxxxx	duty cycle = $T2DCC / 255$

Table 76. Timer 3 control register (address 54h)

Bit	Symbol	Access	Value	Description
7:6	reserved	R/W	-	always write 00; ignore on read
5:2	T3PC	R/W		Timer 3 period:
			0000	4 ms
			0001	8 ms
			0010	20 ms
			0011	30 ms
			0100	50 ms
			0101	100 ms
			0110	200 ms
			0111	400 ms
			1000	800 ms
			1001	1 s
			1010	2 s
			1011	4 s
0:1	T3MC	R/W		Timer 3 mode control:
			00	Timer 3 is in PWM mode; on-time = $T3DCC \times T3PC / 255$
			01	Timer 3 is in Timer mode; on-time = $T3DCC \times t_{w(base)tmr} \mu s$; period defined by T3PC
			10	Timer 3 pulse is triggered at the start of Timer 1 pulse (Synchronous mode); on-time = $T3DCC \times t_{w(base)tmr} \mu s$
			11	Timer 3 pulse is triggered at the end of Timer 2 pulse (Synchronous follower mode); on-time = $T3DCC \times t_{w(base)tmr} \mu s$

Table 77. Timer 3 duty cycle control register (address 55h)

Bit	Symbol	Access	Value	Description
7:0	T3DCC	R/W	xxxxxxx	duty cycle = $T3DCC / 255$

Table 78. Timer 4 control register (address 56h)

Bit	Symbol	Access	Value	Description
7:6	reserved	R/W	-	always write 00; ignore on read
5:2	T4PC	R/W		Timer 4 period:
			0000	4 ms
			0001	8 ms
			0010	20 ms
			0011	30 ms
			0100	50 ms
			0101	100 ms
			0110	200 ms
			0111	400 ms
			1000	800 ms
			1001	1 s
			1010	2 s
			1011	4 s
0:1	T4MC	R/W		Timer 4 mode control:
			00	Timer 4 is in PWM mode; on-time = $T4DCC \times T4PC / 255$
			01	Timer 4 is in Timer mode; on-time = $T4DCC \times t_{w(base)tmr} \mu s$; period defined by T4PC
			10	Timer 4 pulse is triggered at the start of Timer 1 pulse (Synchronous mode); on-time = $T4DCC \times t_{w(base)tmr} \mu s$
			11	Timer 4 pulse is triggered at the end of Timer 3 pulse (Synchronous follower mode); on-time = $T4DCC \times t_{w(base)tmr} \mu s$

Table 79. Timer 4 duty cycle control register (address 57h)

Bit	Symbol	Access	Value	Description
7:0	T4DCC	R/W	xxxxxxx	duty cycle = $T4DCC / 255$

[Table 80](#) lists the values of timer-related register bits when they are (re-)initialized at power-on.

Table 80. Influence of SBC operating modes on register bits related to timers

Symbol	Off (power-on default)	Forced Normal	Standby	Normal	Sleep	Reset	Overload	FSP
T1DCC	00000000	[1]	-	-	-	-	-	-
T1MC	0	[1]	-	-	-	-	-	-
T1PC	0000	[1]	-	-	-	-	-	-
T2DCC	00000000	[1]	-	-	-	-	-	-
T2MC	00	[1]	-	-	-	-	-	-
T2PC	0000	[1]	-	-	-	-	-	-
T3DCC ^[2]	00000000	[1]	-	-	-	-	-	-

Table 80. Influence of SBC operating modes on register bits related to timers...continued

Symbol	Off (power-on default)	Forced Normal	Standby	Normal	Sleep	Reset	Overload	FSP
T3MC ^[2]	00	[1]	-	-	-	-	-	-
T3PC ^[2]	0000	[1]	-	-	-	-	-	-
T4DCC ^[2]	00000000	[1]	-	-	-	-	-	-
T4MC ^[2]	00	[1]	-	-	-	-	-	-
T4PC ^[2]	0000	[1]	-	-	-	-	-	-

[1] Register not accessible; reading returns 0.

[2] When HVIO3 or HVIO4 is configured as a 'limp home' output via MTPNV bits IOnSFC, the associated timer bit settings are ignored.

7.12 Interrupt mechanism and wake-up function

The SBC interrupt mechanism alerts the microcontroller to specific events or changes of state via the interrupt pins, INTN1 and INTN2. Most interrupts can be enabled/disabled via dedicated interrupt enable bits. If an event occurs while the associated interrupt is enabled, pin INTN1 and, depending on the interrupt source, pin INTN2 are forced LOW. If the device is in Sleep mode when the interrupt is generated, the SBC wakes up and enters Reset Mode. The SBC does not distinguish between wake-up and interrupt events. All wake-up events (LIN, CAN and HVIO) generate interrupt requests and all interrupts trigger a wake-up event when the UJA113xA is in a low-power mode. When the SBC wakes up in response to an interrupt or wake-up event, the interrupt pin(s) will be LOW to signal to the microcontroller that an interrupt needs to be processed.

Pins INTN1 and INTN2 are digital open-drain active-LOW outputs that should be connected to the microcontroller. External pull-up resistors to V1 are needed to pull the interrupt pins HIGH when no interrupt is pending. Pin INTN1 is always driven LOW when an interrupt is pending. Pin INTN2 is assigned to a critical subset of interrupts that require immediate action, such as undervoltage or overtemperature warnings. So INTN2 can be used to assign priorities to interrupts via software.

An interrupt status bit is associated with each interrupt source to indicate whether an interrupt is pending. The interrupt status bits are contained in a number of dedicated interrupt status registers (located in the relevant sections of the data sheet). When an interrupt is generated, the microcontroller needs to poll these registers to determine the source of the interrupt. An additional Global interrupt status register ([Table 82](#)) is provided to help speed up this process. The microcontroller can access this register to determine the type of interrupt generated (system, supply, transceiver, bank 0 or bank 1) and then go directly to the relevant status register, minimizing access times.

Once the interrupt source has been identified, the relevant status bit should be cleared (set to 0) by writing 1 to the relevant bit - writing 0 will have no effect. A number of status bits can be cleared in a single write operation by writing 1 to all relevant bits. The interrupt pins are released (go HIGH) when all interrupt status bits have been cleared.

7.12.1 Interrupt delay

If interrupts occur very frequently, they can have a significant impact on the software processing time (because pins INTN1/INTN2 are repeatedly driven LOW, requiring a response from the microcontroller each time). The UJA113xA incorporates an interrupt delay timer to limit the disturbance to the software.

A timer is started and pin INTN1 is released when one or more interrupt status bits are cleared. A number of interrupts may be generated and captured while the timer is running and pin INTN1 remains HIGH. When the timer expires after $t_{to(int)}$, pin INTN1 goes LOW if one or more interrupts are pending. Note that the interrupt status registers can be read and cleared at any time, including while the timer is running and INTN1 is HIGH.

The interrupt delay timer is stopped immediately if pin RSTN goes LOW (as happens when the SBC enters Reset, Sleep, Overload and Off modes). The timer has no effect on pin INTN2. This pin goes LOW as soon as an associated interrupt is generated to allow the microcontroller to react as quickly as possible.

7.12.2 Sleep mode protection

The interrupt (wake-up) function is critical when the UJA113xA is in Sleep mode because the SBC will only leave Sleep mode in response to an interrupt request. To avoid deadlocks, the SBC distinguishes between regular and diagnostic interrupts (see [Section 7.12.3](#)). Regular interrupts are generated by bus (CAN, LIN) and local (HVIO) wake-up events; diagnostic interrupts detect failure/error conditions or state changes. At least one regular interrupt must be enabled before the UJA113xA can switch to Sleep mode. Any attempt to enter Sleep mode while all the regular interrupts are disabled triggers a system reset.

Another condition that must be satisfied before the UJA113xA can switch to Sleep mode is that all interrupt status bits must be cleared (no interrupt pending). If an SPI command to go to Sleep mode (MC = 001) is issued while an interrupt is pending, the SBC immediately switches to Reset mode. This condition applies to all interrupts (regular and diagnostic).

7.12.3 Interrupt sources

[Table 81](#) provides an overview of the interrupts recognized by the UJA113xA. The events that trigger each interrupt are described. In addition, the interrupt type ('regular' or 'diagnostic') is specified along with the associated interrupt pin(s) (INTN1 or both INTN1 and INTN2).

Most interrupts can be enabled and disabled via the interrupt enable registers (see relevant sections of the data sheet). The following interrupts do not have associated interrupt enable bits and are always enabled: WDI, PNFDEI, POSI, OVSDI.

Note that bus wake-up events (CAN, LIN1 and LIN2) also cause the dedicated RXD pins (RXDC, RXDL1 and RXDL2) to go LOW. Pin RXDx is released when the relevant interrupt status bit (CWI, LWI1 or LWI2) is cleared.

Table 81. Interrupt sources

Symbol	Description	Type	Pin	Source
CFI	CAN failure interrupt	diagnostic	INTN1	Status bit VCS and/or status bit CFS is set to 1.
CWI	CAN wake-up interrupt	regular	INTN1	A CAN wake-up event was detected while the transceiver was not in Active mode.
CBSI	CAN-bus silence interrupt	diagnostic	INTN1	Status bit CBSS has changed from 0 to 1.
LWIn	LINn wake-up interrupt	regular	INTN1	A wake-up event was detected at LINn while the transceiver was not in Active mode.
WDI	watchdog failure interrupt	diagnostic	INTN1	The watchdog overflowed in Timeout mode. If the watchdog overflows while a WDI is pending, a reset is performed. Note that this interrupt cannot be deactivated.
OTWI	overtemperature warning interrupt	diagnostic	INTN1, INTN2	The global chip temperature has exceeded the over-temperature warning threshold.
PNFDEI	partial networking frame detect error interrupt	diagnostic	INTN1	A CAN error frame was detected by the partial networking receiver.
POSI	power-on status interrupt	diagnostic	INTN1	The SBC has left Off Mode; interrupt is always enabled.
SPIFI	SPI failure interrupt	diagnostic	INTN1	This interrupt is triggered by the following events: <ul style="list-style-type: none"> illegal WMC code illegal NWP code illegal MC code

Table 81. Interrupt sources...continued

Symbol	Description	Type	Pin	Source
				<ul style="list-style-type: none"> wrong SPI clock count (only 16-, 24- and 32-bit commands are supported) write access to a locked register
V1UI	V1 undervoltage interrupt	diagnostic	INTN1, INTN2	V1 voltage dropped below the 90 % undervoltage threshold while V1 was active (no interrupt triggered in Sleep mode because V1 is off). This interrupt is independent of the V1RTC bit setting.
VEXTUI	V2 undervoltage interrupt	diagnostic	INTN1	V2/VEXT dropped below the 90 % undervoltage threshold.
VEXTOI	V2 overvoltage interrupt	diagnostic	INTN1	V2/VEXT above the 110 % overvoltage threshold.
BMUI	battery monitor undervoltage interrupt	diagnostic	INTN1, INTN2	The voltage measured at the active battery monitoring source (pin BAT or pin BATSENSE) dropped below the selected undervoltage threshold.
BMOI	battery monitor overvoltage interrupt	diagnostic	INTN1, INTN2	The voltage measured at the active battery monitoring source (pin BAT or pin BATSENSE) has risen above the selected overvoltage threshold.
OVSDI	overvoltage shut-down interrupt	diagnostic	INTN1, INTN2	A battery overvoltage will cause the SBC to enter Overload Mode; interrupt is always enabled.
SMPSSI	SMPS status interrupt	diagnostic	INTN1, INTN2	The state of bit SMPSS has changed (see Section 7.7.4.1)
IONOLI	HVION open load interrupt	diagnostic	INTN1	An open load condition was detected at HVION while the high-side or low-side driver was active.
IONSCI	HVION short circuit interrupt	diagnostic	INTN1	A short-circuit condition was detected at HVION while the high-side or low-side driver was active.
IONREI	HVION rising edge interrupt	regular	INTN1	A rising edge wake-up signal was detected at pin HVION when configured as wake input.
IONFEI	HVION falling edge interrupt	regular	INTN1	A falling edge wake-up signal was detected at pin HVION when configured as wake input.

7.12.4 Global interrupt status register

Table 82. Global interrupt status register (address 60h)

Bit	Symbol	Access	Value	Description
7	reserved	R	-	ignore on read
6	B1FIS ^[1]	R	0	no pending interrupt in the bank 1 fail interrupt status register
			1	pending interrupt in the bank 1 fail interrupt status register
5	B1WIS ^[1]	R	0	no pending interrupt in bank 1 wake-up interrupt status register
			1	pending interrupt in the bank 1 wake-up interrupt status register
4	B0FIS ^[2]	R	0	no pending interrupt in the bank 0 fail interrupt status register
			1	pending interrupt in the bank 0 fail interrupt status register
3	B0WIS ^[2]	R	0	no pending interrupt in bank 0 wake-up interrupt status register
			1	pending interrupt in the bank 0 wake-up interrupt status register
2	TRXIS	R	0	no pending interrupt in the Transceiver interrupt status register

Table 82. Global interrupt status register (address 60h)...continued

Bit	Symbol	Access	Value	Description
			1	pending interrupt in the Transceiver interrupt status register
1	SUPIS	R	0	no pending interrupt in the Supply interrupt status register
			1	pending interrupt in the Supply interrupt status register
0	SYSIS	R	0	no pending interrupt in the System interrupt status register
			1	pending interrupt in the System interrupt status register

[1] Reserved in UJA113xAHW/xFx.

[2] Reserved in UJA113xAHW/xF0.

Table 83 lists the values of Global interrupt register bits when they are (re-)initialized at power-on.

Table 83. Influence of SBC operating modes on Global interrupt status register bits

Symbol	Off (power-on default)	Forced Normal	Standby	Normal	Sleep	Reset	Overload	FSP
B0FIS	0	[1]	-	-	-	-	-	0
B0WIS	0	[1]	-	-	-	-	-	0
B1FIS	0	[1]	-	-	-	-	-	0
B1WIS	0	[1]	-	-	-	-	-	0
SUPIS	0	[1]	-	-	-	-	-	0
SYSIS	1	[1]	-	-	-	-	-	0
TRXIS	0	[1]	-	-	-	-	-	0

[1] Register not accessible; reading returns 0.

7.13 Non-volatile SBC configuration

The UJA113xA contains Multiple Time Programmable Non-Volatile (MTPNV) memory cells that allow some of the default device settings to be reconfigured. The MTPNV memory address range is from 0x71 to 0x74. An overview of the MTPNV registers is given in [Table 84](#). Details on bit settings, including factory preset values, can be found in [Table 11](#), [Table 14](#), [Table 60](#) and [Table 61](#).

Table 84. Overview of MTPNV registers

Addr.	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x71	HVIO high-side control ^[1]	IO8HOC	IO7HOC	IO6HOC	IO5HOC	IO4HOC	IO3HOC	IO2HOC	IO1HOC
0x72	HVIO low-side control ^[1]	IO8LOC	IO7LOC	IO6LOC	IO5LOC	IO4LOC	IO3LOC	IO2LOC	IO1LOC
0x73	Start-up control	reserved		RLC		V2SUC	IO4SFC	IO3SFC	IO2SFC
0x74	SBC configuration ctrl.	reserved		V1RTSUC		FNMC	SDMC	VEXTAC	SLPC

[1] For derivatives without the relevant HVIO pin, the associated bit is set to 0; this needs to be taken into account when calculating the CRC value.

7.13.1 Programming the MTPNV cells

Bit NVMPS in the MTPNV status register ([Table 85](#)) must be set to 1 before the non-volatile memory cells can be reprogrammed. Bit NVMPS is pre-set to 1 when the device is shipped. It is reset to 0 after the cells have been programmed. The battery supply voltage must be within the range specified for MTPNV programming ($V_{\text{prog(MTPNV)}}$; see [Table 104](#)) while the cells are being programmed. See also [Section 7.1.3](#).

NVMPS can be set to 1 again by restoring the factory presets (see [Section 7.13.2](#)). When the factory presets are restored, a system reset is generated, automatically forcing the UJA113xA to switch to Forced Normal mode (since FNMC = 1). This ensures that the programming cycle cannot be interrupted by the watchdog.

Programming of the non-volatile memory registers is performed in two steps. First, the required values are written to addresses 0x71 to 0x74. In the second step, reprogramming is confirmed by writing the correct CRC value to the MTPNV CRC control register (see [Section 7.13.1.1](#)). The SBC starts reprogramming the MTPNV cells as soon as the CRC value has been validated. If the CRC value is not correct, reprogramming is aborted. On completion, a system reset is generated during which the device re-boots with the configuration as programmed in the MTPNV cells. Note that updated contents of registers 0x71 to 0x74 cannot be read until the programming process has been successfully completed.

After an MTPNV programming cycle has been completed, the non-volatile memory is protected against being overwritten via a standard SPI write operation.

The MTPNV status register ([Table 85](#)) contains a write counter, WRCNTS, that is incremented each time the MTPNV cells are reprogrammed (up to a maximum value of 111111; there is no overflow). Note that this counter is provided for information purposes only; reprogramming will not be aborted if it reaches its maximum value. An error correction code status bit, ECCS, indicates whether reprogramming was successful. It is not recommended to program the MTPNV cells more than $N_{\text{cy(W)MTP}}$ times (see [Table 104](#)).

Table 85. MTPNV status register (address 70h)

Bit	Symbol	Access	Value	Description
7:2	WRCNTS	R	xxxxxx	write counter: contains the number of times the MTPNV cells were reprogrammed
1	ECCS	R	0	no error detected during MTPNV cell programming
			1	an error was detected during MTPNV cell programming
0	NVMPS	R	0	MTPNV memory cannot be overwritten

Table 85. MTPNV status register (address 70h)...continued

Bit	Symbol	Access	Value	Description
			1	MTPNV memory is ready to be reprogrammed

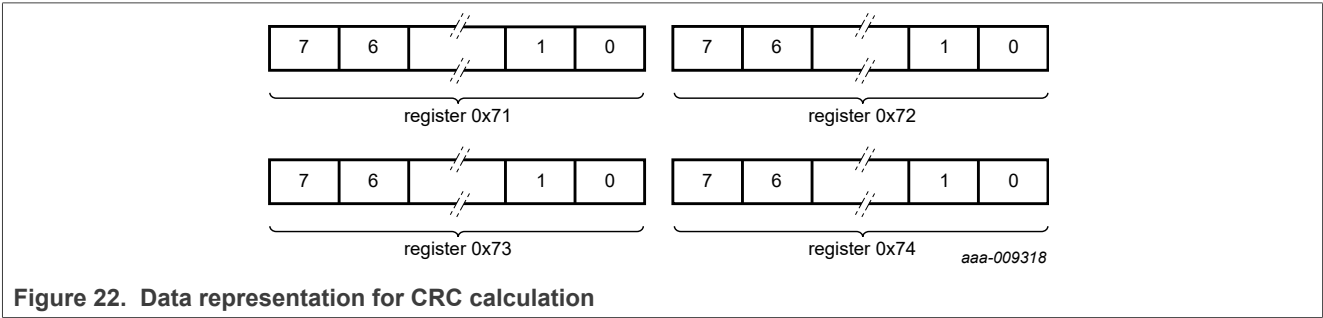
7.13.1.1 Calculating the CRC value for MTP programming

The cyclic redundancy check value stored in bits CRCC in the MTPNV CRC control register is calculated using the data written to registers 0x71 to 0x74. Not writing to one of these registers is equivalent to writing 00h to that register.

Table 86. MTPNV CRC control register (address 75h)

Bit	Symbol	Access	Value	Description
7:0	CRCC	R/W	-	CRC control data

The CRC value is calculated using the data representation shown in [Figure 22](#) and the modulo-2 division with the generator polynomial: $X^8 + X^5 + X^3 + X^2 + X + 1$. The result of this operation must be bitwise inverted.



The following parameters can be used to calculate the CRC value (e.g. via the Autosar method):

Table 87. Parameters for CRC coding

Parameter	Value
CRC result width	8 bits
Polynomial	0x2F
Initial value	0xFF
Input data reflected	no
Result data reflected	no
XOR value	0xFF

Alternatively, the following algorithm can be used:

```
/* Copyright 2015 NXP. NXP Confidential. This software is owned or controlled by
NXP and may only be
* used strictly in accordance with the applicable license terms found at
* https://www.nxp.com/LA_OPT_NXP_SW. The "production use license" in Section
2.3 in the NXP SOFTWARE
* LICENSE AGREEMENT is expressly granted for this software.
*/
data = 0 // unsigned byte
crc = 0xFF
for i = 0 to 3
```

```
data = content_of_address(0x71 + i) EXOR crc
for j = 0 to 7
  if data ≥ 128
    data = data * 2 // shift left by 1
    data = data EXOR 0x2F
  else
    data = data * 2 // shift left by 1
  next j
  crc = data
next i
crc = crc EXOR 0xFF
```

7.13.2 Restoring factory preset values

Factory preset values are restored when the following conditions apply for at least $t_{d(MTPNV)}$ during power-up (see [Section 7.1.3](#)):

- pin RSTN is held LOW
- CANH is pulled up to V_{BAT}
- CANL is pulled down to GND

After the factory preset values have been restored, the SBC enters Forced normal Mode. Since the CAN-bus is clamped dominant, pin RXDC will be LOW. During the factory preset restore process, this pin is forced HIGH to allow a falling edge to signal that the process has been completed. The battery supply voltage must be within the range specified for MTPNV programming ($V_{prog(MTPNV)}$; see [Table 104](#)) while the restore process is ongoing.

The write counter, WRCNTS, in the MTPNV status register is incremented every time the factory presets are restored.

7.14 Device ID

Two bytes are reserved at addresses 0x7E and 0x7F for the UJA113xA identification codes. ID0S and ID1S combine to indicate the UJA113xA series variant, as detailed in [Table 90](#).

Table 88. Identification register 1 (address 7Eh)

Bit	Symbol	Access	Value	Description
7:0	ID0S	R	see Table 90	device identification code (part 1)

Table 89. Identification register 2 (address 7Fh)

Bit	Symbol	Access	Value	Description
7:6	ID1S	R	see Table 90	device identification code (part 2)
5:0	IDVS	R		silicon version:
			xx0xxx	UJA113xAHW
			xx1xxx	UJA113xAHW/xFx

Table 90. Identification codes

Variant	ID0S (8 LBSs of ID code)	ID1S (2 MSBs of ID code)
UJA1131AHW/5	0x11	0x0

Table 90. Identification codes...continued

Variant	ID0S (8 LBSs of ID code)	ID1S (2 MSBs of ID code)
UJA1131AHW/3	0x10	0x0
UJA1132AHW/5	0x01	0x0
UJA1132AHW/3	0x00	0x0
UJA1135AHW/5	0x11	0x1
UJA1135AHW/3	0x10	0x1
UJA1136AHW/5	0x01	0x1
UJA1136AHW/3	0x00	0x1
UJA1131AHW/5F4	0x51	0x0
UJA1131AHW/3F4	0x50	0x0
UJA1131AHW/5F0	0x71	0x0
UJA1131AHW/3F0	0x70	0x0
UJA1132AHW/5F4	0x41	0x0
UJA1132AHW/3F4	0x40	0x0
UJA1132AHW/5F0	0x61	0x0
UJA1132AHW/3F0	0x60	0x0

7.15 General-purpose memory

The UJA113xA allocates 4 bytes of RAM as general-purpose memory for storing user information. The general-purpose registers can be accessed via the SPI at addresses 0x06 to 0x09 (see [Table 95](#)).

Table 91. Influence of SBC operating modes on the general-purpose memory bits

Symbol	Off (power-on default)	Forced Normal	Standby	Normal	Sleep	Reset	Overload	FSP
GPM	00..00	[1]	-	-	-	-	-	-

[1] Register not accessible; reading returns 0.

7.16 SPI

7.16.1 Introduction

The Serial Peripheral Interface (SPI) provides the communication link with the microcontroller, supporting multiple-device operations. The SPI is configured for full-duplex data transfer, so status information is returned when new control data is shifted in. The interface also offers a read-only access option, allowing the application to read back the data without changing the register content.

The SPI uses four interface signals for synchronization and data transfer:

- SCSN: SPI chip select; active LOW
- SCK: SPI clock; default level is LOW due to low-power concept
- SDI: SPI data input
- SDO: SPI data output; floating when pin SCSN is HIGH

Bit sampling is performed on the falling clock edge and data is shifted on the rising clock edge (see [Figure 23](#)).

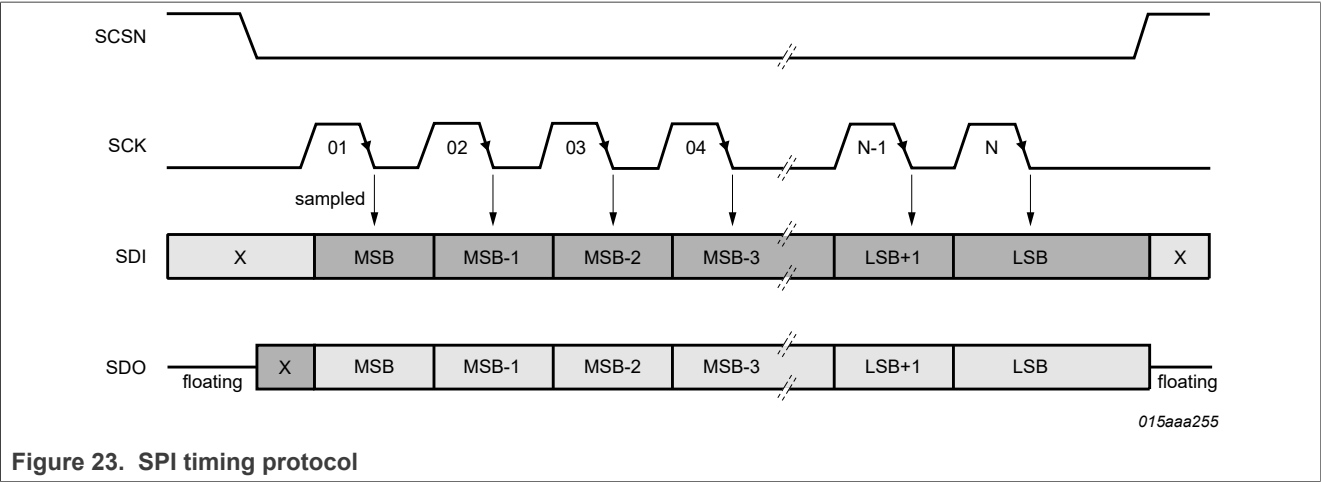
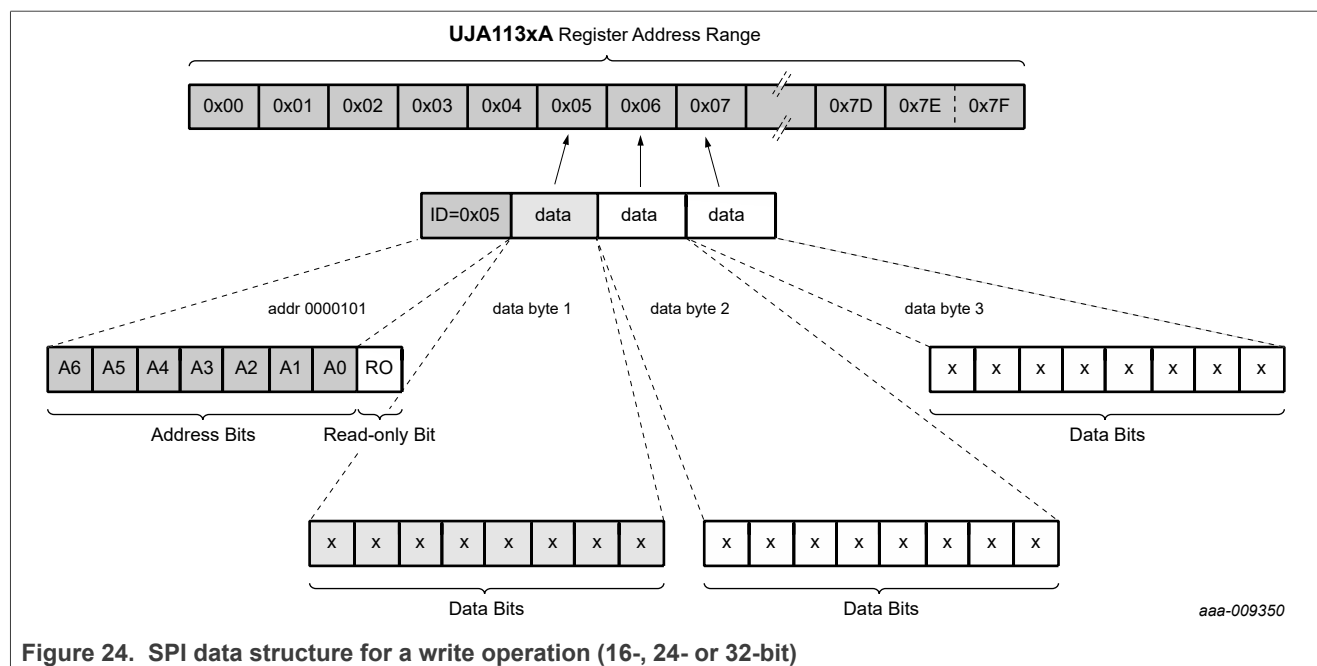


Figure 23. SPI timing protocol

The SPI data in the UJA113xA is stored in a number of dedicated 8-bit registers. Each register is assigned a unique 7-bit address. Two bytes need to be transmitted to the SBC for a single register write operation. The first byte contains the 7-bit address along with a 'read-only' bit (the LSB). The read-only bit must be 0 to indicate a write operation (if this bit is 1, a read operation is assumed and any data on the SDI pin is ignored). The second byte contains the data to be written to the register.

24- and 32-bit operations are also supported. The register address is automatically incremented, once for a 24-bit operation and twice for a 32-bit operation, as illustrated in [Figure 24](#).



During an SPI data write operation, the contents of the addressed register(s) is returned via pin SDO. This also happens for a read operation (where the read-only bit is set to 1).

During a write operation, the UJA113xA monitors the number of SPI bits transmitted. If the number recorded is not 16, 24 or 32, the write operation is aborted and an SPI failure interrupt is generated (SPIFI = 1), if enabled (SPIFIE = 1).

The SBC is ready to process an SPI operation $t_{to(SPI)}$ after leaving Reset mode. Any attempt to read or write before this timeout time has elapsed will generate an SPI failure interrupt

A delay of at least $t_{d(W)SPI}$ must be inserted between consecutive SPI write operations to the same register, otherwise the SBC may not execute the first write access. The delay is measured between successive rising edges on SCSN.

The UJA113xA tolerates attempts to write to registers that do not exist. If the available address space is exceeded during a write operation, the data overflows into address 0x00 (without generating an SPI failure interrupt).

An SPI failure interrupt is generated if an illegal SPI message is received (e.g. the number of bits transmitted is not 16, 24 or 32). The received information is ignored and register contents are not modified. If an SPI write operation does not trigger an interrupt, the data has been successfully written to the addressed register.

7.16.2 Register locking

Certain sections of the register address map (see [Table 92](#)) can be write-protected ('locked') to prevent unintended modifications. Any attempt to overwrite a locked register results in the entire SPI command being ignored (even if part of the SPI command accesses unlocked registers). An SPI failure interrupt is generated (SPIFI = 1), if enabled. Note that this feature only protects locked bits from being modified via the SPI and will not prevent the UJA113xA updating status registers etc.

7.16.3 SPI control and status registers

Table 92. Lock control register (address 0Ah)

Bit	Symbol	Access	Value	Description
7	reserved	R/W	-	always write 0, ignore on read
6	LK6C	R/W		lock control 6: address area 0x68 to 0x6F - data mask (/xFx versions only)
			0	SPI write-access enabled
			1	SPI write-access disabled
5	LK5C	R/W		lock control 5: address area 0x50 to 0x5F - Timer control
			0	SPI write access enabled
			1	SPI write access disabled
4	LK4C	R/W		lock control 4: address area 0x40 to 0x4F - HVIO5 to HVIO8 control (if HVIO bank 1 available; see Section 7.10)
			0	SPI write access enabled
			1	SPI write access disabled
3	LK3C	R/W		lock control 3: address area 0x30 to 0x3F - HVIO1 to HVIO4 control (if HVIO bank 0 available; see Section 7.10)
			0	SPI write access enabled
			1	SPI write access disabled
2	LK2C	R/W		lock control 2: address area 0x20 to 0x2F - transceiver control
			0	SPI write access enabled
			1	SPI write access disabled
1	LK1C	R/W		lock control 1: address area 0x10 to 0x1F - supply control
			0	SPI write access enabled
			1	SPI write access disabled
0	LK0C	R/W		lock control 0: address area 0x06 to 0x09 - general-purpose memory
			0	SPI write access enabled
			1	SPI write access disabled

See also SPI-related bits in [Table 6](#) and [Table 7](#) in [Section 7.1.2](#).

The influence of SBC operating modes on the SPI is summarized in [Table 93](#). It also lists the values of related register bits when they are (re-)initialized to the default values.

Table 93. Influence of SBC operating modes on SPI and related register bits

Block/bit	Operating mode							FSP
	Off	Forced Normal	Standby	Normal	Sleep	Reset	Overload	
SPI	disabled	limited access	active	active	disabled	disabled	disabled	disabled
SPIFI ^[1]	0	^[2]	-	-	-	-	-	0
SPIFIE ^[3]	0	^[2]	-	-	-	-	-	0
LKnC	0	^[2]	-	-	-	-	-	-

[1] see [Table 6](#).
[2] Register not accessible; reading returns 0.
[3] See [Table 7](#).

7.16.4 Register map

The addressable register space contains 128 registers with addresses from 0x00 to 0x7F. The registers are divided into eight functional groups, as shown in [Table 94](#). An overview of the register mapping is provided in [Table 95](#) to [Table 101](#). The functionality of individual bits is discussed in more detail in the relevant sections of the data sheet. Note that not all registers and bits are available in all UJA113xA derivatives.

Table 94. Register groupings

Address range	Description	Content
0x00 to 0x0F	Primary control registers	SBC mode, watchdog, reset, limp-home, Overtemp, EN control
0x10 to 0x1F	Supply control registers	Battery monitoring, V1, V2, SMPS control
0x20 to 0x2F	Transceiver control registers	CAN, LIN1 and LIN2 control
0x30 to 0x3F	HVIO bank 0 control registers	Control of HVIO1 to HVIO4
0x40 to 0x4F	HVIO bank 1 control registers	Control of HVIO5 to HVIO8
0x50 to 0x5F	Timer control registers	Timer 1 to 4 control
0x60 to 0x6F	Interrupt status registers	Interrupt status (and CAN data masks for UJA113x AHW/xFx)
0x70 to 0x7F	MTPNV and ID registers	MTPNV register access

Table 95. Overview of primary control registers

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x00	Watchdog control	WMC			reserved	NWP			
0x01	Mode control	reserved					MC		
0x02	Fail-safe control	ENSC		ENDC	ENC		LHC	RCC	
0x03	Main status	reserved	OTWS	NMS	RSS				
0x04	System interrupt enable	reserved					OTWIE	SPIFIE	reserved
0x05	Watchdog status	reserved				FNMS	SDMS	WDS	
0x06	Memory 0	GPM[7:0]							
0x07	Memory 1	GPM[15:8]							
0x08	Memory 2	GPM[23:16]							
0x09	Memory 3	GPM[31:24]							
0x0A	Lock control	reserved	LK6C	LK5C	LK4C	LK3C	LK2C	LK1C	LK0C
0x0B to 0x0F		reserved							

Table 96. Overview of supply control registers

Addr.	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x10	Regulator control	reserved		V2SC		V2C		V1RTC	
0x11	Battery monitor interrupt ctrl.	reserved							BMSC
0x12	Battery monitor UV control	BMUTC							
0x13	Battery monitor OV control	BMOTC							
0x14	Battery monitor hys. ctrl.	BMHOC				BMHUC			
0x15	V _{BAT} ADC results 1	BMBCD							
0x16	V _{BAT} ADC results 2	reserved					BMBCS	BMBCD	
0x17	BATSENSE ADC results 1	BMSCD							
0x18	BATSENSE ADC results 2	reserved					BMSCS	BMSCD	
0x19	SMPS control	reserved				SMPSOTC	reserved	SMPSC	
0x1A	SMPS o/p voltage control	reserved				SMPSOC			
0x1B	Supply voltage status	reserved		BMOVS	BMUVS	SMPSS	VEXTS		V1S
0x1C	Supply interrupt enable	reserved		SMPSSIE	BMOIE	BMUIE	VEXTOIE	VEXTUIE	V1UIE
0x1D to 0x1F		reserved							

Table 97. Overview of transceiver control registers

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x20	CAN control	reserved	CFDC	PNCOK	CPNC	CSC		CMC	
0x21	LIN control	LSC2		LMC2		LSC1		LMC1	
0x22	Transceiver status	CTS	CPNERR	CPNS	COSCS	CBSS	VLINS	VCS	CFS
0x23	Transceiver interrupt enable	reserved			CBSIE	LWI2E	LWI1E	CFIE	CWIE
0x24 to 0x25		reserved							
0x26	Data rate	reserved					CDR		
0x27	ID 0	ID7:ID0							
0x28	ID 1	ID15:ID8							
0x29	ID 2	ID23:ID16							
0x2A	ID 3	reserved			ID28:ID24				
0x2B	Mask 0	IDM7:IDM0							
0x2C	Mask 1	IDM15:IDM8							
0x2D	Mask 2	IDM23:IDM16							
0x2E	Mask 3	reserved			IDM28:IDM24				
0x2F	Frame control	IDE	PNDM	reserved		DLC			

Table 98. Overview of HVIO control registers

Addr.	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x30	HVIO1 control	IO1SC		IO1AC			IO1CC		
0x31	HVIO2 control	IO2SC		IO2AC			IO2CC		
0x32	HVIO3 control	IO3SC		IO3AC			IO3CC		
0x33	HVIO4 control	IO4SC		IO4AC			IO4CC		
0x34	Bank 0 threshold control	reserved							B0WTC
0x35	Bank 0 wake-up status	reserved				IO4WLS	IO3WLS	IO2WLS	IO1WLS
0x36	Bank 0 driver status	IO4DS		IO3DS		IO2DS		IO1DS	
0x37	Bank 0 wake int. enable	IO4FEIE	IO4REIE	IO3FEIE	IO3REIE	IO2FEIE	IO2REIE	IO1FEIE	IO1REIE
0x38	Bank 0 fail int. enable	IO4SCIE	IO4OLIE	IO3SCIE	IO3OLIE	IO2SCIE	IO2OLIE	IO1SCIE	IO1OLIE
0x39	Bank 0 s/c threshold ctrl.	IO4SCTC		IO3SCTC		IO2SCTC		IO1SCTC	
0x3A	Bank 0 o/l threshold ctrl.	IO4OLTC		IO3OLTC		IO2OLTC		IO1OLTC	
0x3B to 0x3F		reserved							
0x40	HVIO5 control	IO5SC		IO5AC			IO5CC		
0x41	HVIO6 control	IO6SC		IO6AC			IO6CC		
0x42	HVIO7 control	IO7SC		IO7AC			IO7CC		
0x43	HVIO8 control	IO8SC		IO8AC			IO8CC		
0x44	Bank 1 threshold control	reserved							B1WTC
0x45	Bank 1 wake-up status	reserved				IO8WLS	IO7WLS	IO6WLS	IO5WLS
0x46	Bank 1 driver status	IO8DS		IO7DS		IO6DS		IO5DS	
0x47	Bank 1 wake int. enable	IO8FEIE	IO8REIE	IO7FEIE	IO7REIE	IO6FEIE	IO6REIE	IO5FEIE	IO5REIE
0x48	Bank 1 fail int. enable	IO8SCIE	IO8OLIE	IO7SCIE	IO7OLIE	IO6SCIE	IO6OLIE	IO5SCIE	IO5OLIE
0x49	Bank 0 s/c threshold ctrl.	IO8SCTC		IO7SCTC		IO6SCTC		IO5SCTC	
0x4A	Bank 0 o/l threshold ctrl.	IO8OLTC		IO7OLTC		IO6OLTC		IO5OLTC	
0x4B to 0x4F		reserved							

Table 99. Overview of timer control registers

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x50	Timer 1 control	reserved		T1PC				res.	T1MC
0x51	Timer 1 duty cycle control	T1DCC							
0x52	Timer 2 control	reserved		T2PC				T2MC	
0x53	Timer 2 duty cycle control	T2DCC							
0x54	Timer 3 control	reserved		T3PC				T3MC	
0x55	Timer 3 duty cycle control	T3DCC							
0x56	Timer 4 control	reserved		T4PC				T4MC	

Table 99. Overview of timer control registers...continued

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x57	Timer4 duty cycle control	T4DCC							
0x58 to 0x5F		reserved							

Table 100. Overview of interrupt status registers

Addr.	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x60	Global interrupt status	reserved	B1FIS	B1WIS	B0FIS	B0WIS	TRXIS	SUPIS	SYSIS
0x61	System interrupt status	reserved		OVSDI	POSI	reserved	OTWI	SPIFI	WDI
0x62	Supply interrupt status	reserved		SMPSSI	BMOI	BMUI	VEXTOI	VEXTUI	V1UI
0x63	Transceiver interrupt status	reserved		PNFDEI	CBSI	LWI2	LWI1	CFI	CWI
0x64	Bank 0 wake-up interrupt status	IO4FEI	IO4REI	IO3FEI	IO3REI	IO2FEI	IO2REI	IO1FEI	IO1REI
0x65	Bank 0 fail interrupt status	IO4SCI	IO4OLI	IO3SCI	IO3OLI	IO2SCI	IO2OLI	IO1SCI	IO1OLI
0x66	Bank 1 wake-up interrupt status	IO8FEI	IO8REI	IO7FEI	IO7REI	IO6FEI	IO6REI	IO5FEI	IO5REI
0x67	Bank 1 fail interrupt status	IO8SCI	IO8OLI	IO7SCI	IO7OLI	IO6SCI	IO6OLI	IO5SCI	IO5OLI
0x68	Data mask 0	DM0[7:0]							
0x69	Data mask 1	DM1[7:0]							
0x6A	Data mask 2	DM2[7:0]							
0x6B	Data mask 3	DM3[7:0]							
0x6C	Data mask 4	DM4[7:0]							
0x6D	Data mask 5	DM5[7:0]							
0x6E	Data mask 6	DM6[7:0]							
0x6F	Data mask 7	DM7[7:0]							

Table 101. Overview of MTPNV and ID registers

Addr.	Register Name	Bit:								
		7	6	5	4	3	2	1	0	
0x70	MTPNV status	WRCNTS							ECCS	NVMPs
0x71	HVIO high-side control	IO8HOC	IO7HOC	IO6HOC	IO5HOC	IO4HOC	IO3HOC	IO2HOC	IO1HOC	
0x72	HVIO low-side control	IO8LOC	IO7LOC	IO6LOC	IO5LOC	IO4LOC	IO3LOC	IO2LOC	IO1LOC	
0x73	Start-up control	reserved		RLC		V2SUC	IO4SFC	IO3SFC	IO2SFC	
0x74	SBC configuration ctrl.	reserved		V1RTSUC		FNMC	SDMC	VEXTAC	SLPC	
0x75	MTPNV CRC control	CRCC								
0x76 to 0x7D		reserved								
0x7E	Identification register 1	ID0S								

Table 101. Overview of MTPNV and ID registers...continued

Addr.	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x7F	Identification register 2	ID1S		IDVS					

8 Limiting values

Table 102. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134); all voltages are referenced to pin GND, unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Max	Unit
V _x	voltage on pin x ^[1]	pin V1 (max current I _{V1} = 50 mA) ^[2]	-0.3	+6	V
		pins V2 and VCAN	-0.3	+6	V
		pins TXDC, RXDC, EN, SDI, SDO, SCK, SCSN, TXDL1, TXDL2, RXDL1, RXDL2, RSTN, INTN1 and INTN2 ^[3]	-0.3	V _{V1} + 0.3	V
		pin VEXT	-18	+40	V
		pins HVIO1 to HVIO8 ^[4]	-18	+40	V
		pins BAT, BATHS1, BATHS2, BATSMPS, BATV2, L1, LIMP, BATSENSE, ADCCAP	-0.3	+40	V
		pin BOOTH1	V _{L1} - 0.3	V _{L1} + 3.6	V
		pin BOOTH2	V _{L2} - 0.3	V _{L2} + 3.6	V
		pins L2, VSMPS	-0.3	+18	V
		pin CAPA	-0.3	+3.6	V
		pin CAPB (internally shorted to GNDSMPS)	-0.3	+0.3	V
		pins CANH and CANL with respect to any other pin	-58	+58	V
		pins LIN1 and LIN2 with respect to any other pin	-40	+40	V
		GNDSMPS	-0.3	+0.3	V
V _(CANH-CANL)	voltage between pin CANH and pin CANL		-40	+40	V
I _x	current on pin x	reverse polarity			
		pins BAT, BATHS1, BATHS2, BATSMPS, BATV2	-10	-	mA
I _{i(LIMP)}	input current on pin LIMP	LHC = 1	-	20	mA
I _{BATSENSE}	current on pin BATSENSE	continuous current; V _{BATSENSE} < 0 V	-18	-	mA
		peak current; V _{BATSENSE} < 0 V; t _{max} = 2 ms; ISO7637 pulse 1	-180	-	mA
I _r	reverse current	from pin V1 to pin VSMPS; V _{V1} ≤ 5 V ^[5]	-	500	mA
		from pin V2 to pin BATV2; V _{V2} ≤ 5 V ^[5]	-	100	mA
V _{trt}	transient voltage	on pins ^[6] BAT, BATHS1, BATHS2, BATSMPS, BATV2: via reverse polarity diode and capacitor to GND BATSENSE: coupling via 1 kΩ resistor and 10 nF capacitor to GND CANL, CANH: coupling via 1 nF capacitors LIN1, LIN2: coupling via 1 nF capacitors HVIO1 to HVIO8: coupling via 1 nF capacitors VEXT: coupling via 1 nF capacitor			

Table 102. Limiting values...continued

In accordance with the Absolute Maximum Rating System (IEC 60134); all voltages are referenced to pin GND, unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Max	Unit
		pulse 1	-100	-	V
		pulse 2a	-	+75	V
		pulse 3a	-150	-	V
		pulse 3b	-	+100	V
V _{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (150 pF, 330 Ω discharge circuit) [7]			
		pins BAT, BATHS1, BATHS2, BATSMPS, BATV2 with capacitor; CANH, CANL, LIN1 and LIN2, HVIO1 to HVIO8, BATSENSE with 10 nF capacitor and 1 kΩ resistor; VEXT with 2.2 μF capacitor [8]	-6	+6	kV
		Human Body Model (HBM); 100 pF, 1.5 kΩ			
		on any pin [9]	-2	+2	kV
		pins CANH, CANL, LIN1, LIN2 [10]	-6	+6	kV
		pins BAT, BATV2, BATHS1, BATHS2, HVIO1 to HVIO8, BATSENSE, VEXT [11]	-4	+4	kV
		Charged Device Model (CDM); field Induced charge; 4 pF [12]			
		corner pins	-750	+750	V
		all other pins	-500	+500	V
T _{vj}	virtual junction temperature	[13]	-40	+150	°C
		when programming the MTPNV cells	0	+85	°C
T _{stg}	storage temperature	[14]	-55	+150	°C
T _{amb}	ambient temperature	[15]	-40	+125	°C

- [1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.
- [2] V1 has an internal clamping mechanism that ensures that, in both supplied and unsupplied state, an injection current of 50 mA (max) flowing from the connected microcontroller can be tolerated without needing to specify the interface pins to a voltage higher than 6 V. This means that an external Zener diode is not needed to limit the output voltage on V1. The clamping voltage is less than 5 V while the LDO is off (including Sleep mode).
- [3] Maximum injection current of 10 mA per pin and 50 mA in total.
- [4] The difference between the supply voltage on pin BATHS1 and the voltage on any of pins HVIO1 to HVIO4 must not exceed 40 V; similarly the difference between the supply voltage on pin BATHS2 and the voltage on any of pins HVIO5 to HVIO8 must not exceed 40 V.
- [5] A reverse diode connected between V1 (anode) and VSMPS (cathode) limits the voltage drop voltage from V1(+) to VSMPS (-). A reverse diode connected between V2 (anode) and BATV2 (cathode) limits the voltage drop from V2(+) to BATV2 (-).
- [6] Verified by an external test house according to IEC TS 62228 2007, Section 4.2.4; parameters for standard pulses defined in ISO7637 part 2.
- [7] Verified by an external test house according to IEC TS 62228 2007, Section 4.3.
- [8] Only tested relative to ground. Only valid for the application circuit shown in [Figure 31](#).
- [9] According to AEC-Q100-002.
- [10] V1, V2, BAT, BATHS1, BATHS2, BATSMPS, VSMPS, BATV2 and VCAN connected to GND, emulating the application circuit ([Figure 31](#)). HBM pulse as specified in AECQ100-002 used.
- [11] Only tested relative to ground. Only valid for the application circuit shown in [Figure 31](#). HBM pulse as specified in AECQ100-002 used.
- [12] According to AEC-Q100-011.
- [13] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$, where $R_{th(vj-a)}$ is the thermal resistance from virtual junction to ambient of the device (see [Table 103](#)) and P is the customer-application-controlled power dissipation. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).
- [14] T_{stg} in application according to IEC61360-4. For component transport and storage conditions, see instead IEC61760-2.
- [15] Specification for virtual junction temperature T_{vj} is leading, i.e. maximum ambient temperature of 125 °C can only be sustained if self-heating through power dissipation is ≤ 25 °C.

9 Thermal characteristics

Table 103. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
R _{th(vj-a)}	thermal resistance from virtual junction to ambient	[1]	29	K/W
R _{th(vj-c)}	thermal resistance from virtual junction to case	[1]	10	K/W
Ψ _{j-top}	thermal characterization parameter from junction to top of package	[1]	3	K/W

[1] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 70 μm; top and bottom layers: 35 μm) and thermal via array under the exposed pad connected to the first inner copper layer.

10 Static characteristics

Table 104. Static characteristics

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$; $V_{BATSMPS} = V_{BAT} = 2\text{ V}$ to 28 V ; $V_{BATV2} = 5.5\text{ V}$ to 28 V ; $V_{BATHS1} = V_{BATHS2} = 4.5\text{ V}$ to 28 V ; $V_{VCAN} = 4.5\text{ V}$ to 5.5 V ; $R_{LIN1} = R_{LIN2} = 500\text{ }\Omega$; $R_{(CANH-CANL)} = 60\text{ }\Omega$; $L_{SMPS}^{[1]} = 22\text{ }\mu\text{H}$; $C_{SMPS}^{[1]} = 22\text{ }\mu\text{F}$; $V_{VSMPS} = 6\text{ V}$ ($SMPSOC = 0101$); C_{V1} and $C_{VEXT} > 1.76\text{ }\mu\text{F}$; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at $V_{BATSMPS} = V_{BAT} = V_{BATV2} = V_{BATHS1} = V_{BATHS2} = 13\text{ V}$ and $T_{vj} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply current; pins BAT, BATV2, BATHS1, BATHS2, BATSMPS						
Standby mode; CAN wake-up or no wake-up source enabled; $7.7\text{ V} < V_{BATSMPS} < 15\text{ V}$						
I _{DD}	supply current	SMPS in Pass- through mode (SMPSC = 11); I _{V1} = 0 μA; I _{L(o)SMPS} = 0 μA				
		T _{vj} = -40 °C	-	75	-	μA
		T _{vj} = +25 °C	-	80	-	μA
		T _{vj} = +40 °C	-	83	-	μA
		T _{vj} = +85 °C	-	97	-	μA
		-40 °C < T _{vj} < +40 °C	-	-	110	μA
		-40 °C < T _{vj} < 85 °C	-	-	134	μA
Sleep mode; CAN wake-up or no wake-up source enabled; $7.7\text{ V} < V_{BATSMPS} < 15\text{ V}$						
I _{DD}	supply current	SMPS off (SMPSC = 00)				
		T _{vj} = -40 °C	-	43	-	μA
		T _{vj} = +25 °C	-	50	-	μA
		T _{vj} = +40 °C	-	52	-	μA
		T _{vj} = +85 °C	-	64	-	μA
		-40 °C < T _{vj} < +40 °C	-	-	70	μA
		-40 °C < T _{vj} < 85 °C	-	-	90	μA
		SMPS in Pass- through mode (SMPSC = 11); I _{VSMPS} = 0 μA				
		-40 °C < T _{vj} < 85 °C	-	80	109	μA

Table 104. Static characteristics...continued

$T_{vj} = -40\text{ °C to }+150\text{ °C}$; $V_{BATSMPS} = V_{BAT} = 2\text{ V to }28\text{ V}$; $V_{BATV2} = 5.5\text{ V to }28\text{ V}$; $V_{BATHS1} = V_{BATHS2} = 4.5\text{ V to }28\text{ V}$; $V_{VCAN} = 4.5\text{ V to }5.5\text{ V}$; $R_{LIN1} = R_{LIN2} = 500\text{ }\Omega$; $R_{(CANH-CANL)} = 60\text{ }\Omega$; $L_{SMPS}^{[1]} = 22\text{ }\mu\text{H}$; $C_{SMPS}^{[1]} = 22\text{ }\mu\text{F}$; $V_{VSMPS} = 6\text{ V}$ (SMPSOC = 0101); C_{V1} and $C_{VEXT} > 1.76\text{ }\mu\text{F}$; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at $V_{BATSMPS} = V_{BAT} = V_{BATV2} = V_{BATHS1} = V_{BATHS2} = 13\text{ V}$ and $T_{vj} = 25\text{ °C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Additional currents						
I_{DD}	supply current	wake-up source currents				
		one LIN wake-up interrupt enabled: LWI1E = 1 or LWI2E = 1; $-40\text{ °C} < T_{vj} < 85\text{ °C}$	-	2	3	μA
		one HVIO bank input enabled; IOnCC = 011, 100 or 111 with n = 1 to 4 or n = 5 to 8; $-40\text{ °C} < T_{vj} < 85\text{ °C}$	-	2	3	μA
		V2 regulator on; VEXTAC = 1; $I_{V2} = 0\text{ }\mu\text{A}$				
		$T_{vj} = -40\text{ °C}$	-	4	-	μA
		$T_{vj} = +25\text{ °C}$	-	4	-	μA
		$T_{vj} = +40\text{ °C}$	-	4	-	μA
		$T_{vj} = +85\text{ °C}$	-	4	-	μA
		$-40\text{ °C} < T_{vj} < +85\text{ °C}$	-	-	25	μA
		V2 regulator on; VEXTAC = 0; $-40\text{ °C} < T_{vj} < 85\text{ °C}$; $I_{V2} = 0\text{ }\mu\text{A}$	-	80	107	μA
		for first HVIO high-side driver activated (IOnAC > 0) but not turned on; $I_{HVIO_n} = 0\text{ }\mu\text{A}$	-	550	700	μA
		for first HVIO high-side driver activated (IOnAC > 0) and turned on; $I_{HVIO_n} = 0\text{ }\mu\text{A}$	-	1000	1400	μA
		for first active HVIO low-side driver (IOnAC > 0); $I_{HVIO_n} = 0\text{ }\mu\text{A}$	-	1000	1400	μA
		SMPS active (SMPSOC = 00/01); $I_{V1} = 0\text{ }\mu\text{A}$; $I_{L(o)SMPS} = 0\text{ }\mu\text{A}$; $V_{BAT} = 13\text{ V}$; $V_{SMPS} = 6\text{ V}$	[2]	6	8	mA
		Normal mode; $-40\text{ °C} < T_{vj} < 85\text{ °C}$	[2]	1.2	1.7	mA
		CAN Offline Bias mode; $-40\text{ °C} < T_{vj} < 85\text{ °C}$	-	38	55	μA
		CAN Active mode	-	160	280	μA
		CAN Listen-only mode	-	60	125	μA

Table 104. Static characteristics...continued

$T_{vj} = -40\text{ °C to }+150\text{ °C}$; $V_{BATSMPS} = V_{BAT} = 2\text{ V to }28\text{ V}$; $V_{BATV2} = 5.5\text{ V to }28\text{ V}$; $V_{BATHS1} = V_{BATHS2} = 4.5\text{ V to }28\text{ V}$; $V_{VCAN} = 4.5\text{ V to }5.5\text{ V}$; $R_{LIN1} = R_{LIN2} = 500\text{ }\Omega$; $R_{(CANH-CANL)} = 60\text{ }\Omega$; $L_{SMPS}^{[1]} = 22\text{ }\mu\text{H}$; $C_{SMPS}^{[1]} = 22\text{ }\mu\text{F}$; $V_{VSMPS} = 6\text{ V}$ (SMPSOC = 0101); C_{V1} and $C_{VEXT} > 1.76\text{ }\mu\text{F}$; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at $V_{BATSMPS} = V_{BAT} = V_{BATV2} = V_{BATHS1} = V_{BATHS2} = 13\text{ V}$ and $T_{vj} = 25\text{ °C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Additional currents ... continued						
I _{DD}	supply current	CAN Offline Bias mode with active Partial Networking Decoder; Standby or Sleep mode; -40 °C < T _{vj} < 85 °C ^[2]	-	0.55	0.8	mA
		LIN1/2 Active mode; LIN recessive; V _{TXDL1/2} = V _{V1} ; 5 V < V _{BAT} < 18 V	-	1.8	2.6	mA
		LIN1/2 Active mode; LIN dominant; V _{TXDL1/2} = 0 V; 5 V < V _{BAT} < 18 V	-	2.8	6.7	mA
		LIN Listen-only mode; 5 V < V _{BAT} < 18 V	-	-	100	µA
Power on/off detection on pin BAT, VSMPS, BATHS1, BATHS2 and ADCCAP						
V _{th(det)pon}	power-on detection threshold voltage	on pin BAT or pin VSMPS, whichever is higher ^[3]	4.45	-	5.5	V
V _{hys(det)pon}	power-on detection hysteresis voltage	on pin BAT or pin VSMPS, whichever is higher	450	-	-	mV
V _{th(det)poff}	power-off detection threshold voltage	on pin BAT or pin VSMPS, whichever is higher	3.0	-	4.0	V
V _{uvd(CAN)}	CAN undervoltage detection voltage	on pin BAT or pin VSMPS, whichever is higher	4.45	-	5.5	V
V _{uvr(CAN)}	CAN undervoltage recovery voltage	on pin BAT or pin VSMPS, whichever is higher	4.7	-	6	V
V _{uvd}	undervoltage detection voltage	on pin BATHS1 or pin BATHS2	3.4	-	4.2	V
V _{uvd(LIN)}	LIN undervoltage detection voltage	on pin ADCCAP	4.4	4.7	5.0	V
V _{uvr(LIN)}	LIN undervoltage recovery voltage	on pin ADCCAP	4.9	5.2	5.5	V
V _{hys(ugd)LIN}	LIN undervoltage detection hysteresis voltage	on pin ADCCAP	200	-	-	mV
Overvoltage detection/release: supply pin BAT						
V _{th(det)ov}	overvoltage detection threshold voltage		30	-	34	V
V _{th(rel)ov}	overvoltage release threshold voltage		29	-	33	V

Table 104. Static characteristics...continued

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$; $V_{BATSMPS} = V_{BAT} = 2\text{ V}$ to 28 V ; $V_{BATV2} = 5.5\text{ V}$ to 28 V ; $V_{BATHS1} = V_{BATHS2} = 4.5\text{ V}$ to 28 V ; $V_{VCAN} = 4.5\text{ V}$ to 5.5 V ; $R_{LIN1} = R_{LIN2} = 500\text{ }\Omega$; $R_{(CANH-CANL)} = 60\text{ }\Omega$; $L_{SMPS}^{[1]} = 22\text{ }\mu\text{H}$; $C_{SMPS}^{[1]} = 22\text{ }\mu\text{F}$; $V_{VSMPS} = 6\text{ V}$ (SMPSOC = 0101); C_{V1} and $C_{VEXT} > 1.76\text{ }\mu\text{F}$; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at $V_{BATSMPS} = V_{BAT} = V_{BATV2} = V_{BATHS1} = V_{BATHS2} = 13\text{ V}$ and $T_{vj} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
High-speed CAN: pin VCAN						
V _{uvd} (VCAN)	undervoltage detection voltage on pin VCAN		4.5	-	4.75	V
I _{DD} (CAN)	CAN supply current	CAN Active mode; CAN recessive; V _{TXDC} = V _{V1}	1	3	6	mA
		CAN Active mode; CAN dominant; V _{TXDC} = 0 V; R _(CANH-CANL) = no load	3	7.5	15	mA
		CAN not in Active mode; -40 °C < T _{vj} < 85 °C	-	3	5	µA
		Normal mode; MC = 111; CAN Active mode; CAN dominant; V _{TXDC} = 0 V; short-circuit on bus lines; -3 V < (V _{CANH} = V _{CANL}) < +18 V	-	-	59	mA
SMPS pass-through suppression: pins BATSMPS and VSMPS						
V _{ovd} (BATSMPS)	overvoltage detection voltage on pin BATSMPS	V _{BATSMPS} rising	15	-	16	V
V _{uvd} (BATSMPS)	undervoltage detection voltage on pin BATSMPS	V _{BATSMPS} falling	7.1	-	7.7	V
I _{th} (ocd)	overcurrent detection threshold current	on pin VSMPS; for switching from Pass-through mode to an active mode				
		T _{vj} = -40 °C to +150 °C	150	-	350	mA
		T _{vj} = 150 °C	150	-	300	mA
SMPS: pins L1 and L2						
R _(L1-BATSMPS)	resistance between pin L1 and pin BATSMPS	Pass-through mode	-	-	0.8	Ω
R _(L2-VSMPS)	resistance between pin L2 and pin VSMPS	Pass-through mode	-	-	0.8	Ω
SMPS: pin VSMPS						
V _O	output voltage	I _{L(o)SMPS} = -500 mA to 0 mA ^[2] ^[4]	V _{VSMPS} (nom) × 0.95	V _{VSMPS} (nom)	V _{VSMPS} (nom) × 1.05	V
		SMPS active within regulation window ^[4]	V _{VSMPS} (act) - 60 mV	-	V _{VSMPS} (act) + 60 mV	V
I _{sc} (SMPS)	SMPS short circuit current	V _{BATSMPS} = 4 V	-	1.2	-	A
		V _{BATSMPS} = 8 V	-	1.4	-	A
		V _{BATSMPS} = 12 V	-	1.6	-	A
		V _{BATSMPS} = 16 V	-	1.85	-	A

Table 104. Static characteristics...continued

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$; $V_{BATSMPS} = V_{BAT} = 2\text{ V}$ to 28 V ; $V_{BATV2} = 5.5\text{ V}$ to 28 V ; $V_{BATHS1} = V_{BATHS2} = 4.5\text{ V}$ to 28 V ; $V_{VCAN} = 4.5\text{ V}$ to 5.5 V ; $R_{LIN1} = R_{LIN2} = 500\text{ }\Omega$; $R_{(CANH-CANL)} = 60\text{ }\Omega$; $L_{SMPS}^{[1]} = 22\text{ }\mu\text{H}$; $C_{SMPS}^{[1]} = 22\text{ }\mu\text{F}$; $V_{VSMPS} = 6\text{ V}$ (SMPSOC = 0101); C_{V1} and $C_{VEXT} > 1.76\text{ }\mu\text{F}$; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at $V_{BATSMPS} = V_{BAT} = V_{BATV2} = V_{BATHS1} = V_{BATHS2} = 13\text{ V}$ and $T_{vj} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SMPS performance: pin BATSMPS						
V _{DD}	supply voltage ^[2]	UJA1131A and UJA1132A; V _{VSMPS} = 6 V (SMPSOC = 0101)				
		I _{VSMPS} = -50 mA	2	-	28	V
		I _{VSMPS} = -150 mA	2.5	-	28	V
		I _{VSMPS} = -240 mA	3.25	-	28	V
		I _{VSMPS} = -400 mA	4.5	-	28	V
		I _{VSMPS} = -500 mA	5.5	-	28	V
		I _{VSMPS} = -700 mA	7.0	-	28	V
		UJA1131A and UJA1132A; V _{VSMPS} =7 V (SMPSOC = 1010)				
		I _{VSMPS} = -50 mA	2	-	28	V
		I _{VSMPS} = -110 mA	2.5	-	28	V
		I _{VSMPS} = -180 mA	3.25	-	28	V
		I _{VSMPS} = -300 mA	4.5	-	28	V
		I _{VSMPS} = -420 mA	5.5	-	28	V
		I _{VSMPS} = -640 mA	7.0	-	28	V
		UJA1135A and UJA1136A				
		I _{VSMPS} = -10 mA	2	-	28	V
		I _{VSMPS} = -500 mA	5.5	-	28	V
Voltage source; pin V1						
V _O	output voltage	V _{O(V1)nom} = 5 V; V _{SMPS} = 5.7 V to 16 V; I _{V1} = -400 mA to 0 mA	4.9	5	5.1	V
		V _{O(V1)nom} = 5 V; V _{SMPS} = 5.9 V to 16 V; I _{V1} = -500 mA to 0 mA	4.9	5	5.1	V
		I _{V1} = 50 μA to 50 mA	5.5	-	6	V
		V _{O(V1)nom} = 3.3 V; V _{SMPS} = 4.3 V to 16 V; I _{V1} = -500 mA to 0 mA	3.234	3.3	3.366	V
R _(VSMPS-V1)	resistance between pin VSMPS and pin V1	saturation down to power off; I _{V1} = -500 mA	-	-	2	Ω
V _{uvd}	undervoltage detection voltage	90 %; V _{O(V1)nom} = 5 V	4.5	-	4.75	V
		80 %; V _{O(V1)nom} = 5 V	4	-	4.25	V
		70 %; V _{O(V1)nom} = 5 V	3.5	-	3.75	V
		60 %; V _{O(V1)nom} = 5 V	3	-	3.25	V
		90 %; V _{O(V1)nom} = 3.3 V	2.97	-	3.135	V

Table 104. Static characteristics...continued

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$; $V_{BATSMPS} = V_{BAT} = 2\text{ V}$ to 28 V ; $V_{BATV2} = 5.5\text{ V}$ to 28 V ; $V_{BATHS1} = V_{BATHS2} = 4.5\text{ V}$ to 28 V ; $V_{VCAN} = 4.5\text{ V}$ to 5.5 V ; $R_{LIN1} = R_{LIN2} = 500\text{ }\Omega$; $R_{(CANH-CANL)} = 60\text{ }\Omega$; $L_{SMPS}^{[1]} = 22\text{ }\mu\text{H}$; $C_{SMPS}^{[1]} = 22\text{ }\mu\text{F}$; $V_{VSMPs} = 6\text{ V}$ (SMPSOC = 0101); C_{V1} and $C_{VEXT} > 1.76\text{ }\mu\text{F}$; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at $V_{BATSMPS} = V_{BAT} = V_{BATV2} = V_{BATHS1} = V_{BATHS2} = 13\text{ V}$ and $T_{vj} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{uvr}	undervoltage recovery voltage	90 %; $V_{O(V1)nom} = 5\text{ V}$	4.5	-	4.75	V
		90 %; $V_{O(V1)nom} = 3.3\text{ V}$	2.97	-	3.135	V
$I_{O(sc)}$	short-circuit output current		-900	-	-500	mA
Voltage source; pin V2/VEXT						
V_{uvd}	undervoltage detection voltage		4.5	-	4.75	V
V_{ovd}	overvoltage detection voltage		5.2	-	5.5	V
$I_{O(sc)}$	short-circuit output current		-280	-	-100	mA
V_O	output voltage	pin V2 shorted to pin VEXT; $V_{BATV2} = 5.7\text{ V}$ to 28 V ; $I_{V2} = -100\text{ mA}$ to 0 mA ; $C_{VEXT} > 3.3\text{ }\mu\text{F}$	4.9	5	5.1	V
		pin V2 not connected; $V_{BATV2} = 5.7\text{ V}$ to 28 V ; $I_{V2} = -5\text{ mA}$ to 0 mA	4.925	5	5.05	V
		pin V2 not connected; $V_{BATV2} = 5.7\text{ V}$ to 28 V ; $I_{V2} = -70\text{ mA}$ to -5 mA	4.9	5	5.1	V
$R_{(BATV2-V2)}$	resistance between pin BATV2 and pin V2	pin V2 shorted to pin VEXT on PCB; saturation; $I_{V2} = -100\text{ mA}$	-	-	7.5	Ω
$R_{(BATV2-VEXT)}$	resistance between pin BATV2 and pin VEXT	pin V2 not connected on PCB; saturation; $I_{VEXT} = -70\text{ mA}$	-	-	11	Ω
Serial peripheral interface inputs; pins SDI, SCK and SCSN						
$V_{th(sw)}$	switching threshold voltage	$V_{V1} = 2.97\text{ V}$ to 5.5 V	$0.25V_{V1}$	-	$0.75V_{V1}$	V
$V_{th(sw)hys}$	switching threshold voltage hysteresis		$0.05V_{V1}$	-	-	V
R_{pd}	pull-down resistance	on pin SCK	40	60	80	k Ω
		on pin SDI; $V_{SDI} < 0.25 \times V_{V1}$	40	60	80	k Ω
R_{pu}	pull-up resistance	on pin SCSN	40	60	80	k Ω
		on pin SDI; $V_{SDI} > 0.75 \times V_{V1}$	40	60	80	k Ω
$I_{LI(SDI)}$	input leakage current on pin SDI		-5	-	+5	μA
C_i	input capacitance	$V_i = V_{V1}$ ^[2]	-	3	6	pF

Table 104. Static characteristics...continued

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$; $V_{BATSMPS} = V_{BAT} = 2\text{ V}$ to 28 V ; $V_{BATV2} = 5.5\text{ V}$ to 28 V ; $V_{BATHS1} = V_{BATHS2} = 4.5\text{ V}$ to 28 V ; $V_{VCAN} = 4.5\text{ V}$ to 5.5 V ; $R_{LIN1} = R_{LIN2} = 500\text{ }\Omega$; $R_{(CANH-CANL)} = 60\text{ }\Omega$; $L_{SMPS}^{[1]} = 22\text{ }\mu\text{H}$; $C_{SMPS}^{[1]} = 22\text{ }\mu\text{F}$; $V_{VSMPs} = 6\text{ V}$ (SMPSOC = 0101); C_{V1} and $C_{VEXT} > 1.76\text{ }\mu\text{F}$; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at $V_{BATSMPS} = V_{BAT} = V_{BATV2} = V_{BATHS1} = V_{BATHS2} = 13\text{ V}$ and $T_{vj} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Serial peripheral interface data output; pin SDO						
V_{OH}	HIGH-level output voltage	$I_{OH} = -4\text{ mA}$; $V_{V1} = 2.97\text{ V}$ to 5.5 V	$V_{V1} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	$I_{OL} = 4\text{ mA}$; $V_{V1} = 2.97\text{ V}$ to 5.5 V	-	-	0.4	V
$I_{LO(off)}$	off-state output leakage current	$V_{SCSN} = V_{V1}$; $V_O = 0\text{ V}$ to V_{V1}	-5	-	+5	μA
C_o	output capacitance	$SCSN = V_{V1}$ [2]	-	3	6	pF
Reset input/output; pin RSTN						
V_{OL}	LOW-level output voltage	$V_{V1} = 1\text{ V}$ to 5.5 V ; pull-up resistor to $V_{V1} \geq 900\text{ }\Omega$; $-40\text{ }^{\circ}\text{C} < T_{vj} < T_{th(act)otp(max)}$	0	-	$0.2V_{V1}$	V
R_{pu}	pull-up resistance		40	60	80	k Ω
$V_{th(sw)}$	switching threshold voltage	$V_{V1} = 2.97\text{ V}$ to 5.5 V	$0.25V_{V1}$	-	$0.75V_{V1}$	V
$V_{th(sw)hys}$	switching threshold voltage hysteresis		$0.05V_{V1}$	-	-	V
Interrupt output; pin INTN1 and INTN2						
V_{OL}	LOW-level output voltage	$I_{OL} = 4\text{ mA}$; $V_{V1} = 2.97\text{ V}$ to 5.5 V	-	-	0.4	V
Enable output; pin EN						
V_{OH}	HIGH-level output voltage	$I_{OH} = -4\text{ mA}$; $V_{V1} = 2.97\text{ V}$ to 5.5 V	$V_{V1} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	$I_{OL} = 4\text{ mA}$; $V_{V1} = 1.0\text{ V}$ to 5.5 V	-	-	$0.2V_{V1}$	V
Limp home output; pin LIMP						
V_O	output voltage	$I_{LIMP} = 0.8\text{ mA}$; LHC = 1; $-40\text{ }^{\circ}\text{C} < T_{vj} < T_{th(act)otp(max)}$	-	-	0.4	V
I_L	leakage current	$V_{LIMP} = V_{BAT}$; LHC = 0	-	-	5	μA
CAN transmit data input; pin TXDC						
$V_{th(sw)}$	switching threshold voltage	$V_{V1} = 2.97\text{ V}$ to 5.5 V	$0.25V_{V1}$	-	$0.75V_{V1}$	V
$V_{th(sw)hys}$	switching threshold voltage hysteresis		$0.05V_{V1}$	-	-	V
R_{pu}	pull-up resistance		40	60	80	k Ω

Table 104. Static characteristics...continued

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$; $V_{BATSMPS} = V_{BAT} = 2\text{ V}$ to 28 V ; $V_{BATV2} = 5.5\text{ V}$ to 28 V ; $V_{BATHS1} = V_{BATHS2} = 4.5\text{ V}$ to 28 V ; $V_{VCAN} = 4.5\text{ V}$ to 5.5 V ; $R_{LIN1} = R_{LIN2} = 500\text{ }\Omega$; $R_{(CANH-CANL)} = 60\text{ }\Omega$; $L_{SMPS}^{[1]} = 22\text{ }\mu\text{H}$; $C_{SMPS}^{[1]} = 22\text{ }\mu\text{F}$; $V_{VSMPs} = 6\text{ V}$ (SMPSOC = 0101); C_{V1} and $C_{VEXT} > 1.76\text{ }\mu\text{F}$; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at $V_{BATSMPS} = V_{BAT} = V_{BATV2} = V_{BATHS1} = V_{BATHS2} = 13\text{ V}$ and $T_{vj} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CAN receive data output; pin RXDC						
V_{OH}	HIGH-level output voltage	$I_{OH} = -4\text{ mA}$; $V_{V1} = 2.97\text{ V}$ to 5.5 V	$V_{V1} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	$I_{OL} = 4\text{ mA}$; $V_{V1} = 2.97\text{ V}$ to 5.5 V	-	-	0.4	V
R_{pu}	pull-up resistance	CAN Offline mode	40	60	80	k Ω
High-speed CAN bus lines; pins CANH and CANL						
$V_{O(dom)}$	dominant output voltage	CAN Active mode; $V_{TXDC} = 0\text{ V}$; $R_L = 50\text{ }\Omega$ to $65\text{ }\Omega$				
		pin CANH	2.75	3.5	4.5	V
		pin CANL	0.5	1.5	2.25	V
$V_{dom(TX)sym}$	transmitter dominant voltage symmetry	$V_{dom(TX)sym} = V_{VCAN} - V_{CANH} - V_{CANL}$; $V_{VCAN} = 5\text{ V}$	-400	-	+400	mV
V_{TXsym}	transmitter voltage symmetry	$V_{TXsym} = V_{CANH} + V_{CANL}$; $C_{SPLIT} = 4.7\text{ nF}$; ^[2] $f_{TXD} = 250\text{ kHz}$, 1 MHz or 2.5 MHz ^[5]	$0.9V_{VCAN}$	-	$1.1V_{VCAN}$	V
$V_{O(dif)}$	differential output voltage	CAN Active mode (dominant); $V_{TXDC} = 0\text{ V}$; $V_{VCAN} = 4.75\text{ V}$ to 5.5 V				
		$R_{(CANH-CANL)} = 50\text{ }\Omega$ to $65\text{ }\Omega$	1.5	-	3.0	V
		$R_{(CANH-CANL)} = 45\text{ }\Omega$ to $70\text{ }\Omega$	1.4	-	3.3	V
		$R_{(CANH-CANL)} = 2240\text{ }\Omega$ ^[2]	1.5	-	5.0	V
		recessive; $R_{(CANH-CANL)} = \text{no load}$				
		CAN Active/Listen-only/Offline Bias modes; $V_{TXDC} = V_{V1}$	-50	-	+50	mV
		CAN Offline mode	-0.2	-	+0.2	V
$V_{O(rec)}$	recessive output voltage	CAN Active mode; $V_{TXDC} = V_{V1}$; $R_{(CANH-CANL)} = \text{no load}$	2.0	$0.5V_{VCAN}$	3.0	V
		CAN Offline mode; $R_{(CANH-CANL)} = \text{no load}$	-0.1	-	+0.1	V
		CAN Offline Bias/Listen-only modes; $V_{VCAN} = 0\text{ V}$; $R_{(CANH-CANL)} = \text{no load}$	2.0	2.5	3.0	V
$I_{O(sc)dom}$	dominant short-circuit output current	CAN Active mode; $V_{TXDC} = 0\text{ V}$; $V_{VCAN} = 5\text{ V}$				
		pin CANH; $-3\text{ V} \leq V_{CANH} \leq +27\text{ V}$	-55	-	-	mA
		pin CANL; $-15\text{ V} \leq V_{CANH} \leq +18\text{ V}$	-	-	55	mA
$I_{O(sc)rec}$	recessive short-circuit output current	$V_{CANL} = V_{CANH} = -27\text{ V}$ to $+32\text{ V}$; $V_{TXDC} = V_{V1}$	-3	-	+3	mA
$V_{rec(RX)}$	receiver recessive voltage	$-12\text{ V} \leq V_{CANL} \leq +12\text{ V}$; $-12\text{ V} \leq V_{CANH} \leq +12\text{ V}$				
		CAN Active/Listen-only modes	-4 ^[2]	-	+0.5	V

Table 104. Static characteristics...continued

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$; $V_{BATSMPS} = V_{BAT} = 2\text{ V}$ to 28 V ; $V_{BATV2} = 5.5\text{ V}$ to 28 V ; $V_{BATHS1} = V_{BATHS2} = 4.5\text{ V}$ to 28 V ; $V_{VCAN} = 4.5\text{ V}$ to 5.5 V ; $R_{LIN1} = R_{LIN2} = 500\text{ }\Omega$; $R_{(CANH-CANL)} = 60\text{ }\Omega$; $L_{SMPS}^{[1]} = 22\text{ }\mu\text{H}$; $C_{SMPS}^{[1]} = 22\text{ }\mu\text{F}$; $V_{VSMPS} = 6\text{ V}$ (SMPSOC = 0101); C_{V1} and $C_{VEXT} > 1.76\text{ }\mu\text{F}$; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at $V_{BATSMPS} = V_{BAT} = V_{BATV2} = V_{BATHS1} = V_{BATHS2} = 13\text{ V}$ and $T_{vj} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		CAN Offline/Offline Bias modes	-4 ^[2]	-	+0.4	V
$V_{\text{dom(RX)}}$	receiver dominant voltage	$-12\text{ V} \leq V_{\text{CANL}} \leq +12\text{ V}$; $-12\text{ V} \leq V_{\text{CANH}} \leq +12\text{ V}$				
		CAN Active/Listen-only modes	0.9	-	9.0 ^[2]	V
		CAN Offline/Offline Bias modes	1.15	-	9.0 ^[2]	V
$V_{\text{th(RX)dif}}$	differential receiver threshold voltage	CAN Active/Listen-only modes; $-12\text{ V} \leq V_{\text{CANL}} \leq +12\text{ V}$; $-12\text{ V} \leq V_{\text{CANH}} \leq +12\text{ V}$	0.5	0.7	0.9	V
		CAN Offline mode; $-12\text{ V} \leq V_{\text{CANL}} \leq +12\text{ V}$; $-12\text{ V} \leq V_{\text{CANH}} \leq +12\text{ V}$	0.4	0.7	1.15	V
$V_{\text{th(RX)dif(hys)}}$	differential receiver threshold voltage hysteresis	CAN Active mode; - $12\text{ V} < V_{\text{CANH}} < +12\text{ V}$; - $12\text{ V} < V_{\text{CANL}} < +12\text{ V}$	1	30	60	mV
R_i	input resistance	$-2\text{ V} \leq V_{\text{CANL}} \leq +7\text{ V}$; $-2\text{ V} \leq V_{\text{CANH}} \leq +7\text{ V}$	9	15	28	k Ω
ΔR_i	input resistance deviation	$0\text{ V} \leq V_{\text{CANL}} \leq +5\text{ V}$; $0\text{ V} \leq V_{\text{CANH}} \leq +5\text{ V}$	-1	-	+1	%
$R_{i(\text{dif})}$	differential input resistance	$-2\text{ V} \leq V_{\text{CANL}} \leq +7\text{ V}$; $-2\text{ V} \leq V_{\text{CANH}} \leq +7\text{ V}$; valid for all CAN operating modes	19	30	52	k Ω
C_i	input capacitance	CANH/CANL to GND ^[2]	-	-	20	pF
$C_{i(\text{dif})}$	differential input capacitance	^[2]	-	-	10	pF
I_L	leakage current	$V_{\text{BAT}} = 0\text{ V}$; $V_{\text{VCAN}} = 0\text{ V}$ or shorted to GND via 47 k Ω ; $V_{\text{CANH}} = V_{\text{CANL}} = 5\text{ V}$	-5	-	+5	μA
LIN transmit data inputs; pins TXDL1 and TXDL2						
$V_{\text{th(sw)}}$	switching threshold voltage	$V_{V1} = 2.97\text{ V}$ to 5.5 V	$0.25V_{V1}$	-	$0.75V_{V1}$	V
$V_{\text{th(sw)hys}}$	switching threshold voltage hysteresis		$0.05V_{V1}$	-	-	V
R_{pu}	pull-up resistance		40	60	80	k Ω
LIN receive data output; pin RXDL1, RXDL2						
V_{OH}	HIGH-level output voltage	$I_{\text{OH}} = -4\text{ mA}$; $V_{V1} = 2.97\text{ V}$ to 5.5 V	$V_{V1} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	$I_{\text{OL}} = 4\text{ mA}$; $V_{V1} = 2.97\text{ V}$ to 5.5 V	-	-	0.4	V
R_{pu}	pull-up resistance	LIN Offline mode	40	60	80	k Ω

Table 104. Static characteristics...continued

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$; $V_{BATSMPS} = V_{BAT} = 2\text{ V}$ to 28 V ; $V_{BATV2} = 5.5\text{ V}$ to 28 V ; $V_{BATHS1} = V_{BATHS2} = 4.5\text{ V}$ to 28 V ; $V_{VCAN} = 4.5\text{ V}$ to 5.5 V ; $R_{LIN1} = R_{LIN2} = 500\text{ }\Omega$; $R_{(CANH-CANL)} = 60\text{ }\Omega$; $L_{SMPS}^{[1]} = 22\text{ }\mu\text{H}$; $C_{SMPS}^{[1]} = 22\text{ }\mu\text{F}$; $V_{VSMPS} = 6\text{ V}$ (SMPSOC = 0101); C_{V1} and $C_{VEXT} > 1.76\text{ }\mu\text{F}$; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at $V_{BATSMPS} = V_{BAT} = V_{BATV2} = V_{BATHS1} = V_{BATHS2} = 13\text{ V}$ and $T_{vj} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LIN bus line; pin LIN1, LIN2						
I_{BUS_LIM}	current limitation for driver dominant state	LIN Active mode; $V_{BAT} = V_{LIN1} = V_{LIN2} = 18\text{ V}$; $V_{TXDL1} = V_{TXDL2} = 0\text{ V}$	40	-	200	mA
$I_{BUS_PAS_rec}$	receiver recessive input leakage current	$5\text{ V} < V_{LINn} < 18\text{ V}$; $5\text{ V} < V_{BAT} < 18\text{ V}$; $V_{LINn} \geq V_{BAT}$; $V_{TXDLn} = V_{V1}$	-	-	20	μA
$I_{BUS_PAS_dom}$	receiver dominant input leakage current including pull-up resistor	$V_{TXDLn} = V_{V1}$; $V_{LINn} = 0\text{ V}$; $V_{BAT} = 12\text{ V}$	-1	-	-	mA
$I_{BUS_NO_GND}$	loss-of-ground bus current	$V_{BAT} = 12\text{ V}$; $V_{GND} = V_{BAT}$; $0\text{ V} < V_{LINn} < 18\text{ V}$	-1	-	+1	mA
$I_{BUS_NO_BAT}$	loss-of-battery bus current	$V_{BAT} = 0\text{ V}$; $0\text{ V} < V_{LINn} < 18\text{ V}$	-	-	30	μA
V_{BUSrec}	receiver recessive state	$V_{BAT} = 5\text{ V}$ to 18 V	$0.6V_{BAT}$	-	-	V
V_{BUSdom}	receiver dominant state	$V_{BAT} = 5\text{ V}$ to 18 V	-	-	$0.4V_{BAT}$	V
V_{BUS_CNT}	receiver center voltage	$V_{BUS_CNT} = (V_{BUSrec} + V_{BUSdom})/2$; $V_{BAT} = 5\text{ V}$ to 18 V ; LIN Active mode	$0.475 \times V_{BAT}$	$0.5 \times V_{BAT}$	$0.525 \times V_{BAT}$	V
V_{HYS}	receiver hysteresis voltage	$V_{HYS} = V_{BUSrec} - V_{BUSdom}$; $V_{BAT} = 5\text{ V}$ to 18 V ; LIN Active mode	-	-	$0.175 \times V_{BAT}$	V
$V_{SerDiode}$	voltage drop at the serial diode	in pull-up path with $R_{responder}$; $I_{SerDiode} = 0.9\text{ mA}$	0.4	-	1	V
C_{LIN}	capacitance on pin LIN	with respect to GND; on pins LIN1 and LIN2 ^[2]	-	-	30	pF
$R_{responder}$	responder resistance		20	30	60	k Ω
High-voltage I/O: pins HVIO1 to HVIO8						
$V_{th(sw)f}$	falling switching threshold voltage	absolute wake-up threshold: B0WTC = B1WTC = 1	2.4	-	3.75	V
$V_{th(sw)r}$	rising switching threshold voltage	absolute wake-up threshold: B0WTC = B1WTC = 1	2.8	-	4.1	V
$V_{th(sw)}$	switching threshold voltage	ratiometric wake-up threshold: B0WTC = B1WTC = 0	$0.38 \times V_{BATHSx}$	$0.5 \times V_{BATHSx}$	$0.6 \times V_{BATHSx}$	V
$V_{hys(I)}$	input hysteresis voltage	absolute wake-up threshold: B0WTC = B1WTC = 1	250	-	800	mV
		ratiometric wake-up threshold: B0WTC = B1WTC = 0	$0.025 \times V_{BATHSx}$	-	$0.2 \times V_{BATHSx}$	V
I_i	input current	at wake-up	-	-	5	μA

Table 104. Static characteristics...continued

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$; $V_{BATSMPS} = V_{BAT} = 2\text{ V}$ to 28 V ; $V_{BATV2} = 5.5\text{ V}$ to 28 V ; $V_{BATHS1} = V_{BATHS2} = 4.5\text{ V}$ to 28 V ; $V_{VCAN} = 4.5\text{ V}$ to 5.5 V ; $R_{LIN1} = R_{LIN2} = 500\text{ }\Omega$; $R_{(CANH-CANL)} = 60\text{ }\Omega$; $L_{SMPS}^{[1]} = 22\text{ }\mu\text{H}$; $C_{SMPS}^{[1]} = 22\text{ }\mu\text{F}$; $V_{VSMPS} = 6\text{ V}$ (SMPSOC = 0101); C_{V1} and $C_{VEXT} > 1.76\text{ }\mu\text{F}$; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at $V_{BATSMPS} = V_{BAT} = V_{BATV2} = V_{BATHS1} = V_{BATHS2} = 13\text{ V}$ and $T_{vj} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{on}	on-state resistance	between pins BATHSx and HVION pins; ^[6] HVION configured as high-side driver; $I_{HVION} = -60\text{ mA}$	-	-	24	Ω
		between pins BATHSx and HVION pins; ^{[6][2]} HVION configured as high-side driver; $I_{HVION} = -60\text{ mA}$; $T_{vj} = 175\text{ }^{\circ}\text{C}$	-	-	27	Ω
		between pins HVION and GND; HVION configured as low-side driver; $I_{HVION} = 60\text{ mA}$	-	-	24	Ω
		between pins HVION and GND; ^[2] HVION configured as low-side driver; $I_{HVION} = 60\text{ mA}$; $T_{vj} = 175\text{ }^{\circ}\text{C}$	-	-	27	Ω
ΔR_{on}	on-state resistance difference	between BATHSx and HVION pairs; ^[6] HVION configured as high-side driver; $I_{HVION} = -60\text{ mA}$	-	-	5	%
		between HVION and GND pairs; HVION configured as low-side driver; $I_{HVION} = 60\text{ mA}$	-	-	10	%
$I_{O(sc)}$	short-circuit output current	peak value; HVION configured as high-side driver; $V_{HVION} = 0\text{ V}$ ^[2]	-1.3	-	-	A
		peak value; HVION configured as low-side driver; $V_{HVION} = 18\text{ V}$ ^[2]	-	-	1.3	A
I_L	leakage current	output drivers configured and off; ^[2] $0\text{ V} < V_{HVION} < 18\text{ V}$	-5	-	5	μA
$I_{th(det)sc}$	short-circuit detection threshold current	HVION high-side driver ^[7]				
		$I_{OnSCTC} = 00$	-36	-30	-24	mA
		$I_{OnSCTC} = 01$	-54	-45	-36	mA
		$I_{OnSCTC} = 10$	-72	-60	-48	mA
		$I_{OnSCTC} = 11$	-108	-90	-72	mA
		HVION low-side driver				
		$I_{OnSCTC} = 00$	24	30	36	mA
		$I_{OnSCTC} = 01$	36	45	54	mA
		$I_{OnSCTC} = 10$	48	60	72	mA
		$I_{OnSCTC} = 11$	72	90	108	mA
$I_{th(det)open}$	open load detection threshold current	HVION high-side driver				
		$I_{OnOLTC} = 00$	-4.1	-2	-1.25	mA
		$I_{OnOLTC} = 01$	-7	-5	-4	mA
		$I_{OnOLTC} = 10$	-13	-10	-8	mA

Table 104. Static characteristics...continued

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$; $V_{BATSMPS} = V_{BAT} = 2\text{ V}$ to 28 V ; $V_{BATV2} = 5.5\text{ V}$ to 28 V ; $V_{BATHS1} = V_{BATHS2} = 4.5\text{ V}$ to 28 V ; $V_{VCAN} = 4.5\text{ V}$ to 5.5 V ; $R_{LIN1} = R_{LIN2} = 500\text{ }\Omega$; $R_{(CANH-CANL)} = 60\text{ }\Omega$; $L_{SMPS}^{[1]} = 22\text{ }\mu\text{H}$; $C_{SMPS}^{[1]} = 22\text{ }\mu\text{F}$; $V_{VSMPS} = 6\text{ V}$ (SMPSOC = 0101); C_{V1} and $C_{VEXT} > 1.76\text{ }\mu\text{F}$; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at $V_{BATSMPS} = V_{BAT} = V_{BATV2} = V_{BATHS1} = V_{BATHS2} = 13\text{ V}$ and $T_{vj} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		IO _{OLTC} = 11	-25	-20	-16	mA
		HVIO _{On} low-side driver				
		IO _{OLTC} = 00	1.25	2	6	mA
		IO _{OLTC} = 01	4	5	9	mA
		IO _{OLTC} = 10	8	10	13	mA
		IO _{OLTC} = 11	16	20	24	mA
I _{sink(act)} HVIO	HVIO activation sink current	HVIO configured as low-side driver with slope control (IO _{NC} = 010); V _{HVIO_{On}} = 2.0 V	70	125	170	mA
Battery monitoring; pins BAT and BATSENSE						
V _i	input voltage	conversion range; V _{VSMPS(nom)} = 6 V to 8 V	2	-	20	V
V _{ADC(acc)}	ADC voltage accuracy	accuracy of ADC conversion results stored in bits BMBCD and BMSCD (see Section 7.7.2)	-300	-	+300	mV
Battery input filter capacitor; pin ADCCAP						
R _(BAT-ADCCAP)	resistance between pin BAT and pin ADCCAP		0.5	1	1.7	k Ω
MTP non-volatile memory						
N _{cy(W)} MTP	number of MTP write cycles	^[2]	-	-	200	-
V _{prog(MTPNV)}	MTPNV programming voltage	^[2]	6	-	28	V
Temperature protection						
T _{th(act)otp}	overtemperature protection activation threshold temperature		167	177	187	$^{\circ}\text{C}$
T _{th(rel)otp}	overtemperature protection release threshold temperature		127	137	147	$^{\circ}\text{C}$
T _{th(warn)otp}	overtemperature protection warning threshold temperature		127	137	147	$^{\circ}\text{C}$

[1] L_{SMPS} and C_{SMPS} are external components needed to configure the SMPS. See [Section 7.7.4](#).

[2] Not tested in production; guaranteed by design.

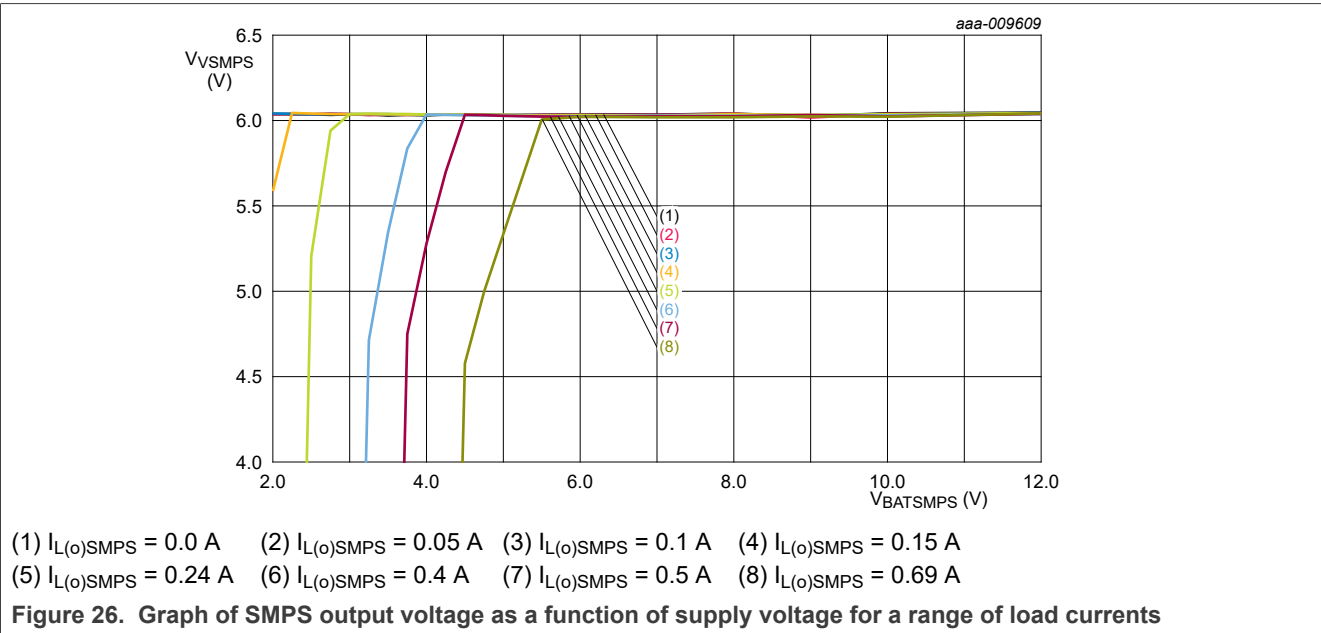
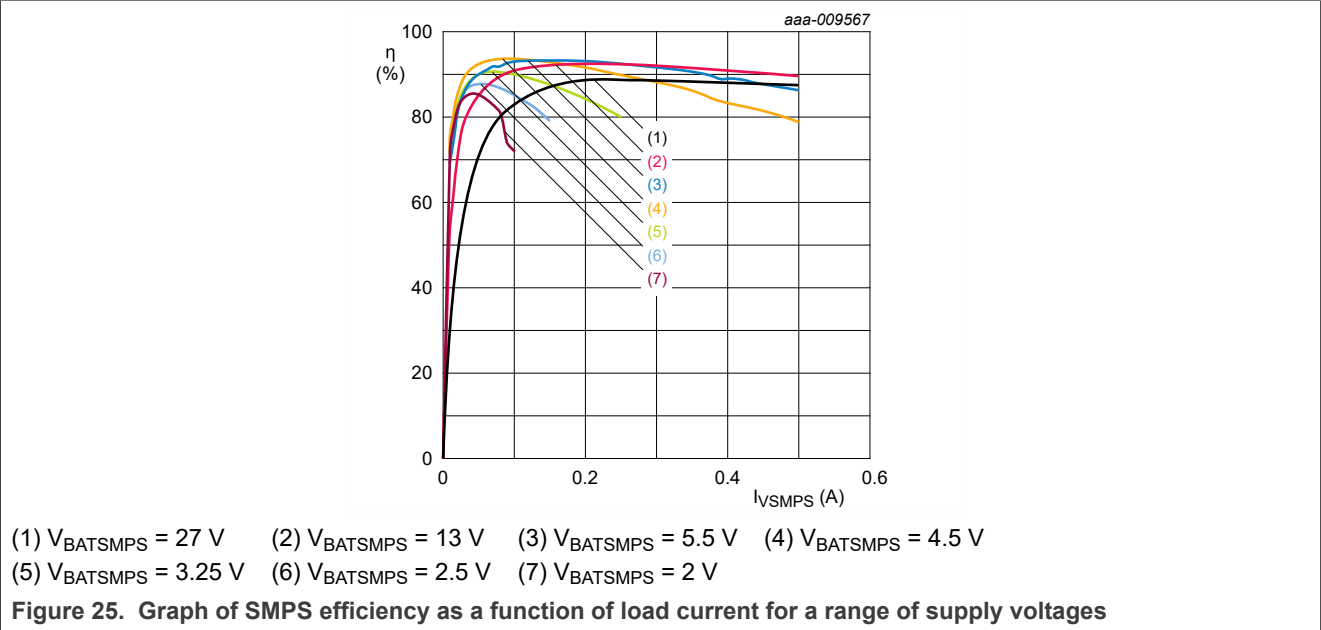
[3] For exceptions, see [Section 7.1.3](#).

[4] V_{VSMPS(nom)} is between 5 V and 8 V and is selected via bits SMPSOC (see [Table 30](#))

[5] The test circuit used to measure the bus output voltage symmetry (which includes C_{SPLIT}) is shown in [Figure 33](#).

[6] When x = 1, n = 1 to 4; when x = 2, n = 5 to 8.

[7] A level on the pin below than -0.8 V may be interpreted as a short circuit.



11 Dynamic characteristics

Table 105. Dynamic characteristics

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$; $V_{BATSMPS} = V_{BAT} = 2\text{ V}$ to 28 V ; $V_{BATV2} = 5.5\text{ V}$ to 28 V ; $V_{BATHS1} = V_{BATHS2} = 4.5\text{ V}$ to 28 V ; $V_{VCAN} = 4.5\text{ V}$ to 5.5 V ; $R_{LIN1} = R_{LIN2} = 500\text{ }\Omega$; $R_{CANH-CANL} = 60\text{ }\Omega$; $L_{SMPS}^{[1]} = 22\text{ }\mu\text{H}$; $C_{SMPS}^{[1]} = 22\text{ }\mu\text{F}$; $V_{VSMPS} = 6\text{ V}$ (SMPSOC = 0101); C_{V1} and $C_{VEXT} > 1.76\text{ }\mu\text{F}$; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at $V_{BATSMPS} = V_{BAT} = V_{BATV2} = V_{BATHS1} = V_{BATHS2} = 13\text{ V}$ and $T_{vj} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SMPS						
f_{sw}	switching frequency		315	380	465	kHz
$t_{to(reg)}$	regulation time-out time	SMPSS is set to 1 when V_{VSMPS} is outside the regulation window for longer than $t_{to(reg)}$	137	-	203	μs
$t_{d(act)}$	active mode delay time	minimum time SMPS spends in switched mode before a new mode transition can be attempted				
		Pass-through mode and $(I_{L(o)SMPS} > I_{th(ocd)}(V_{SMPS}))$ or $(V_{BATSMPS} < V_{UVD(BATSMPS)})$ or $(V_{BATSMPS} > V_{OVD(BATSMPS)})$	0.9	1	1.1	ms
$t_{t(sw-pt)}$	transition time from switched mode to pass-through mode		2.7	3	3.3	ms
Battery supply						
$t_{startup}$	start-up time	from V_{BAT} exceeding the power-on detection threshold until V_{V1} exceeds the 90 % undervoltage threshold; $C_{V1} < 10\text{ }\mu\text{F}$; $-500\text{ mA} < I_{V1} < 0\text{ mA}$	[2]	1	2.1	ms
$t_{det(ov)}$	overvoltage detection time	from overvoltage threshold exceeded to OVSDI interrupt	400	-	480	ms
$t_{d(sd)ov}$	overvoltage shutdown delay time	after OVSDI interrupt	100	-	120	ms
$t_{det(ov)LIN}$	LIN overvoltage detection time	from overvoltage threshold exceeded to entering LIN Off mode	[2]	-	1.1	ms
Voltage source; pin V1						
$t_{det(uv)}$	undervoltage detection time	V_{V1} falling	[3]	-	39	μs
$t_{d(uvd-RSTNL)}$	delay time from undervoltage detection to RSTN LOW		-	-	40	μs
HS-CAN transceiver supply; pin VCAN						
$t_{det(uv)}$	undervoltage detection time	V_{VCAN} falling	[3]	-	32	μs

Table 105. Dynamic characteristics...continued

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$; $V_{BATSMPS} = V_{BAT} = 2\text{ V}$ to 28 V ; $V_{BATV2} = 5.5\text{ V}$ to 28 V ; $V_{BATHS1} = V_{BATHS2} = 4.5\text{ V}$ to 28 V ; $V_{VCAN} = 4.5\text{ V}$ to 5.5 V ; $R_{LIN1} = R_{LIN2} = 500\text{ }\Omega$; $R_{(CANH-CANL)} = 60\text{ }\Omega$; $L_{SMPS}^{[1]} = 22\text{ }\mu\text{H}$; $C_{SMPS}^{[1]} = 22\text{ }\mu\text{F}$; $V_{VSMPS} = 6\text{ V}$ (SMPSOC = 0101); C_{V1} and $C_{VEXT} > 1.76\text{ }\mu\text{F}$; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at $V_{BATSMPS} = V_{BAT} = V_{BATV2} = V_{BATHS1} = V_{BATHS2} = 13\text{ V}$ and $T_{vj} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage source; pin VEXT						
$t_{det(uv)}$	undervoltage detection time	V_{VEXT} falling ^[3]	6	-	39	μs
		at start-up of VEXT; V_{VEXT} falling	2.2	2.5	2.8	ms
$t_{det(ov)}$	overvoltage detection time	V_{VEXT} rising ^[3]	6	-	39	μs
Serial peripheral interface timing; pins SCSN, SCK, SDI and SDO; see Figure 30						
$t_{cy(clk)}$	clock cycle time	$V_{V1} = 2.97\text{ V}$ to 5.5 V	250	-	-	ns
$t_{SPILEAD}$	SPI enable lead time	$V_{V1} = 2.97\text{ V}$ to 5.5 V	50	-	-	ns
t_{SPILAG}	SPI enable lag time	$V_{V1} = 2.97\text{ V}$ to 5.5 V	50	-	-	ns
$t_{clk(H)}$	clock HIGH time	$V_{V1} = 2.97\text{ V}$ to 5.5 V	100	-	-	ns
$t_{clk(L)}$	clock LOW time	$V_{V1} = 2.97\text{ V}$ to 5.5 V	100	-	-	ns
$t_{su(D)}$	data input set-up time	$V_{V1} = 2.97\text{ V}$ to 5.5 V	50	-	-	ns
$t_{h(D)}$	data input hold time	$V_{V1} = 2.97\text{ V}$ to 5.5 V	50	-	-	ns
$t_{v(Q)}$	data output valid time	pin SDO; $V_{V1} = 2.97\text{ V}$ to 5.5 V ; $C_L = 20\text{ pF}$	-	-	50	ns
$t_{d(SDI-SDO)}$	SDI to SDO delay time	SPI address bits and read-only bit; $C_L = 20\text{ pF}$	-	-	50	ns
$t_{WH(S)}$	chip select pulse width HIGH	$V_{V1} = 2.97\text{ V}$ to 5.5 V	250	-	-	ns
$t_{to(SPI)}$	SPI time-out time	after leaving Reset mode; $V_{V1} = 2.97\text{ V}$ to 5.5 V	-	-	53	μs
$t_{d(W)SPI}$	SPI write delay time	between two consecutive write access operations	-	-	10	μs
$t_{d(SCKL-SCSNL)}$	delay time from SCK LOW to SCSN LOW		50	-	-	ns
Reset input/output; pin RSTN						
$t_{w(rst)}$	reset pulse width	output pulse width				
		RLC = 00	20	-	25	ms
		RLC = 01	10	-	12.5	ms
		RLC = 10	3.6	-	5	ms
		RLC = 11	1	-	1.5	ms
		input pulse width	18	-	-	μs
$t_{to(rst)}$	reset time-out time		120	135	150	ms

Table 105. Dynamic characteristics...continued

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$; $V_{BATSMPS} = V_{BAT} = 2\text{ V}$ to 28 V ; $V_{BATV2} = 5.5\text{ V}$ to 28 V ; $V_{BATHS1} = V_{BATHS2} = 4.5\text{ V}$ to 28 V ; $V_{VCAN} = 4.5\text{ V}$ to 5.5 V ; $R_{LIN1} = R_{LIN2} = 500\text{ }\Omega$; $R_{(CANH-CANL)} = 60\text{ }\Omega$; $L_{SMPS}^{[1]} = 22\text{ }\mu\text{H}$; $C_{SMPS}^{[1]} = 22\text{ }\mu\text{F}$; $V_{VSMPS} = 6\text{ V}$ (SMPSOC = 0101); C_{V1} and $C_{VEXT} > 1.76\text{ }\mu\text{F}$; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at $V_{BATSMPS} = V_{BAT} = V_{BATV2} = V_{BATHS1} = V_{BATHS2} = 13\text{ V}$ and $T_{vj} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Interrupt time-out; pin INTN1						
$t_{to(int)}$	interrupt time-out time	INTN1 remains HIGH for at least $t_{to(int)}$ after being released	0.9	1	1.1	ms
High-voltage I/O: pins HVIO1 to HVIO8						
$t_{w(wake)}$	wake-up pulse width	input configuration; interrupt enabled	51.5	-	-	μs
$f_{s(wake)}$	wake-up sampling frequency		55	-	142	kHz
$t_{det(fail)HVIO}$	HVIO failure detection time	open-load detection, HVIO already running ^[4]	18	21	24	μs
		overcurrent detection, HVIO already running ^[4]	12	27	30	μs
$t_{rec(fail)HVIO}$	HVIO failure recovery time	open-load recovery, HVIO already running ^[5]	30	34	38	μs
$t_{d(on)HVIO}$	HVIO turn-on delay time	fast slope	36	40	44	μs
		slow slope	72	80	88	μs
$t_{d(fdet-INTN1L)}$	delay time from failure detection to INTN1 LOW		-	8	9	μs
Battery monitoring: pins BAT, BATSENSE						
$t_c(ADC)$	ADC conversion time	time taken to measure and convert input voltage and store result in bits BMBCD or BMSCD (see Section 7.7.2); Normal mode; $0\text{ V} < V_{BAT} < 20\text{ V}$	5.4	6	6.6	μs
CAN transceiver timing; pins CANH, CANL, TXDC and RXDC; see Figure 27 , Figure 28 , Figure 32 and Figure 33						
$t_{d(TXDC-busdom)}$	delay time from TXDC to bus dominant		-	55	-	ns
$t_{d(TXDC-busrec)}$	delay time from TXDC to bus recessive		-	65	-	ns
$t_{d(busdom-RXDC)}$	delay time from bus dominant to RXDC	$C_{RXDC} = 15\text{ pF}$	-	105	-	ns
$t_{d(busrec-RXDC)}$	delay time from bus recessive to RXDC	$C_{RXDC} = 15\text{ pF}$	-	125	-	ns
$t_{d(TXDCH-RXDCH)}$	delay time from TXDC HIGH to RXDC HIGH	$70\% V_{TXDC}$ to $70\% V_{RXDC}$; $C_{RXDC} = 15\text{ pF}$; $t_{bit(TXDC)} = 200\text{ ns}$; $C_{(CANH-CANL)} = 100\text{ pF}$;	-	-	255	ns
$t_{d(TXDCL-RXDCL)}$	delay time from TXDC LOW to RXDC LOW	$30\% V_{TXDC}$ to $30\% V_{RXDC}$; $C_{RXDC} = 15\text{ pF}$; $t_{bit(TXDC)} = 200\text{ ns}$; $C_{(CANH-CANL)} = 100\text{ pF}$;	-	-	255	ns

Table 105. Dynamic characteristics...continued

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$; $V_{BATSMPS} = V_{BAT} = 2\text{ V}$ to 28 V ; $V_{BATV2} = 5.5\text{ V}$ to 28 V ; $V_{BATHS1} = V_{BATHS2} = 4.5\text{ V}$ to 28 V ; $V_{VCAN} = 4.5\text{ V}$ to 5.5 V ; $R_{LIN1} = R_{LIN2} = 500\text{ }\Omega$; $R_{(CANH-CANL)} = 60\text{ }\Omega$; $L_{SMPS}^{[1]} = 22\text{ }\mu\text{H}$; $C_{SMPS}^{[1]} = 22\text{ }\mu\text{F}$; $V_{VSMPS} = 6\text{ V}$ ($SMPSOC = 0101$); C_{V1} and $C_{VEXT} > 1.76\text{ }\mu\text{F}$; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at $V_{BATSMPS} = V_{BAT} = V_{BATV2} = V_{BATHS1} = V_{BATHS2} = 13\text{ V}$ and $T_{vj} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{bit(RXDC)}$	bit time on pin RXDC	$t_{bit(TXDC)} = 500\text{ ns}$	400	-	550	ns
		$t_{bit(TXDC)} = 200\text{ ns}$	120	-	220	ns
$t_{bit(bus)}$	transmitted recessive bit width	$t_{bit(TXD)} = 500\text{ ns}$	435	-	530	ns
		$t_{bit(TXD)} = 200\text{ ns}$	155	-	210	ns
Δt_{rec}	receiver timing symmetry	$t_{bit(TXD)} = 500\text{ ns}$	-65	-	+40	ns
		$t_{bit(TXD)} = 200\text{ ns}$	-45	-	+15	ns
$t_{wake(busdom)}$	bus dominant wake-up time	first pulse (after first recessive) for wake-up on pins CANH and CANL Sleep mode ^[6]	0.5	-	1.8	μs
		second pulse for wake-up on pins CANH and CANL ^[6]	0.5	-	1.8	μs
$t_{wake(busrec)}$	bus recessive wake-up time	first pulse for wake-up on pins CANH and CANL; Sleep mode ^[6]	0.5	-	1.8	μs
		second pulse (after first dominant) for wake-up on pins CANH and CANL ^[6]	0.5	-	1.8	μs
$t_{to(wake)bus}$	bus wake-up time-out time	between first and second dominant pulses; CAN Offline mode ^[7]	0.8	-	10	ms
$t_{to(dom)TXDC}$	TXDC dominant time-out time	CAN Active mode; $V_{TXDC} = 0\text{ V}$ ^[7]	0.8	3	5	ms
$t_{to(silence)}$	bus silence time-out time	recessive time measurement started in all CAN modes ^[7]	0.8	1	1.2	s
$t_{d(busact-bias)}$	delay time from bus active to bias		-	-	200	μs
$t_{d(act)CAN}$	CAN activation delay time	MC = 111; CAN entering CAN Active mode; $t_{d(act)norm}$ expired	-	-	24	μs
CAN partial networking						
$N_{bit(idle)}$	number of idle bits	before a new SOF is accepted; CFDC = 1 ^[2]	6	-	10	-
$t_{fltr(bit)dom}$	dominant bit filter time	arbitration data rate $\leq 500\text{ kbit/s}$; CFDC = 1 ^{[2][8]}	5	-	17.5	%
LIN transceivers; pins LIN1, LIN2, TXDL1, TXDL2, RXDL1, RXDL2						
$\delta 1$	duty cycle 1	$V_{th(rec)(max)} = 0.744V_{BAT}$; $V_{th(dom)(max)} = 0.581V_{BAT}$; $t_{bit} = 50\text{ }\mu\text{s}$; $V_{BAT} = 7\text{ V}$ to 18 V ^{[9][10][11]}	0.396	-	-	
		$V_{th(rec)(max)} = 0.768V_{BAT}$; $V_{th(dom)(max)} = 0.6V_{BAT}$; $t_{bit} = 50\text{ }\mu\text{s}$; $V_{BAT} = 5\text{ V}$ to 7 V ^{[9][10][11]}	0.396	-	-	

Table 105. Dynamic characteristics...continued

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$; $V_{BATSMPS} = V_{BAT} = 2\text{ V}$ to 28 V ; $V_{BATV2} = 5.5\text{ V}$ to 28 V ; $V_{BATHS1} = V_{BATHS2} = 4.5\text{ V}$ to 28 V ; $V_{VCAN} = 4.5\text{ V}$ to 5.5 V ; $R_{LIN1} = R_{LIN2} = 500\text{ }\Omega$; $R_{(CANH-CANL)} = 60\text{ }\Omega$; $L_{SMPS}^{[1]} = 22\text{ }\mu\text{H}$; $C_{SMPS}^{[1]} = 22\text{ }\mu\text{F}$; $V_{VSMPS} = 6\text{ V}$ (SMP SOC = 0101); C_{V1} and $C_{VEXT} > 1.76\text{ }\mu\text{F}$; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at $V_{BATSMPS} = V_{BAT} = V_{BATV2} = V_{BATHS1} = V_{BATHS2} = 13\text{ V}$ and $T_{vj} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\delta 2$	duty cycle 2	$V_{th(rec)(min)} = 0.442V_{BAT}$; ^{[10][11][12]} $V_{th(dom)(min)} = 0.284V_{BAT}$; $t_{bit} = 96\text{ }\mu\text{s}$; $V_{BAT} = 7.6\text{ V}$ to 18 V	-	-	0.581	
		$V_{th(rec)(min)} = 0.405V_{BAT}$; ^{[10][11][12]} $V_{th(dom)(min)} = 0.271V_{BAT}$; $t_{bit} = 96\text{ }\mu\text{s}$; $V_{BAT} = 5.6\text{ V}$ to 7.6 V	-	-	0.581	
$\delta 3$	duty cycle 3	$V_{th(rec)(max)} = 0.778V_{BAT}$; ^{[9][10][11]} $V_{th(dom)(max)} = 0.616V_{BAT}$; $t_{bit} = 96\text{ }\mu\text{s}$; $V_{BAT} = 7\text{ V}$ to 18 V	0.417	-	-	
		$V_{th(rec)(max)} = 0.805V_{BAT}$; ^{[9][10][11]} $V_{th(dom)(max)} = 0.637V_{BAT}$; $t_{bit} = 96\text{ }\mu\text{s}$; $V_{BAT} = 5\text{ V}$ to 7 V	0.417	-	-	
$\delta 4$	duty cycle 4	$V_{th(rec)(min)} = 0.389V_{BAT}$; ^{[10][11][12]} $V_{th(dom)(min)} = 0.251V_{BAT}$; $t_{bit} = 96\text{ }\mu\text{s}$; $V_{BAT} = 7.6\text{ V}$ to 18 V	-	-	0.590	
		$V_{th(rec)(min)} = 0.372V_{BAT}$; ^{[10][11][12]} $V_{th(dom)(min)} = 0.238V_{BAT}$; $t_{bit} = 96\text{ }\mu\text{s}$; $V_{BAT} = 5.6\text{ V}$ to 7.6 V	-	-	0.590	
t_{rx_pd}	receiver propagation delay	rising and falling; ^[11] $C_{RXD} = 20\text{ pF}$	-	-	6	μs
t_{rx_sym}	receiver propagation delay symmetry	$C_{RXD} = 20\text{ pF}$; rising edge with respect to falling edge ^[11]	-2	-	+2	μs
$t_{wake(dom)LIN}$	LIN dominant wake-up time	LIN Offline mode	30	80	150	μs
$t_{to(dom)TXDL}$	TXDL dominant time-out time	LIN Active mode; $V_{TXDL} = 0\text{ V}$ ^[7]	28	32	36	ms
Mode transition						
$t_{d(act)norm}$	normal mode activation delay time	MC = 111; delay before CAN and LIN transceivers, battery monitoring and HVIO low side drivers are activated after the SBC switches to Normal mode ^[2]	-	-	320	μs
MTP non-volatile memory						
$t_{ret(data)}$	data retention time	$T_{vj} = 90\text{ }^{\circ}\text{C}$	20	-	-	year
$t_{d(MTPNV)}$	MTPNV delay time	before factory presets are restored; $V_{RSTN} = 0\text{ V}$, $V_{CANL} = 0\text{ V}$ and $V_{CANH} > 5\text{ V}$ during power-up with $V_{BAT} = 7.7\text{ V}$ to 28 V	0.9	1	1.1	s
$t_{prog(MTPNV)}$	MTPNV programming time	correct CRC code received at address 0x75; $V_{BAT} = 6\text{ V}$ to 28 V	43	48	53	ms

Table 105. Dynamic characteristics...continued

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$; $V_{BATSMPS} = V_{BAT} = 2\text{ V}$ to 28 V ; $V_{BATV2} = 5.5\text{ V}$ to 28 V ; $V_{BATHS1} = V_{BATHS2} = 4.5\text{ V}$ to 28 V ; $V_{VCAN} = 4.5\text{ V}$ to 5.5 V ; $R_{LIN1} = R_{LIN2} = 500\text{ }\Omega$; $R_{(CANH-CANL)} = 60\text{ }\Omega$; $L_{SMPS}^{[1]} = 22\text{ }\mu\text{H}$; $C_{SMPS}^{[1]} = 22\text{ }\mu\text{F}$; $V_{VSMPS} = 6\text{ V}$ (SMPSOC = 0101); C_{V1} and $C_{VEXT} > 1.76\text{ }\mu\text{F}$; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at $V_{BATSMPS} = V_{BAT} = V_{BATV2} = V_{BATHS1} = V_{BATHS2} = 13\text{ V}$ and $T_{vj} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Watchdog						
$t_{\text{trig(wd)1}}$	watchdog trigger time 1	Normal mode watchdog Window mode only ^[13]	$0.45 \times \text{NWP}^{[14]}$	-	$0.55 \times \text{NWP}^{[14]}$	ms
$t_{\text{trig(wd)2}}$	watchdog trigger time 2	Normal, Standby and Sleep modes; watchdog Window and Timeout modes ^[15]	$0.9 \times \text{NWP}^{[14]}$	-	$1.11 \times \text{NWP}^{[14]}$	ms
$t_{\text{d(SCSNH-RSTNL)}}$	delay time from SCSN HIGH to RSTN LOW	rising edge to falling edge; watchdog in window mode, triggered in the first half of the watchdog period (before $t_{\text{trig(wd)1}}$)	-	-	0.2	ms
Timer						
T_{tmr}	timer period	TnPC = 0000 (4 ms selected)	3.67	4.08	4.49	ms
		TnPC = 0001 (8 ms selected)	7.34	8.16	8.98	ms
		TnPC = 0010 (20 ms selected)	18.36	20.40	22.44	ms
		TnPC = 0011 (30 ms selected)	25.70	28.56	31.42	ms
		TnPC = 0100 (50 ms selected)	44.06	48.96	53.86	ms
		TnPC = 0101 (100 ms selected)	88.12	97.92	107.72	ms
		TnPC = 0110 (200 ms selected)	176.25	195.84	215.43	ms
		TnPC = 0111 (400 ms selected)	352.51	391.68	430.85	ms
		TnPC = 1000 (800 ms selected)	705.02	783.36	861.70	ms
		TnPC = 1001 (1 s selected)	899.64	999.6	1099.56	ms
		TnPC = 1010 (2 s selected)	1799.28	1999.2	2199.12	ms
		TnPC = 1011 (4 s selected)	3598.56	3998.4	4398.24	ms
$t_{\text{w(base)tmr}}$	timer base pulse width		86.4	96	105.6	μs

[1] L_{SMPS} and C_{SMPS} are external components needed to configure the SMPS. See [Section 7.7.4](#).

[2] Not tested in production; guaranteed by design.

[3] A persistent undervoltage/overvoltage condition will not be detected before the min time has elapsed, but will be detected, at the latest, by the time the max time has elapsed.

[4] A persistent failure will not be detected before the min time has elapsed but will be detected, at the latest, by the time the max time has elapsed.

[5] A persistent open-load recovery will not be detected before the min time has elapsed, but will be detected, at the latest, by the time the max time has elapsed.

[6] A dominant/recessive phase shorter than the min value is guaranteed not to be seen as a dominant/recessive bit; a dominant/recessive phase longer than the max value is guaranteed to be seen as a dominant/recessive bit.

[7] Time-out occurs between the min and max values. Time-out is guaranteed not to occur below the min value; time-out is guaranteed to occur above the max value.

[8] Up to 2 Mbit/s data speed.

[9] $\delta 1, \delta 3 = \frac{t_{\text{bus(rec)(min)}}}{2 \times t_{\text{bit}}}$. Variable $t_{\text{bus(rec)(min)}}$ is illustrated in the LIN timing diagram in [Figure 29](#).

[10] Bus load conditions are: $C_{\text{LIN}} = 1\text{ nF}$ and $R_{\text{LIN}} = 1\text{ k}\Omega$; $C_{\text{LIN}} = 6.8\text{ nF}$ and $R_{\text{LIN}} = 600\text{ }\Omega$; $C_{\text{LIN}} = 10\text{ nF}$ and $R_{\text{LIN}} = 500\text{ }\Omega$; see [Figure 34](#).

[11] See LIN timing diagram in [Figure 29](#).

[12] $\delta 2, \delta 4 = \frac{t_{\text{bus(rec)(max)}}}{2 \times t_{\text{bit}}}$. Variable $t_{\text{bus(rec)(max)}}$ is illustrated in the LIN timing diagram in [Figure 29](#).

- [13] A system reset will be performed if the watchdog is in Window mode and is triggered earlier than $t_{\text{trig(wd)1}}$ after the start of the watchdog period (thus in the first half of the watchdog period).
- [14] The nominal watchdog period is programmed via the NWP control bits in the Watchdog control register (Table 9); valid in watchdog Window mode only.
- [15] The watchdog will be reset if it is in window mode and is triggered after $t_{\text{trig(wd)1}}$, but not later than $t_{\text{trig(wd)2}}$, after the start of the watchdog period (thus, in the second half of the watchdog period). If the watchdog is in Timeout mode, it will be reset if it is triggered within $t_{\text{trig(wd)2}}$ after the start of the watchdog period.

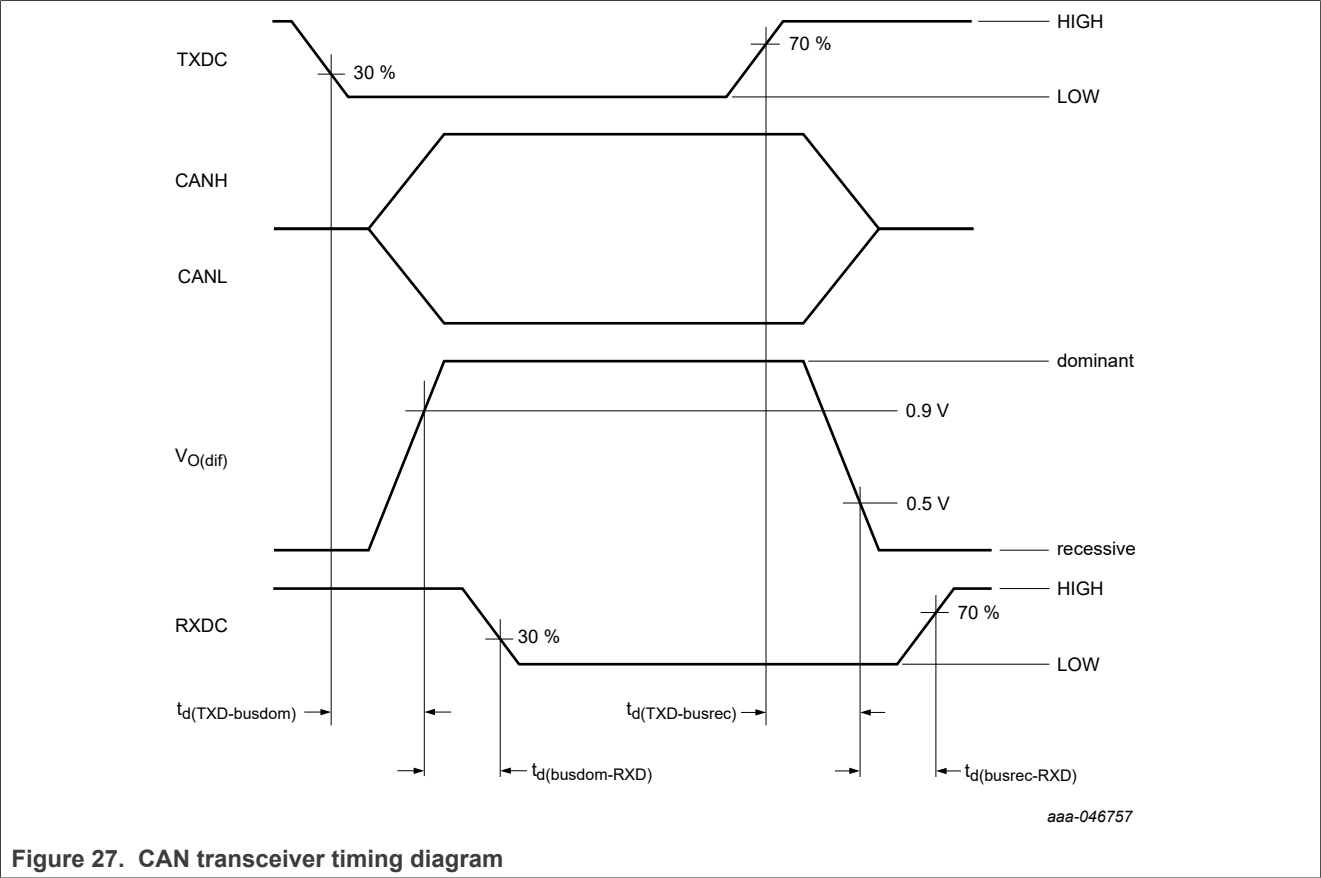
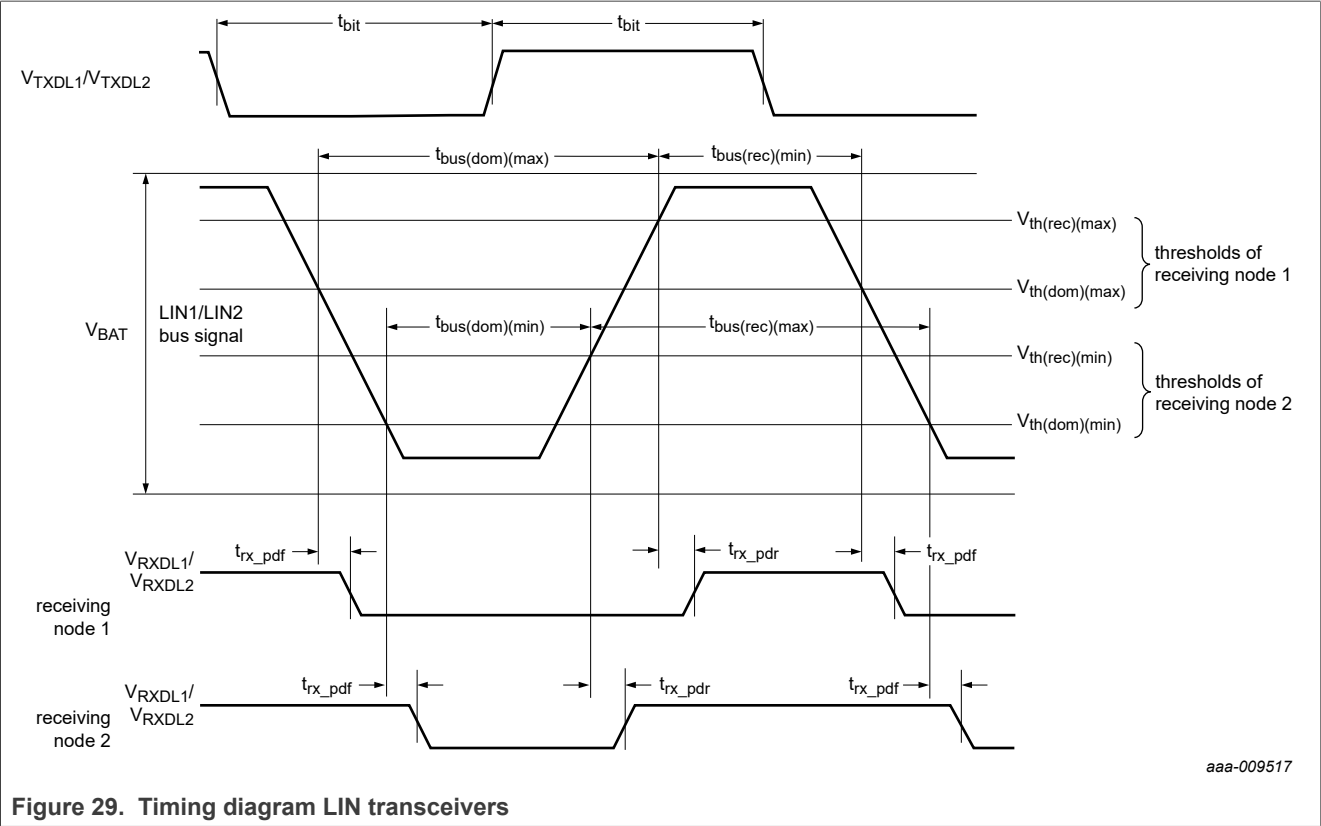
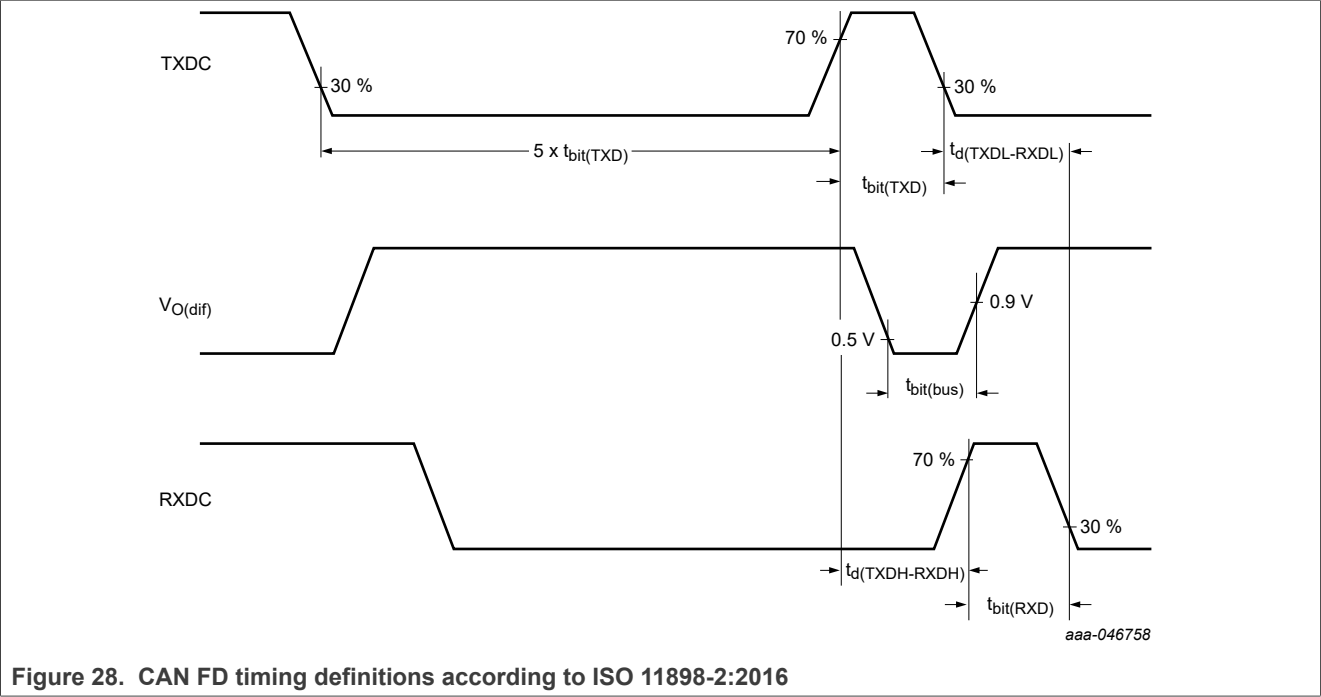
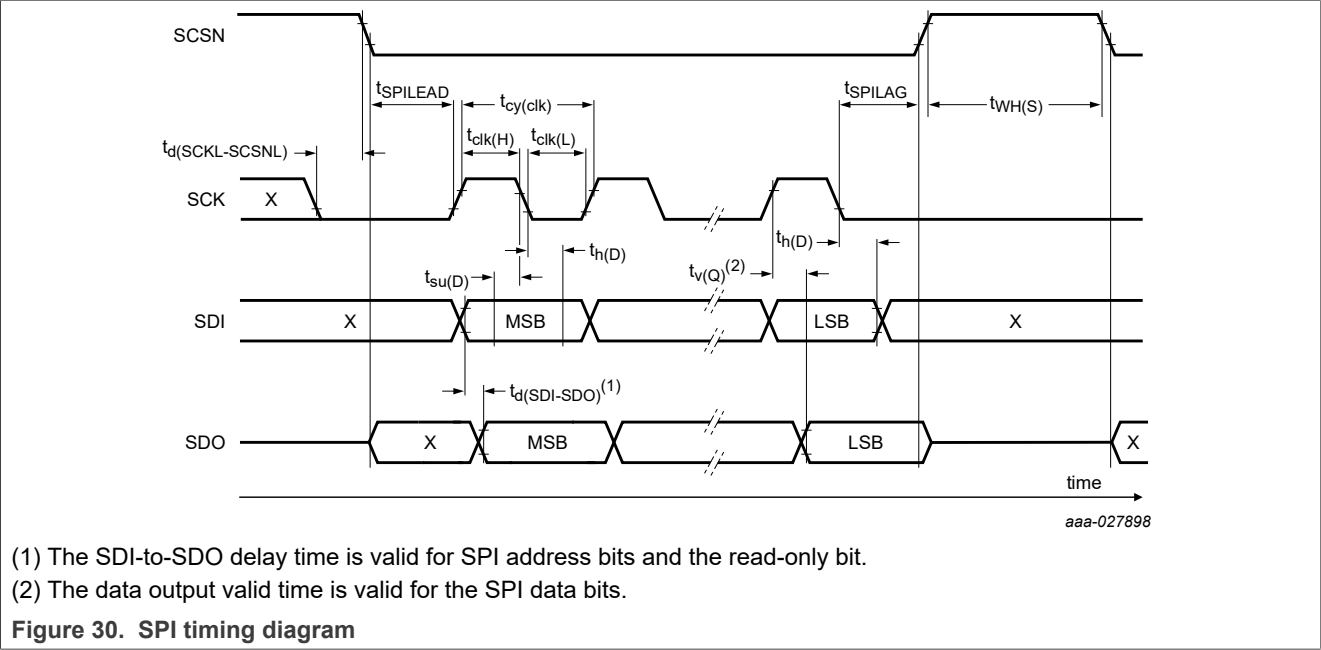


Figure 27. CAN transceiver timing diagram

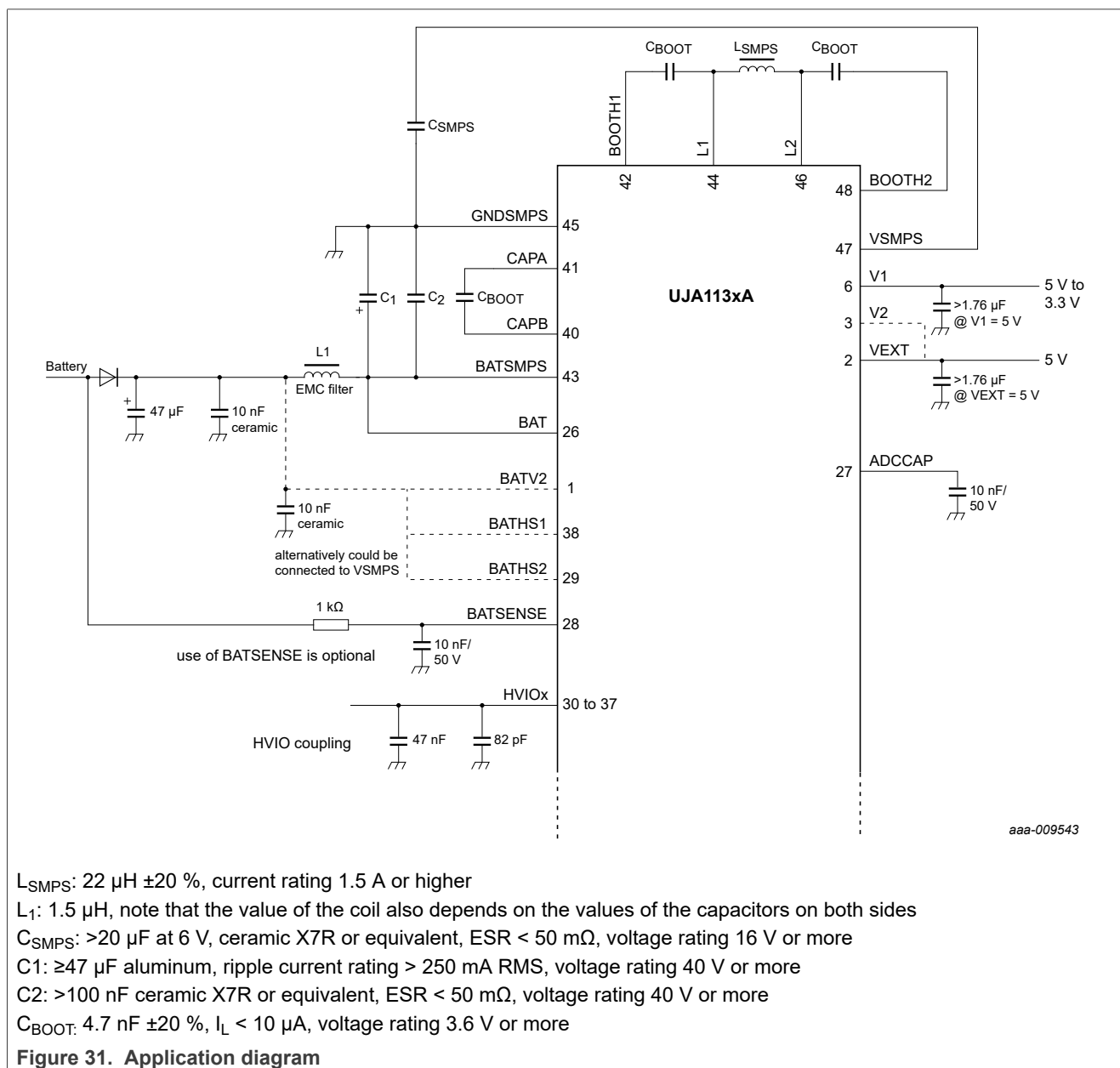




12 Application information

12.1 Application diagram

The minimum external circuitry needed for the UJA113xA is shown in [Figure 31](#). Additional information about external components and requirements on PCB layout is available in the application note (see [Section 12.2](#)).



12.2 Application note

Further information on the application of the UJA113xA series can be found in NXP application note AN13928 ‘UJA113xA series application note’.

13 Test information

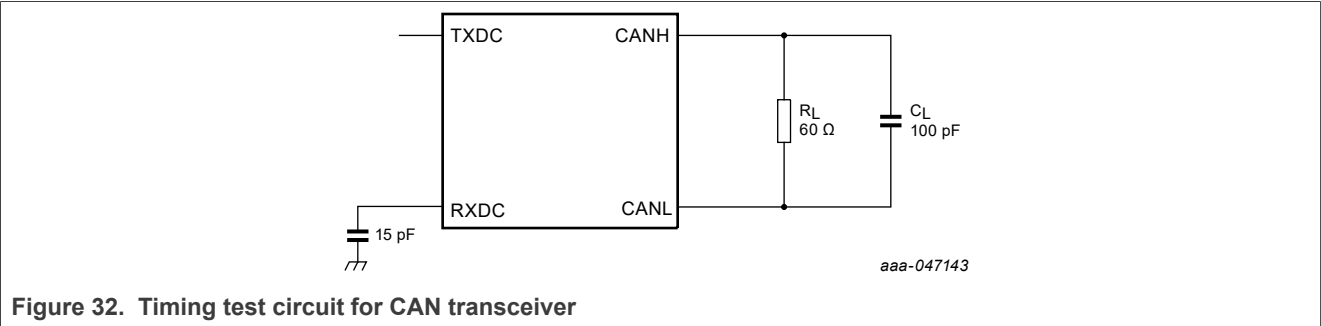


Figure 32. Timing test circuit for CAN transceiver

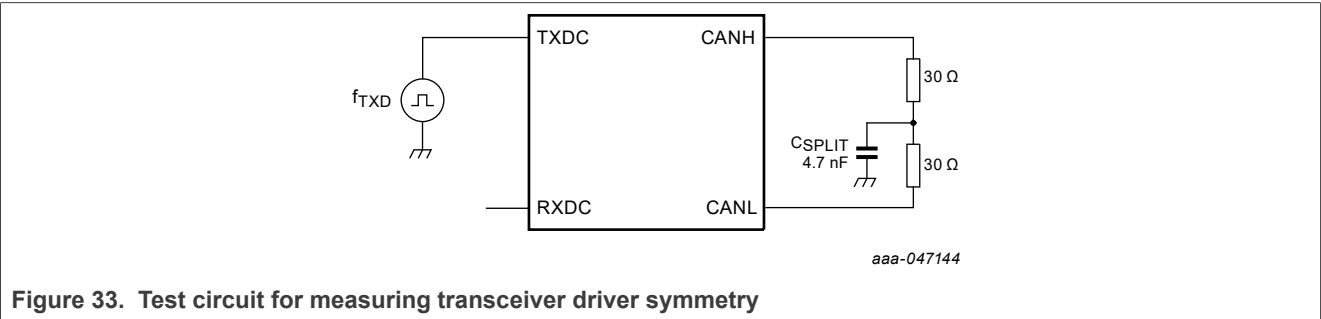


Figure 33. Test circuit for measuring transceiver driver symmetry

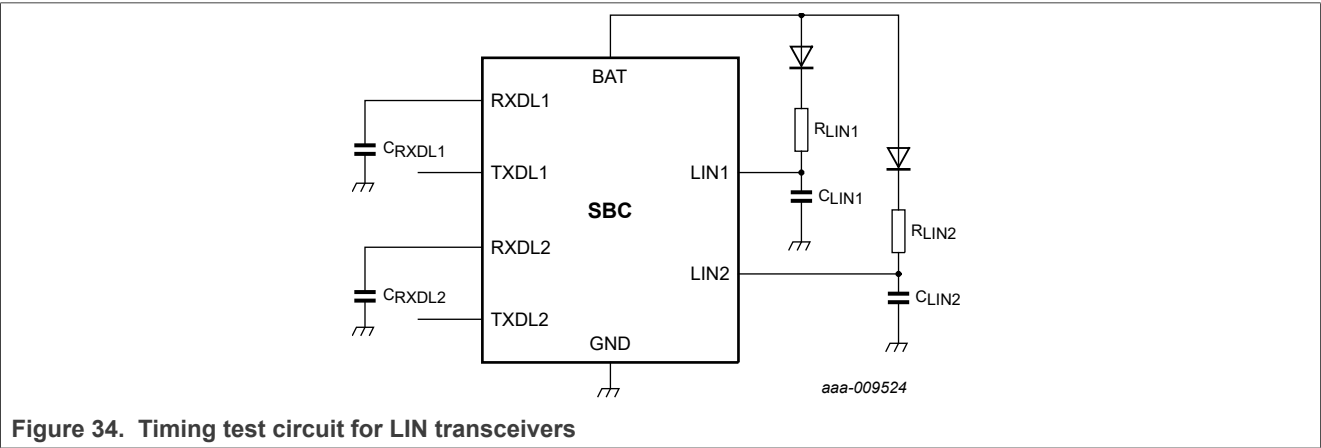


Figure 34. Timing test circuit for LIN transceivers

13.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 Rev-G - Failure mechanism based stress test qualification for integrated circuits*, and is qualified for use in road vehicles with a nominal 12 V system.

14 Package outline

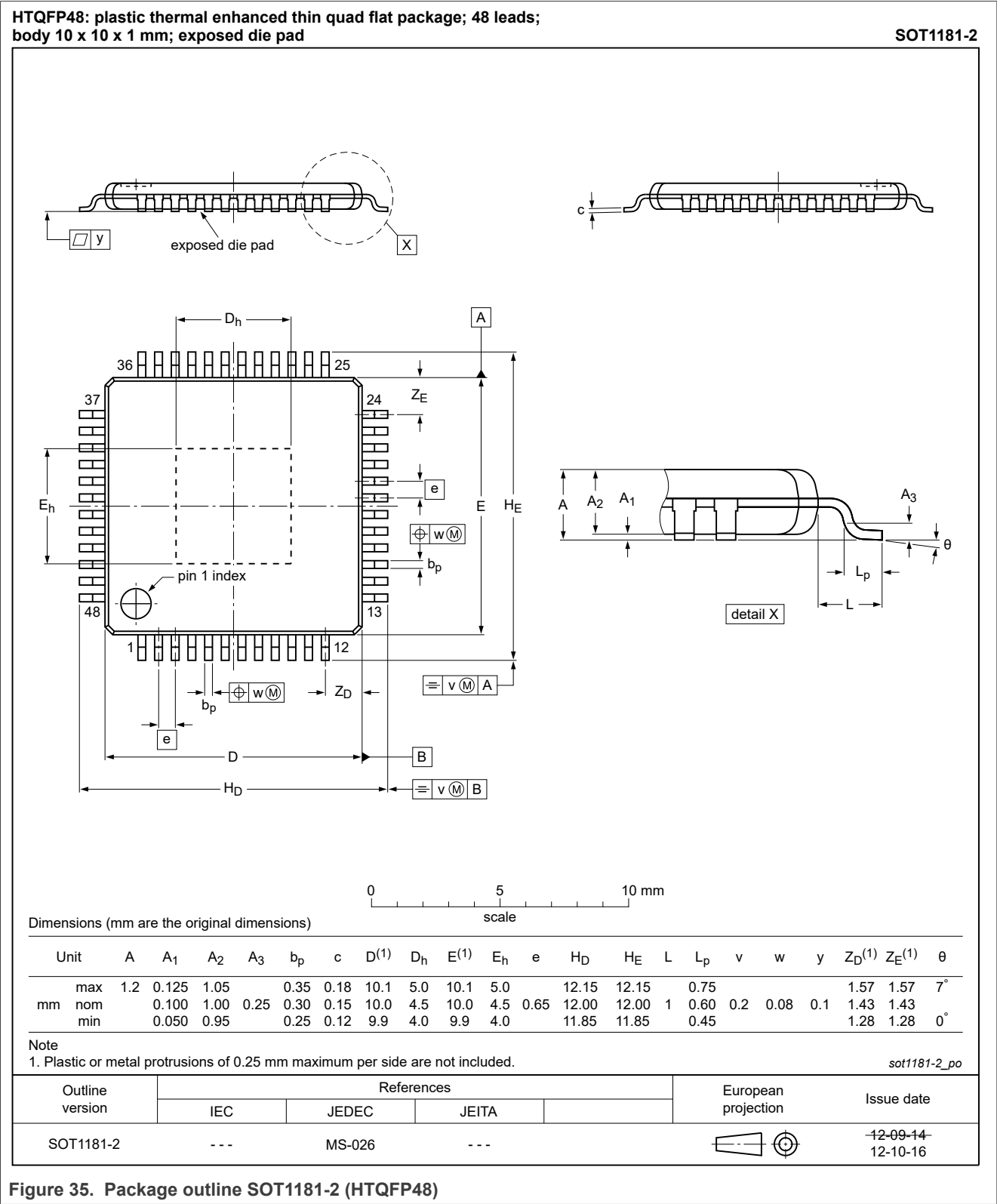


Figure 35. Package outline SOT1181-2 (HTQFP48)

15 Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

16 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 36](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 106](#) and [Table 107](#)

Table 106. SnPb eutectic process (from J-STD-020D)

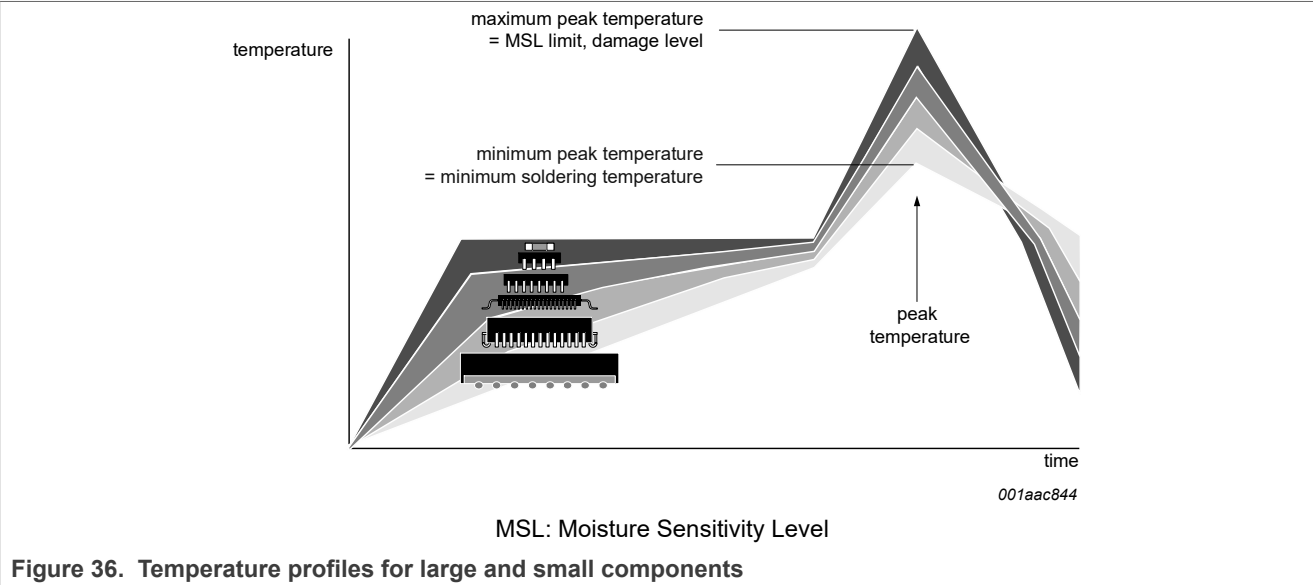
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 107. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 36](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

17 Appendix: ISO 11898-2:2016 parameter cross-reference list

Table 108. ISO 11898-2:2016 to NXP data sheet parameter conversion

ISO 11898-2:2016		NXP data sheet	
Parameter	Notation	Symbol	Parameter
HS-PMA dominant output characteristics			
Single ended voltage on CAN_H	V _{CAN_H}	V _{O(dom)}	dominant output voltage
Single ended voltage on CAN_L	V _{CAN_L}		
Differential voltage on normal bus load	V _{Diff}	V _{O(dif)}	differential output voltage
Differential voltage on effective resistance during arbitration			
Optional: Differential voltage on extended bus load range			
HS-PMA driver symmetry			
Driver symmetry	V _{SYM}	V _{TXsym}	transmitter voltage symmetry
Maximum HS-PMA driver output current			
Absolute current on CAN_H	I _{CAN_H}	I _{O(sc)dom}	dominant short-circuit output current
Absolute current on CAN_L	I _{CAN_L}		
HS-PMA recessive output characteristics, bus biasing active/inactive			
Single ended output voltage on CAN_H	V _{CAN_H}	V _{O(rec)}	recessive output voltage
Single ended output voltage on CAN_L	V _{CAN_L}		
Differential output voltage	V _{Diff}	V _{O(dif)}	differential output voltage
Optional HS-PMA transmit dominant timeout			
Transmit dominant timeout, long	t _{dom}	t _{to(dom)} TXDC	TXDC dominant time-out time
Transmit dominant timeout, short			
HS-PMA static receiver input characteristics, bus biasing active/inactive			
Recessive state differential input voltage range	V _{Diff}	V _{th(RX)dif}	differential receiver threshold voltage
Dominant state differential input voltage range		V _{rec(RX)}	receiver recessive voltage
		V _{dom(RX)}	receiver dominant voltage
HS-PMA receiver input resistance (matching)			
Differential internal resistance	R _{Diff}	R _{i(dif)}	differential input resistance
Single ended internal resistance	R _{CAN_H} R _{CAN_L}	R _i	input resistance
Matching of internal resistance	MR	ΔR _i	input resistance deviation
HS-PMA implementation loop delay requirement			
Loop delay	t _{Loop}	t _d (TXDCH-RXDCH)	delay time from TXDC HIGH to RXDC HIGH
		t _d (TXDCL-RXDCL)	delay time from TXDC LOW to RXDC LOW

Table 108. ISO 11898-2:2016 to NXP data sheet parameter conversion...continued

ISO 11898-2:2016		NXP data sheet	
Parameter	Notation	Symbol	Parameter
Optional HS-PMA implementation data signal timing requirements for use with bit rates above 1 Mbit/s up to 2 Mbit/s and above 2 Mbit/s up to 5 Mbit/s			
Transmitted recessive bit width @ 2 Mbit/s / @ 5 Mbit/s, intended	t _{Bit(Bus)}	t _{bit(bus)}	transmitted recessive bit width
Received recessive bit width @ 2 Mbit/s / @ 5 Mbit/s	t _{Bit(RXD)}	t _{bit(RXDC)}	bit time on pin RXDC
Receiver timing symmetry @ 2 Mbit/s / @ 5 Mbit/s	Δt _{Rec}	Δt _{rec}	receiver timing symmetry
HS-PMA maximum ratings of V _{CAN_H} , V _{CAN_L} and V _{Diff}			
Maximum rating V _{Diff}	V _{Diff}	V _(CANH-CANL)	voltage between pin CANH and pin CANL
General maximum rating V _{CAN_H} and V _{CAN_L}	V _{CAN_H}	V _x	voltage on pin x
Optional: Extended maximum rating VCAN_H and VCAN_L	V _{CAN_L}		
HS-PMA maximum leakage currents on CAN_H and CAN_L, unpowered			
Leakage current on CAN_H, CAN_L	I _{CAN_H} I _{CAN_L}	I _L	leakage current
Number of recessive bits before next SOF			
Number of recessive bits before a new SOF shall be accepted	n _{Bits_idle}	N _{bit(idle)}	number of idle bits
Bitfilter in CAN FD data phase			
CAN FD data phase bitfilter (option 1)	pBitfilter option1	t _{fltr(bit)dom}	dominant bit filter time
HS-PMA bus biasing control timings			
CAN activity filter time, long	t _{Filter}	t _{wake(busdom)}	bus dominant wake-up time
CAN activity filter time, short		t _{wake(busrec)}	bus recessive wake-up time
Wake-up timeout, short	t _{Wake}	t _{to(wake)bus}	bus wake-up time-out time
Wake-up timeout, long			
Timeout for bus inactivity	t _{Silence}	t _{to(silence)}	bus silence time-out time
Bus Bias reaction time	t _{Bias}	t _{d(busact-bias)}	delay time from bus active to bias

18 Revision history

Table 109. Revision history

Document ID	Release date	Description
UJA113xA_SER v.1.0	28 March 2024	• Initial version

Legal information

Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Contents

1	General description	1	7.7.4.5	Transitions to and from Pass-through mode	38
2	Features and benefits	2	7.7.4.6	Overload protection	40
2.1	General	2	7.7.5	Linear regulators	40
2.2	Integrated buck and boost converter (SMPS)	2	7.7.5.1	V1 regulator	40
2.3	Low-drop voltage regulators (LDOs)	3	7.7.5.2	Voltage regulator V2	41
2.4	CAN transceiver	3	7.7.5.3	Regulator control register	42
2.5	LIN transceivers	3	7.8	High-speed CAN transceiver	43
2.6	High-voltage I/Os (HVIOs; not available in UJA113xAHW/xF0 variants)	4	7.8.1	CAN operating modes	43
2.7	A/D converter for monitoring the battery voltage	4	7.8.1.1	CAN Active mode	44
2.8	Power management	4	7.8.1.2	CAN Listen-only mode	45
2.9	System control and diagnostic features	5	7.8.1.3	CAN Offline and Offline Bias modes	45
3	Product family overview	6	7.8.1.4	CAN Off mode	46
4	Ordering information	7	7.8.2	CAN standard wake-up (partial networking not enabled)	46
5	Block diagram	8	7.8.3	CAN partial networking (UJA113xAHW/xFx only)	47
6	Pinning information	10	7.8.3.1	Wake-up frame	47
6.1	Pinning	10	7.8.3.2	CAN FD frames	48
6.2	Pin description	10	7.8.4	Fail-safe features	49
7	Functional description	12	7.8.5	CAN transceiver control and status registers	50
7.1	System Controller	12	7.8.6	CAN partial networking configuration registers	54
7.1.1	Operating modes	12	7.9	LIN transceiver(s)	57
7.1.1.1	Off mode	12	7.9.1	LIN2.x/ISO 17987-4:2016 (12 V)/SAE J2602 compliance	57
7.1.1.2	Standby mode	12	7.9.2	LIN operating modes	57
7.1.1.3	Normal mode	13	7.9.2.1	LIN Active mode	58
7.1.1.4	Sleep mode	14	7.9.2.2	LIN Offline mode	59
7.1.1.5	Overload mode	14	7.9.2.3	LIN Listen-only mode	59
7.1.1.6	Reset mode	14	7.9.2.4	LIN Off mode	59
7.1.1.7	Forced Sleep Preparation (FSP) mode	15	7.9.3	Fail-safe features	60
7.1.1.8	Forced Normal mode	15	7.9.3.1	General fail-safe features	60
7.1.2	System control and status registers	16	7.9.3.2	TXDL dominant time-out	60
7.1.3	Exceptional start-up behavior	18	7.9.4	LIN slope control	60
7.2	Watchdog	18	7.9.5	Operation when supply voltage is outside specified operating range	60
7.2.1	Software development mode	21	7.9.6	LIN transceiver control and status registers	60
7.2.2	Watchdog behavior in Window mode	22	7.10	High-voltage input/output pins (HVIOs; not available in UJA113xAHW/xF0)	62
7.2.3	Watchdog behavior in Timeout mode	22	7.10.1	HVIO configuration	62
7.2.4	Watchdog behavior in Autonomous mode	22	7.10.1.1	HVIO slope control	63
7.3	System reset	22	7.10.2	Direct control of HVIOs (only valid for variants with 8 HVIO pins)	64
7.3.1	Characteristics of pin RSTN	24	7.10.3	Short-circuit and open load detection	64
7.3.2	Selecting the output reset pulse width	24	7.10.4	Automatic load shedding	65
7.3.3	Reset sources	25	7.10.5	Safety features	65
7.4	EN output	26	7.10.6	HVIO pins configured as limp home outputs	65
7.4.1	Fail-safe control register	26	7.10.7	HVIO control and status registers	66
7.5	Limp home function	27	7.11	Timer control	79
7.6	Global temperature protection	28	7.11.1	Timer control and status registers	81
7.7	Power supplies	28	7.12	Interrupt mechanism and wake-up function	85
7.7.1	Battery supply pins	28	7.12.1	Interrupt delay	85
7.7.2	Battery monitor	28	7.12.2	Sleep mode protection	86
7.7.3	Overvoltage shut-down	32	7.12.3	Interrupt sources	86
7.7.4	Buck and Boost converter (SMPS)	32	7.12.4	Global interrupt status register	87
7.7.4.1	SMPS parameter selection and status monitoring	32			
7.7.4.2	Automatic up/down principle	35			
7.7.4.3	Start-up and inrush currents	36			
7.7.4.4	Pass-through mode operation	36			

7.13	Non-volatile SBC configuration	89
7.13.1	Programming the MTPNV cells	89
7.13.1.1	Calculating the CRC value for MTP programming	90
7.13.2	Restoring factory preset values	91
7.14	Device ID	91
7.15	General-purpose memory	92
7.16	SPI	93
7.16.1	Introduction	93
7.16.2	Register locking	94
7.16.3	SPI control and status registers	95
7.16.4	Register map	96
8	Limiting values	101
9	Thermal characteristics	103
10	Static characteristics	103
11	Dynamic characteristics	116
12	Application information	125
12.1	Application diagram	125
12.2	Application note	125
13	Test information	126
13.1	Quality information	126
14	Package outline	127
15	Handling information	128
16	Soldering of SMD packages	128
16.1	Introduction to soldering	
16.2	Wave and reflow soldering	
16.3	Wave soldering	
16.4	Reflow soldering	
17	Appendix: ISO 11898-2:2016 parameter cross-reference list	131
18	Revision history	132
	Legal information	133