NXP Semiconductors
User's Guide

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i.MX 8M Mini Hardware Developer's Guide

1. Overview

This document aims to help hardware engineers design and test the i.MX 8M Mini series processors. It provides examples on board layout and design checklists to ensure first-pass success, and solutions to avoid board bring-up problems.

Engineers should understand board layouts and board hardware terminology.

This guide is released with relevant device-specific hardware documentation, such as datasheets, reference manuals, and application notes. All these documents are available on www.nxp.com/imx8mminievk.

1.1. Device supported

This document supports the i.MX 8M Mini (14 x 14 mm package).

Contents

1.2. Essential references

This guide is supplementary to the i.MX 8M Mini series chip reference manuals and data sheets. For reflow profile and thermal limits during soldering, see *General Soldering Temperature Process Guidelines* (document AN3300). These documents are available on www.nxp.com/i.MX8MMINI.

1.3. Supplementary references

1.3.1. General information

The following documents introduces the Arm® processor architecture and computer architecture.

- For information about the Arm Cortex®-A35 processor, see: www.arm.com/products/processors/cortex-a/cortex-a35-processor.php
- For information about the Arm Cortex-A53 processor, see: www.arm.com/products/processors/cortex-a/cortex-a53-processor.php
- For information about the Arm Cortex-A72 processor, see: www.arm.com/products/processors/cortex-a/cortex-a72-processor.php
- For information about the Arm Cortex-M4F processor, see: www.arm.com/products/processors/cortex-m/cortex-m4-processor.php
- Computer Architecture: A Quantitative Approach (Fourth Edition) - by John L. Hennessy and David A. Patterson
- Computer Organization and Design: The Hardware/Software Interface (Second Edition), by David A. Patterson and John L. Hennessy

The following documentation introduces the high-speed board design:

- Right the First Time- A Practical Handbook on High Speed PCB and System Design - Volumes I & II - Lee W. Ritchey (Speeding Edge) - ISBN 0-9741936- 0-72
- Signal and Power Integrity Simplified (2nd Edition) - Eric Bogatin (Prentice Hall)- ISBN 0-13-703502-0
- High Speed Digital Design- A Handbook of Black Magic - Howard W. Johnson & Martin Graham (Prentice Hall) - ISBN 0-13-395724-1
- High Speed Signal Propagation- Advanced Black Magic - Howard W. Johnson & Martin Graham - (Prentice Hall) - ISBN 0-13-084408-X
- High Speed Digital System Design- A handbook of Interconnect Theory and Practice - Hall, Hall and McCall (Wiley Interscience 2000) - ISBN 0-36090-2
- Signal Integrity Issues and Printed Circuit Design - Doug Brooks (Prentice Hall) ISBN 0-13-141884-X
- PCB Design for Real-World EMI Control - Bruce R. Archambeault (Kluwer Academic Publishers Group) - ISBN 1-4020-7130-2
- Digital Design for Interference Specifications - A Practical Handbook for EMI Suppression -David L. Terrell & R. Kenneth Keenan (Newnes Publishing) - ISBN 0-7506-7282-X

- Electromagnetic Compatibility Engineering - Henry Ott (1st Edition - John Wiley and Sons) - ISBN 0-471-85068-3
- Introduction to Electromagnetic Compatibility - Clayton R. Paul (John Wiley and Sons) - ISBN 978-0-470-18930-6
- Grounding & Shielding Techniques - Ralph Morrison (5th Edition - John Wiley & Sons) - ISBN 0-471-24518-6
- EMC for Product Engineers - Tim Williams (Newnes Publishing) - ISBN 0-7506- 2466-3

1.4. Related documentation

Additional literature will be published when new NXP products become available.

For the list of current documents, see www.nxp.com/i.MX8MMINI.

1.5. Conventions

Table 1 lists the notational conventions used in this document.

Table 1. Conventions used in the document

Conventions	Description
`Courier`	Used to indicate commands, command parameters, code examples, and file and directory names.
Italics	Used to indicates command or function parameters.
Bold	Function names are written in bold.
cleared/set	When a bit takes the value zero, it means to be cleared; when it takes a value of one, it means to be set.
mnemonics	Instruction mnemonics are shown in lowercase bold. Book titles in text are set in italics.
sig_name	Internal signals are written in all lowercase.
nnnn nnnnh	Denotes hexadecimal number
0b	Denotes binary number
rA, **r**B	Instruction syntax used to identify a source GPR
rD	Instruction syntax used to identify a destination GPR
REG[FIELD]	Abbreviations for registers are shown in uppercase. Specific bits, fields, or ranges appear in brackets. For example, MSR[LE] refers to the little-endian mode enable bit in the machine state register.
x	An italicized *x* indicates an alphanumeric variable.
n, *m*	An italicized *n* indicates a numeric variable.

In this guide, notation for all logical, bit-wise, arithmetic, comparison, and assignment operations follow C Language conventions.

1.6. Acronyms and abbreviations

Table 2 defines the acronyms and abbreviations used in this document.

Table 2. Definitions and acronyms

Acronym	Definition
ARM	Advanced RISC Machines processor architecture
BGA	Ball Grid Array package
BOM	Bill of Materials
BSDL	Boundary Scan Description Language
CAN	Flexible Controller Area Network peripheral
CCM	Clock Controller Module
CSI	MIPI Camera Serial Interface
DDR	Dual Data Rate DRAM
DDR3L	Low voltage DDR3 DRAM
DDR4	DDR4 DRAM
DDRC	DDR Controller
DFP	Downstream Facing Port (USB Type-C)
DRP	Dual Role Port (USB Type-C)
ECSPI	Enhanced Configurable SPI peripheral
EIM	External Interface Module
ENET	10/100/1000 Mbps Ethernet MAC peripheral
EPIT	Enhanced Periodic Interrupt Timer peripheral
ESR	Equivalent Series Resistance
GND	Ground
GPC	General Power Controller
GPIO	General Purpose Input/Output
HDCP	High-bandwidth Digital Content Protection
I^2C	Inter-integrated Circuit interface
IBIS	Input output Buffer Information Specification
IOMUX	i.MX 8M Mini chip-level I/O multiplexing
JTAG	Joint Test Action Group
KPP	Keypad Port Peripheral
LDB	LVDS Display Bridge
LDO	Low Drop-Out regulator
LPCG	Low Power Clock Gating
LPDDR4	Low Power DDR4 DRAM
LVDS	Low-Voltage Differential Signaling
MLB	Media Local Bus
ODT	On-Die Termination
OTP	One-Time Programmable
PCB	Printed Circuit Board
PCIe	PCI Express
PCISig	Peripheral Component Interconnect Special Interest Group
PDN	Power Distribution Network
PMIC	Power Management Integrated Circuit
POR	Power-On Reset
PTH	Plated Through Hole PCB (i.e. no microvias)
RGMII	Reduced Gigabit Media Independent Interface (Ethernet)
RMII	Reduced Media Independent Interface (Ethernet)
ROM	Read-Only Memory

2. i.MX 8M Mini design checklist

This document provides a design checklist for the i.MX 8M Mini (14 x 14 mm package) processor. The design checklist tables recommend optimal design and provide explanations to help users understand better. All supplemental tables referenced by the checklist appear in sections following the design checklist tables.

2.1. Design checklist table

Table 3. LPDDR4 recommendations (i.MX 8M Mini)

Check box	Recommendations	Explanation/Supplemental recommendations
	1. Connect the DRAM_ZN ball on the processor (ball P2) to a 240 Ω, 1% resistor to GND.	This is a reference used during DRAM output buffer driver calibration.
	2. The ZQ0 and ZQ1 balls on the LPDDR4 device should be connected through 240Ω, 1% resistors to the LPDDR4 VDD2 rail.	—
	3. Place a 10 kΩ, 5% resistor to ground on the DRAM reset signal.	This will ensure adherence to the JEDEC specification until the control is configured and starts driving the DDR.
	4. The ODT_CA balls on the LPDDR4 device should be connected directly or through a 10 kΩ resistor to the LPDDR4 VDD2 rail.	LPDDR4 ODT on the i.MX 8M Mini is command-based, making processor ODT_CA output balls unnecessary.
	5. The architecture for each chip inside the DRAM package must be x 16.	The processor does not support byte mode specified in JESD209-4B.
	6. The processor ball MTEST (ball N2), should be left unconnected.	These are observability ports for manufacturing and are not used otherwise.
	7. The VREF pin on the processor (ball P1) can be left unconnected.	The VREF signal for LPDDR4 is generated internally by the processor.
	8. If 16bit LPDDR4 memory device is used, the signals should only be connected to channel A of I.MX8M Mini DDR controller, the reference design of 8MMINILPD4- EVK can't be used.	On 8MMINILPD4- EVK, 32bit LPDDR4 Memory Channel A/B are swapped for easier signal routing.

Table 4. DDR4/DDR3L recommendations (i.MX 8M Mini)

Check box	Recommendations	Explanation/Supplemental recommendations
	1. Connect the ZQ(DRAM_ZN) ball on the processor (ball P2) to individual 240 Ω, 1% resistors to GND.	This is a reference used during DRAM output buffer driver calibration.
	2. The ZQ ball on each DDR4/DDR3L device should be connected through individual 240 Ω, 1% resistors to GND.	—
	3. Place a 10 kΩ, 5% resistor to ground on the DRAM reset signal.	This will ensure adherence to the JEDEC specification until the control is configured and starts driving the DDR.
	4. The processor ball MTEST (ball N2), should be left unconnected.	These are observability ports for manufacturing and are not used otherwise.

Table 5. GPIO recommendations

Check box	Recommendations	Explanation/Supplemental recommendations
	1. Use external resistors in 3.3V mode, if pull up/down is needed.	IO internal pull up/down is not supported in 3.3V mode. Users need to disable the internal pull up/down through software and use external pull up/down resistors instead. All IO pin groups are impacted except for XTAL, DDR, PCI, USB, and MIPI PHY IO's. See Errata e50080 for detailed information.
	2. Disable internal pull up/down by software.	Disable the internal pull up/down by setting PAD Control register PE bit (Pull Resistors Enable Field) to **0**. For example, disable this bit in initialization code or DTB under Linux OS.

Table 6. I^2C recommendations

Check box	Recommendations	Explanation/Supplemental recommendations
	3. Verify the target I^2C interface clock rates	The I^2C bus can only be operated as fast as the slowest peripheral on the bus. If faster operation is required, move the slow devices to another I^2C port.
	4. Verify that there are no I^2C address conflicts on any of the I^2C buses utilized	There are multiple I^2C ports available on chip, so if a conflict exists, move one of the conflicting devices to a different I^2C bus. If it is impossible, use a I^2C bus switch (NXP part number PCA9646).
	5. Do not place more than one set of pull-up resistors on the I^2C lines.	This could result in excessive loading and potential incorrect operation. Choose the pull-up value commensurate with the bus speed being used.
	6. Ensure that the VCC rail powering the i.MX 8M Mini I^2C interface balls matches the supply voltage used for the pull-up resistors and the slave I^2C devices.	Prevent device damage or incorrect operation due to voltage mismatch.

Table 7. JTAG recommendations

Check box	Recommendations	Explanation/Supplemental recommendations
	1. Do not use external pullup or pulldown resistors on JTAG_TDO.	JTAG_TDO is configured with an on-chip keeper circuit and the floating condition is actively eliminated.
	2. Follow the recommendations for external pull-up and pull-down resistors given in Table 16.	—
	3. For normal operation, TEST_MODE (ball D26) should be pulled down using a 100KOhm resistor. To enter boundary-scan mode, this pin should be pulled up to NVCC_JTAG using a 4.7KOhm resistor. Please reference "COMPLIANCE_PATTERNS" in the chip BSDL file.	—
	4. JTAG_MOD should be connected to ground through a resistor.	—

Table 8. Reset and ON/OFF recommendations

Check box	Recommendations	Explanation/Supplemental recommendations
	1. The POR_B input must be asserted at powered up and remain asserted until the last power rail for devices required for system boot are at their working voltage. This functionality is controlled by the PMIC (BD71847MWV) on EVK.	POR_B is driven by the PMIC. If a reset button is used, it should be connected to the PWRON_B pin of the PMIC instead of directly connected to POR_B pin of the CPU. When POR_B is asserted (low) on the i.MX 8M Mini, the output PMIC_ON_REQ remains asserted (high).
	2. For portable applications, the ONOFF pin may be connected to an ON/OFF SPST push-button switch to ground. An external pull-up resistor is required on this pin.	A brief connection to GND in OFF mode causes the internal power management state machine to change state to ON. In ON mode, a brief connection to GND generates an interrupt (intended to initiate a software-controllable power-down). The connection to GND for approximate 5 seconds or more causes a forced OFF.
	3. Connect GPIO1_IO02(WDOG_B, ball AG13) to external PMIC or reset IC to repower the system except SNVS is strongly recommended.	i.MX8M Mini can't be reset by internal reset source in idle mode, repower is preferred. Some peripherals like SD3.0, QSPI also need repower during system reset.
	4. GPIO1_IO02(WDOG_B, ball AG13) is used as Cold Reset, external pull up resistor (100Kohm) is needed to support boundary-scan mode.	In boundary scan mode, WDOG_B is floating. Without the external 100Kohm pull up, WDOG_B will repeatedly reset 8MMINILPD4-EVK when entering boundary-scan mode.

Table 9. PCIe recommendations

Check box	Recommendations	Explanation/Supplemental recommendations
	1. Use an appropriate external PCIe reference clock generator.	The NXP EVK board design uses an IDT 9FGV0241 device. However, NXP does not recommend one supplier over another, and does not suggest that this is the only clock generator supplier. The device used should support all the specs (jitter, accuracy, etc.).
	2. The differential transmitters from the processor must be AC coupled. It is recommended to use a 0.1 µF cap on both the PCIE_TXP and PCIE_TXN outputs.	PCIe specification compliance requires AC coupling at each transmitter. The receiver must be DC coupled.
	3. The PCIEx_RESREF ball (ball D19) should be connected to the ground through a 8.2 K Ω, 1% resistor.	—

Table 10. USB recommendations

Check box	Recommendations	Explanation/Supplemental recommendations
	1. Connect a 200 Ω, 1% resistor to the ground on the USBx_TXRTUNE ball (ball E19 and E22).	—
	2. Route all USB differential signals with 90 Ω differential impedance.	—
	3. ESD protection should be implemented at the connector pins. Choose a low capacitance device recommended for high-speed interfaces.	This will prevent potential damages to board components from ESD.

Table 11. FlexSPI recommendations

Check box	Recommendations	Explanation/Supplemental recommendations
	1. Read strobe(DQS) pad should be floated or with a 10-18pF cap load to compensate SIO/SCK pins load for high speed running, if the memory device doesn't provide DQS.	There are three modes for the internal sample clock for FlexSPI read data: Dummy read strobe generated by FlexSPI controller and looped back internally(FlexSPIn_MCR0[RXCLKSRC] = 0x0), can only reach 66Mhz operation frequency; Dummy read strobe generated by FlexSPI controller and looped back through the DQS pad(FlexSPIn_MCR0[RXCLKSRC] = 0x1), can reach 133Mhz operation frequency. In this mode, this pin can be floated or put some cap loads on board level to compensate SIO/SCK pins load; Read strobe provided by memory device and input from DQS pad(FlexSPIn_MCR0[RXCLKSRC] = 0x3), can reach 133Mhz operation frequency.

Table 12. Oscillator/Crystal recommendations

Check box	Recommendations	Explanation/Supplemental recommendations
	1. Connect a 24 MHz crystal and a 510K Ω resistor between 24M_XTALI and 24M_XTALO (balls B27 and C26).	This crystal should have ESR not greater than 80 Ω, and be rated for a drive level of at least 180 µW. Follow the manufacturer's recommendation for loading capacitance. Use short traces between the crystal and the processor, with a ground plane under the crystal, load capacitors, and associated traces.
	2. Use the 32.768 kHz clock generated by the PMIC (BD71847MWV) to drive the i.MX 8M Mini RTC_XTALI input (ball A26), and connect RTC_XTALO (ball B25) to VDD_SNVS_0P8.	The voltage level of this driving clock should not exceed the voltage of the NVCC_SNVS rail, or the damage/malfunction may occur. The RTC signal should not be driven if the NVCC_SNVS supply is OFF. It can lead to damage or malfunction. For RTC V_{IL} and V_{IH} voltage levels, see the latest i.MX 8M Mini datasheet available at www.nxp.com/i.MX8MMINI.

Table 13. i.MX 8M Mini power/decoupling recommendations

Check box	Recommendations	Explanation/Supplemental recommendations
	1. Comply with the power-up sequence guidelines as described in the datasheet to guarantee reliable operations of the device.	Any deviation from these sequences may result in the following situations: • Excessive current during power-up phase • Prevention of the device from booting • Irreversible damage to the processor (worst case)
	2. Maximum ripple voltage requirements	Common requirement for ripple noise peak-to-peak value should be less than 5% of the supply voltage nominal value.
	3. If using BD71847MWV PMIC to provide power, make sure all the regulators except LDO5 have output L/C components properly connected, even if unused.	Leaving any regulator except LDO5 output open will lead to malfunction of the whole PMIC.

Table 14. Decoupling capacitors recommendations (i.MX 8M Mini)

Checkbox	Supply	2.2 nF	0.22 µF	1 µF	4.7 µF	10 µF	Notes
	VDD_DRAM, VDD_VPU, VDD_GPU, VDD_DRAM_PLL_0P8	—	—	6	—	2	These 4 power rails are combined together on EVK
	NVCC_DRAM	—	—	6	—	2	—
	VDD_ARM	—	—	5	—	1	—
	VDD_SOC	—	—	5	—	1	—
	VDD_SNVS_0P8	—	1	—	—	—	—
	NVCC_SNVS_1P8	—	—	1	—	—	—
	VDD_24M_XTAL_1P8	—	1	—	—	—	—
	VDD_DRAM_PLL_1P8	—	—	1	—	—	—
	PVCC_1P8	—	2	—	—	—	—
	VDD_ARM_PLL_1P8, VDD_ANA0_1P8, VDD_ANA1_1P8, VDD_USB_1P8, VDD_PCI_1P8, VDD_MIPI_1P8	—	4	—	—	1	—
	NVCC_NAND, NVCC_SAI1, NVCC_SAI3, NVCC_SAI5, NVCC_ECSPI, VDD_USB_3P3	—	5	—	1	—	—
	NVCC_JTAG, NVCC_SAI2, NVCC_GPIO1, NVCC_I2C, NVCC_UART, NVCC_SD1, NVCC_CLK	—	3	—	—	1	—
	NVCC_SD2	—	1	—	—	—	—
	NVCC_ENET	—	1	—	—	—	—
	VDD_ARM_PLL_0P8, VDD_ANA_0P8, VDD_USB_0P8, VDD_PCI_0P8	—	1	—	1	—	—
	VDD_MIPI_1P2	—	1	—	—	—	—
	VDD_MIPI_0P9	—	1	—	—	—	—
	MIPI_VREG_CAP	1	—	—	—	—	—
	Capacitor part number used on EVK: • 2.2 nF --- GRM033R71C222KA88D • 0.22 µF --- LMK063BJ224MP-F • 1 µF --- 02016D105MAT2A • 4.7 µF --- CL05A475KP5NRNC • 10 µF --- ZRB15XR60J106ME12D						

Table 15. PCB design recommendations

Check box	Recommendations	Explanation/Supplemental recommendations
	1. High-speed signal traces have reference plane in adjacent layer and are impedance controlled.	Controlled impedance is the key factor to have good signal integrity. Note that the reference plane can only be GND or the signal's own I/O power. Do not use other nets as reference.
	2. High-speed signal traces never cross gap or slot in reference plane.	Crossing gap in reference plane will cause reflection and increase crosstalk.
	3. Place at least one GND stitching via within 50 mils of signal via when switching reference planes.	GND stitching via can help keep impedance continuous and reduce via crosstalk.
	4. Appropriate delay matching is done for parallel bus.	Signals within a bus should have delay time matched to maintain timing margin.
	5. The true and complementary signal of a differential pair must have delay matched to within 1ps.	The true and complementary signal within a differential pair should have delay time tightly matched.
	6. DDR interface passed SI simulation. Alternatively, directly copy the EVK DDR layout design.	Generally, SI simulation should be performed for DDR interface that runs at 3000 MT/s to ensure stable working. If this is not feasible, just copy the EVK DDR layout design as well as the board stack-up.
	7. Place test point on key signals to ease debugging. When placing test point on high-speed signal traces, make sure its diameter is no more than 20mil and the test point be directly placed on the trace with no stub.	Test points can bring excessive capacitance and should be carefully handled on high-speed signal traces.
	8. Decoupling capacitors are placed as close to IC power pins as possible.	This is to reduce the inductance from decoupling capacitor to IC power pin, to improve decoupling effectiveness.

2.2. JTAG signal termination

Table 16 is a JTAG termination chart showing what terminations should be placed on PCB designs.

Table 16. Recommended JTAG board terminations

JTAG signal	I/O type	External termination	Comments
JTAG_TCK	Input	10 kΩ pull-down	—
JTAG_TMS	Input	None	Internal pulled up to NVCC_JTAG, no external termination required
JTAG_TDI	Input	None	Internal pulled up to NVCC_JTAG, no external termination required
JTAG_TDO	3-state output	None	—
JTAG_TRSTB	Input	None	No connection from JTAG to processor, internal pulled up to NVCC_JTAG

2.3. Signal termination for Boundary-scan

Table 17 is a signal termination chart showing what terminations should be placed on board designs to support Boundary-scan.

Table 17. Recommended board terminations for Boundary-scan

Signal	I/O type	External termination	Comments
BOOT_MODE0	Input	Pull Up	BOOT_MODE0, BOOT_MODE1, JTAG_MOD, TEST_MODE must be at 1101 to enter Boundary-scan mode.
BOOT_MODE1	Input	Pull Up	
JTAG_MOD	Input	Pull Down	
TEST_MODE	Input	Pull Up	
GPIO1_IO02 (WDOG_B)	Input	Pull Up	External pull up resistor (100Kohm) is needed to support boundary-scan mode.

3. i.MX 8M Mini layout/routing recommendations

3.1. Introduction

This chapter describes how to assist design engineers with the layout of an i.MX 8M Mini-based system.

3.2. Basic design recommendations

When using the Allegro design tool, the schematic symbol & PCB footprint created by NXP is recommended. When not using the Allegro tool, use the Allegro footprint export feature (supported by many tools). If the export is not possible, create the footprint per the package dimensions outlined in the product data sheet.

Native Allegro layout and gerber files are available on www.nxp.com/imx8mminievk.

3.2.1. Placing decoupling capacitors

Place small decoupling and larger bulk capacitors on the bottom side of the PCB.

The 0201 or 0402 decoupling and 0603 or larger bulk capacitors should be mounted as close as possible to the power vias. The distance should be less than 50 mils. Additional bulk capacitors can be placed near the edge of the BGA via array. Placing the decoupling capacitors close to the power balls is critical to minimize inductance and ensure high-speed transient current required by the processor. See the i.MX 8M Mini EVK layouts for examples of the desired decoupling capacitor placement.

The following list describes how to choose correct decoupling scheme:

- Place the largest capacitance in the smallest package that budget and manufacturing can support.
- For high-speed bypassing, select the required capacitance with the smallest package (for example, 0.1 μF, 0.22 μF, 1.0 μF, or even 2.2 μF in a 0201 package size).
- Minimize trace length (inductance) to small caps.
- Series inductance cancels out capacitance.
- Tie caps to GND plane directly with a via.
- Place capacitors close to the power ball of the associated package from the schematic.
- A preferred BGA power decoupling design is available on the EVK board design available on www.nxp.com/imx8mminievk. Customers should use the NXP design strategy for power and decoupling.

3.3. Stack-up and manufacturing recommendations

3.3.1. Stack-up recommendation (i.MX 8M Mini)

Due to the number of balls on the i.MX 8M Mini processor in the 14 mm x 14 mm package, a minimum 8-layer PCB stack-up is recommended. For the 8-layers on the PCB, a sufficient number of layers need to be dedicated to power on routing to meet the IR drop target of 2% for the i.MX 8M Mini CPU power rails.

The constraints for the trace width will depend on such factors as the board stack-up and associated dielectric and copper thickness, required impedance, and required current (for power traces). The stack-up also determines the constraints for routing and spacing. Consider the following requirements when designing the stack-up and selecting board material:

- Board stack-up is critical for high-speed signal quality.
- Preplanning impedance of critical traces is required.
- High-speed signals must have reference planes on adjacent layers to minimize cross-talk.
- PCB material: the material used on EVK is TU768.

3.3.2. Manufacturing recommendation (i.MX 8M Mini)

Since the i.MX 8M Mini processor uses 0.5mm-pitch BGA package, the PCB technology must meet below requirement to fully fanout all the signals of the processor using PTH(plated through holes).

- Minimum trace width: 3.2mil
- Minimum trace to trace/pad spacing: 3.2mil
- Minimum via size: 8mil-diameter hole, 16mil-diameter pad
- Minimum via pad to pad spacing: 4mil

Figure 1 shows the reference routing of the i.MX 8M Mini, PTH is ok for the fanout, HDI is not needed.

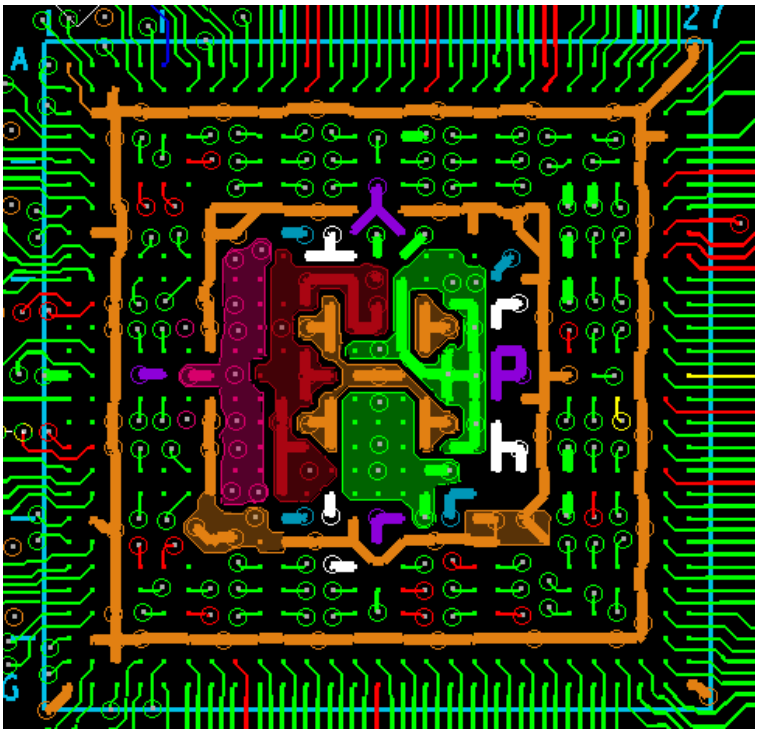

Figure 1. i.MX 8M Mini fanout routing on EVK

3.3.3. EVK PCB stack-up (i.MX 8M Mini)

Table 18 and Table 19 show stack-up of the EVK. Both the CPU board and the BB board use 8-layer stack-up.

Table 18. 8MMINILPD4-CPU Board stack up information

Layer	Description	Coppoer (Oz.)	Dielectric thickness (mil)
1	Signal	0.333+Plating	
	Dielectric		2.611 mil
2	GND	1	
	Dielectric		3.94 mil
3	Signal	0.5	
	Dielectric		3.7 mil
4	GND	1	
	Dielectric		16.14 mil

Table 18. 8MMINILPD4-CPU Board stack up information

Layer	Description	Coppoer (Oz.)	Dielectric thickness (mil)
5	Power	1	
	Dielectric		3.805 mil
6	Power	0.5	
	Dielectric		3.94 mil
7	GND	1	
	Dielectric		2.611 mil
8	Signal	0.333+Plating	
Finished:	47.244(4.724/-4.724) mil		1.2(+0.12/-0.12) MM
Designed:	43.858 mil		1.114 MM
Material:	TU768		TU768

Table 19. 8MMINI-BB Board stack up information

Layer	Description	Coppoer (Oz.)	Dielectric thickness (mil)
1	Signal	0.5+Plating	
	Dielectric		2.717 mil
2	GND	1	
	Dielectric		4.33 mil
3	Signal	1	
	Dielectric		11.085 mil
4	Power	1	
	Dielectric		14.170 mil
5	Power	1	
	Dielectric		11.415 mil
6	Signal	1	
	Dielectric		4.33 mil
7	GND	1	
	Dielectric		2.717 mil
8	Signal	0.5+Plating	
Finished:	62.992(6.299/-6.299) mil		1.6(+0.16/-0.16) MM
Designed:	59.173 mil		1.503 MM
Material:	TU768		TU768

3.4. DDR design recommendations

3.4.1. DDR connection information

The i.MX 8M Mini processor can be used with LPDDR4, DDR4 or DDR3L memory. Since these memory types have different I/O signals, there are 38 generically-named functional balls, depending on the type of memory used. See Table 20 for the connectivity of these generic balls for DDR3L, LPDDR4 and DDR4. The schematic symbol created by NXP already replaced these generic names with DDR function.

Table 20. DDR3L/LPDDR4/DDR4 connectivity

Ball name	Ball #	LPDDR4 function	DDR4 function	DDR3L function
DRAM_AC00	F4	CKE0_A	CKE0	CKE0
DRAM_AC01	F5	CKE1_A	CKE1	CKE1
DRAM_AC02	K4	CS0_A	CS0_n	CS0#
DRAM_AC03	J4	CS1_A	C0	-
DRAM_AC04	L2	CK_t_A	BG0	BA2
DRAM_AC05	L1	CK_c_A	BG1	A14
DRAM_AC06	F6	-	ACT_n	A15
DRAM_AC07	J5	-	A9	A9
DRAM_AC08	J6	CA0_A	A12	A12/BC#
DRAM_AC09	K6	CA1_A	A11	A11
DRAM_AC10	E4	CA2_A	A7	A7
DRAM_AC11	D5	CA3_A	A8	A8
DRAM_AC12	N4	CA4_A	A6	A6
DRAM_AC13	N5	CA5_A	A5	A5
DRAM_AC14	K5	-	A4	A4
DRAM_AC15	N6	-	A3	A3
DRAM_AC16	M1	-	CK_t_A	CK_A
DRAM_AC17	M2	-	CK_c_A	CK#_A
DRAM_AC19	N2	MTEST	MTEST	MTEST
DRAM_AC20	AB4	CKE0_B	CK_t_B	CK_B
DRAM_AC21	AB5	CKE1_B	CK_c_B	CK#_B
DRAM_AC22	W4	CS1_B	-	-
DRAM_AC23	V4	CS0_B	-	-
DRAM_AC24	U2	CK_t_B	A2	A2
DRAM_AC25	U1	CK_c_B	A1	A1
DRAM_AC26	N1	-	BA1	BA1
DRAM_AC27	R6	-	PARITY	-
DRAM_AC28	W6	CA0_B	A13	A13
DRAM_AC29	V6	CA1_B	BA0	BA0
DRAM_AC30	AC4	CA2_B	A10 / AP	A10 / AP
DRAM_AC31	AD5	CA3_B	A0	A0
DRAM_AC32	R4	CA4_B	C2	-
DRAM_AC33	R5	CA5_B	CAS_n / A15	CAS#
DRAM_AC34	T1	-	WE_n / A14	WE#
DRAM_AC35	T2	-	RAS_n / A16	RAS#
DRAM_AC36	V5	-	ODT0	ODT0
DRAM_AC37	W5	-	ODT1	ODT1
DRAM_AC38	AB6	-	CS1_n	CS1#

3.4.2. LPDDR4-3000 design recommendations

The following list provides some generic guidelines that should be adhered to when implementing an i.MX 8M Mini design using LPDDR4.

1. It is expected that the layout engineer and design team already has experience and training with DDR designs at speeds of 1.5 GHz / 3000 MT/s.
2. Refer to solid GND plane only for all the high-speed signal traces.
3. Keep edge to edge spacing of high-speed signal traces no less than 2 times the trace width to minimize trace crosstalk.
4. At a speed of 3000 MT/s, signal vias can be a significant source of crosstalk. If not properly designed, it can introduce crosstalk larger than that from the trace. To minimize via crosstalk, make sure the total number of vias to be two or less on each point-to-point single-ended/differential trace. Place at least one ground stitching via within 50 mils of signal via when switching reference planes to provide continuous return path and reduce crosstalk. If it is not possible to place enough ground stitching vias due to space limitation, try to make the length that the signal actually travels on the via as short as possible, as illustrated in Figure 2.

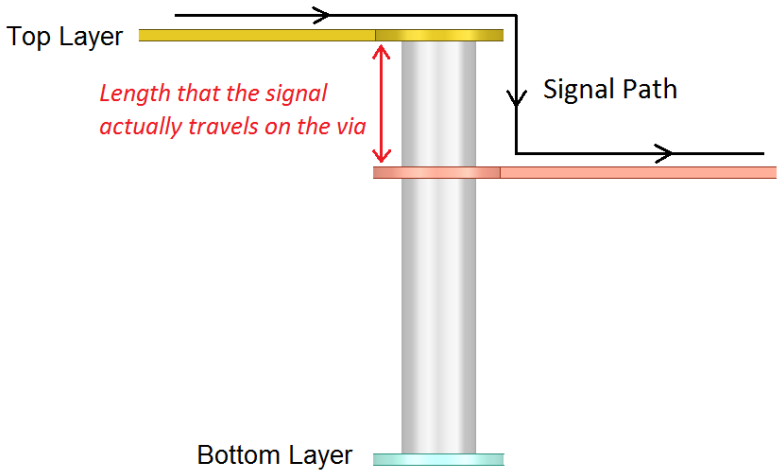

Figure 2. Length that the signal actually travels on the Via

5. CLK and DQS signal can be routed on different layer with DQ/CA signals to ease routing. When doing this, keep no less than 5 times trace width spacing from other signals.
6. Use time delay instead of length when performing the delay matching. The delay matching includes the PCB trace delay and the IC package delay. Incorporate the package pin delay into the CAD tool's constraint manager.
7. Include the delay of vias when performing delay matching. This can be realized in Allegro tool by enabling the **Z Axis Delay** in "Setup -> Constraints -> Modes".
8. Byte swapping within each 16-bit channel is OK. Bit swapping within each slice/byte lane is OK.
9. Bit swapping of Command/Address (CA[5:0]) signals is **NOT** allowed.

10. i.MX 8M Mini does not drive ODT_CA signal. The ODT_CA balls on the LPDDR4 devices should be connected directly or through a resistor to the VDD2 supply.
11. In general, the 200-ball LPDDR4 package should be placed 200 mils from the i.MX 8M Mini.
12. Enable the DBI (data bus inversion) feature. It can help reduce both power consumption and power noise.

3.4.2.1. i.MX 8M Mini LPDDR4-3000 routing recommendations

LPDDR4-3000 needs to be routed with signal fly times matched shown in Table 21. The delay of the via transitions needs to be included in the overall calculation. This can be realized in Allegro tool by enabling the **Z Axis Delay** in "Setup - Constraints - Modes".

An example of the delay match calculation has been shown for the i.MX 8M Mini EVK board design in Table 22 and Table 23. This analysis was done for the LPDDR4-3000 implementation using the i.MX 8M Mini. In Table 22 and Table 23, the **PCB Delay** column is obtained directly from the Allegro PCB file, and the **Pkg Delay** column is the package delay obtained from Table 31.

NXP recommends that users simulate their LPDDR4 implementation before fabricating PCBs.

Table 21. i.MX 8M Mini LPDDR4-3000 routing recommendations

LPDDR4-3000				
LPDDR4 signal (each 16-bit channel)	**Group**	**PCB + package prop delay**		
		Min	**Max**	**Considerations**
CK_t/CK_c	Clock	Short as possible	200 ps	Match the true/complement signals within 1 ps.
CA[5:0]	Address/ Command/ Control	CK_t - 25 ps	CK_t + 25 ps	
CS[1:0]				
CKE[1:0]				
DQS0_t/DQS0_c	Byte 0 - DQS	CK_t - 85 ps	CK_t + 85 ps	Match the true/complement signals of DQS within 1 ps.
DM0	Byte 0 - Data	DQS0_t -10 ps	DQS0_t +10 ps	
DQ[7:0]				
DQS1_t/DQS1_c	Byte 1 - DQS	CK_t - 85 ps	CK_t + 85 ps	
DM1	Byte 1 - Data	DQS1_t -10 ps	DQS1_t +10 ps	
DQ[15:8]				

Table 22. LPDDR4 delay matching example (CA/CTL signals)

Net name	PCB delay (ps)	Pkg delay (ps)	Comments
DRAM_CK_T_A	140.1	41.1	Vias are L1-> L8->L1
	181.2		Total Net Delay
DRAM_CK_C_A	140.4	41.2	Vias are L1-> L8->L1
	181.6		Total Net Delay
DRAM_CA0_A	142.8	39.6	Vias are L1-> L3->L1
	182.4		Total Net Delay
DRAM_CA1_A	148.2	29.1	Vias are L1-> L3->L1
	177.3		Total Net Delay
DRAM_CA2_A	131.2	54.8	Vias are L1-> L3->L1
	186.0		Total Net Delay
DRAM_CA3_A	126.7	59.7	Vias are L1-> L3->L1
	186.4		Total Net Delay

Table 22. LPDDR4 delay matching example (CA/CTL signals)

Net name	PCB delay (ps)	Pkg delay (ps)	Comments
DRAM_CA4_A	145.9	33.8	Vias are L1-> L3->L1
	179.7		Total Net Delay
DRAM_CA5_A	145.7	32.0	Vias are L1-> L3->L1
	177.7		Total Net Delay
DRAM_nCS0_A	145.5	35.9	Vias are L1-> L3->L1
	181.4		Total Net Delay
DRAM_nCS1_A	138.1	44.2	Vias are L1-> L3->L1
	182.3		Total Net Delay
DRAM_CKE0_A	134.9	51.2	Vias are L1-> L3->L1
	186.1		Total Net Delay
DRAM_CKE1_A	142.4	39.9	Vias are L1-> L3->L1
	182.3		Total Net Delay

Table 23. LPDDR4 length matching example (byte lane 1 signals)

Net name	PCB delay (ps)	Pkg delay (ps)	Comments
DRAM_SDQS1_T_A	84.2	48.6	Vias are L1-> L8->L1
	132.8		Total Net Delay
DRAM_SDQS1_C_A	84.8	47.2	Vias are L1-> L8->L1
	132.0		Total Net Delay
DRAM_DMI1_A	75.6	58.6	Routed on top layer, no via
	134.2		Total Net Delay
DRAM_DATA8_A	89.0	45.0	Routed on top layer, no via
	134.0		Total Net Delay
DRAM_DATA9_A	83.9	50.1	Routed on top layer, no via
	134.0		Total Net Delay
DRAM_DATA10_A	87.9	46.2	Routed on top layer, no via
	134.1		Total Net Delay
DRAM_DATA11_A	86.9	47.2	Routed on top layer, no via
	134.1		Total Net Delay
DRAM_DATA12_A	94.3	40.3	Routed on top layer, no via
	134.7		Total Net Delay
DRAM_DATA13_A	86	48.8	Routed on top layer, no via
	134.8		Total Net Delay
DRAM_DATA14_A	76.4	58.4	Routed on top layer, no via
	134.8		Total Net Delay
DRAM_DATA15_A	81.8	52.4	Routed on top layer, no via
	134.2		Total Net Delay

3.4.2.2. LPDDR4-3000 routing example (i.MX 8M Mini)

Figure 3 to Figure 5 show the placement and routing of the LPDDR4 signals on the i.MX 8M Mini EVK board. The CLK and DQS signals are routed on bottom layer to save routing space on top layer and layer 3. Chanel A data byte lane 1 and channel B data byte lane 0 signals are routed on top layer, and Chanel A data byte lane 0, channel B data byte lane 1 and CA/CTL signals are routed on layer 3. This is to make the signal actually travels on the via as short as possible to minimize via crosstalk.

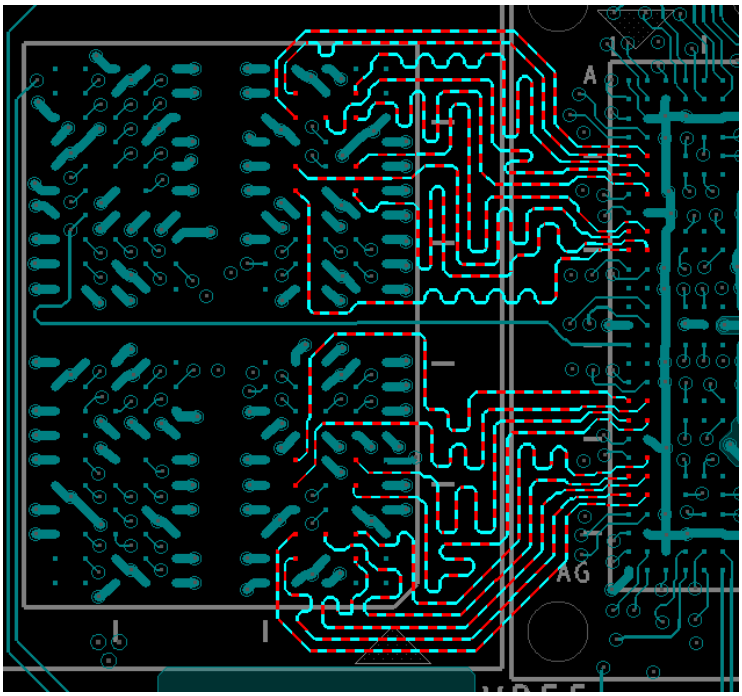

Figure 3. i.MX 8M Mini EVK board LPDDR4 routing (Top Layer)

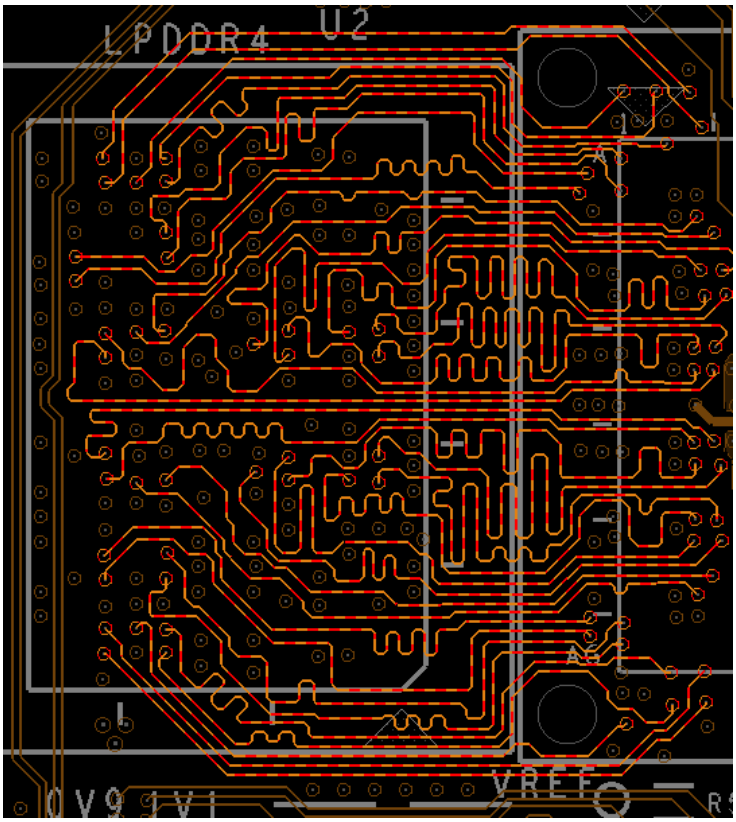

Figure 4. i.MX 8M Mini EVK board LPDDR4 routing (Layer 3)

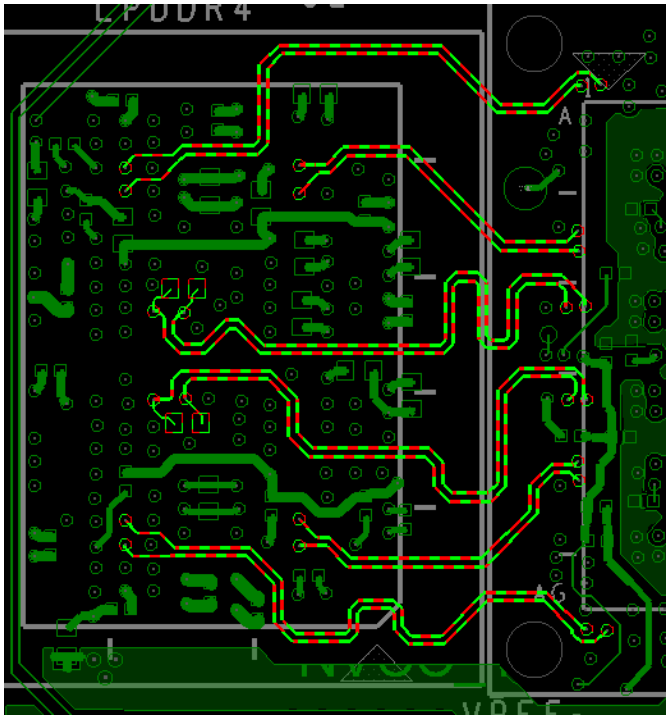

Figure 5. i.MX 8M Mini EVK board LPDDR4 routing (Bottom Layer)

3.4.3. i.MX 8M Mini DDR4-2400 design recommendations

The following list provides some generic guidelines for implementing an i.MX 8M Mini design using DDR4.

1. It is expected that the layout engineer and design team already has experience and training with DDR designs at speeds of 1.2 GHz / 2400 MT/s.
2. 2pcs x16 DRAM routed in T-topology is recommended to achieve total 2GB density. When doing T-topology routing, it is recommended to keep the propagation delay of each branch less than 150ps (about 900 mil in length), with no larger than 10ps difference between the two branches. In this case, VTT termination can be eliminated to ease routing and save BOM cost. In addition, there is an initial collapse on the eye diagram of Addr/Cmd/Ctrl due to absence of VTT termination. To make the sampling position still at the center of the eye opening, CK should be routed with propagation delay 100ps larger than that of Addr/Cmd/Ctrl, as shown in Figure 6.

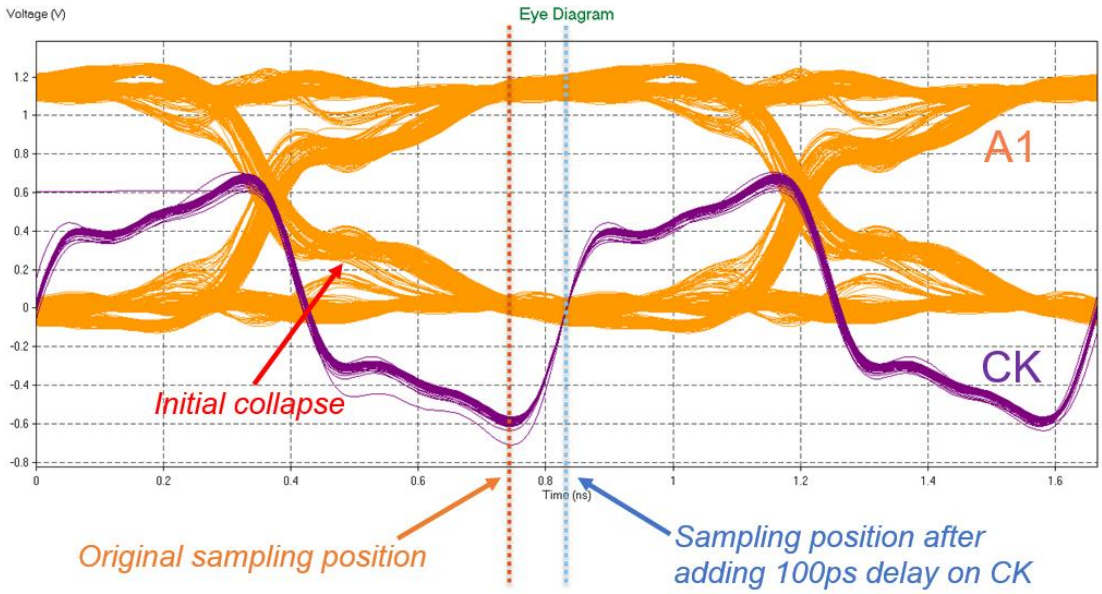

Figure 6. Initial eye collapse on address signals

3. DQ/DMI signal traces must refer to solid GND plane only. Addr/Cmd/Ctrl signal traces can refer to GND plane only or GND+VDDQ plane (when routed as strip line). Referring to VDDQ plane only is not allowed.
4. Keep edge-to-edge spacing of high-speed signal traces no less than 1.5 times the trace width to minimize trace crosstalk.
5. At a speed of 2400 MT/s, signal vias can be a significant source of crosstalk. If not properly designed, it can introduce crosstalk larger than that from the trace. To minimize via crosstalk, make sure that the number of vias on each point-to-point signal is no more than 2. For T-topology signal, only 1 via at transmitter, 1 at T-junction, 1 at each receiver is allowed. Place at least one ground stitching via within 50 mils of signal via when switching reference planes to provide continuous return path and reduce crosstalk. If it is not possible to place enough ground stitching vias due to space limitation, try to make the length that the signal actually travels on the via as short as possible, as illustrated in Figure 7.

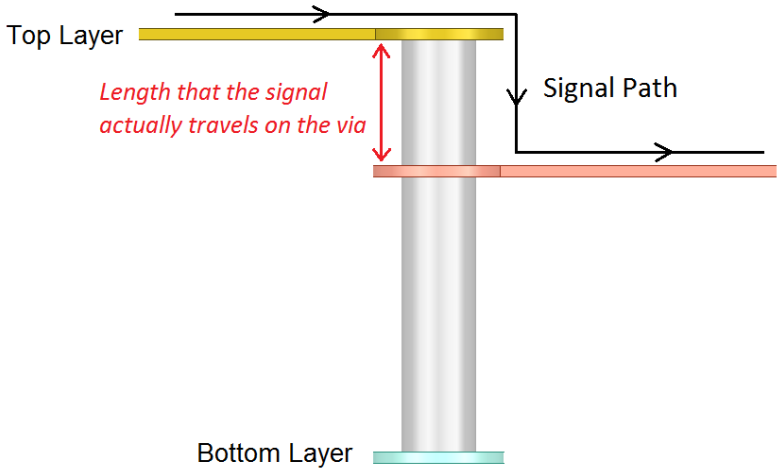

Figure 7. Length that the signal actually travels on the Via

6. CLK and DQS signal can be routed on different layers with DQ/CA signals to ease routing. When doing this, keep no less than 5 times trace width spacing from other signals.
7. Use time delay instead of length when performing the delay matching. The delay matching includes the PCB trace delay and the IC package delay. Incorporate the package pin delay into the CAD tool's constraint manager.
8. Include the delay of vias when performing delay matching. This can be realized in Allegro tool by enabling the **Z Axis Delay** in **Setup** -> **Constraints** -> **Modes**.
9. Byte swapping between upper/lower byte lane is allowed. Bit swapping within each slice/byte lane is allowed.
10. Bit swapping of Cmd/Addr/Ctrl signals is **NOT** allowed.
11. In general, the 2pcs DDR4 DRAM should be placed 300 mils away from each other, with 150 mils from the i.MX 8M Mini.
12. Enable the Data Bus Inversion (DBI) feature. It can help reduce both power consumption and power noise.

3.4.3.1. i.MX 8M Mini DDR4-2400 routing recommendations

DDR4-2400 needs to be routed with signal fly times matched shown in Table 24. The delay of the via transitions needs to be included in the overall calculation. This can be realized in Allegro tool by enabling the **Z Axis Delay** in **Setup** -> **Constraints** -> **Modes**.

An example of the delay match calculation has been shown for the i.MX 8M Mini DDR4 EVK board design in Table 25 and Table 26. This analysis is done for the DDR4-2400 implementation using the i.MX 8M Mini. In Table 25 and Table 26, the **PCB Delay** column is obtained directly from the Allegro PCB file, and the **Pkg Delay** column is the package delay obtained from Table 31.

Table 24. i.MX 8M Mini DDR4-2400 routing recommendations

DDR4-2400				
DDR4/DDR3L signal	**Group**	**PCB + package prop delay**		**Considerations**
		Min.	**Max.**	
CK_t/CK_c	Clock	Short as possible	500ps	Match the true/complement signals within 1 ps.
A[13:0]/BA[1:0]/BG0	Address/ Command/ Control	CK_t - 125 ps	CK_t - 75 ps	See section 3.4.3 item #2 for more details.
CS/RAS/WE/CAS				
CKE/ODT				
DQS0_t/DQS0_c	Byte 0 - DQS	Short as possible	CK_t + 1.0 * ^{t}CK	Match the true/complement signals of DQS within 1 ps.
DM0	Byte 0 - Data	DQS0_t -10 ps	DQS0_t +10 ps	
DQ[7:0]				
DQS1_t/DQS1_c	Byte 1 - DQS	Short as possible	CK_t + 1.0 * ^{t}CK	
DM1	Byte 1 - Data	DQS1_t -10 ps	DQS1_t +10 ps	
DQ[15:8]				
DQS2_t/DQS2_c	Byte 2 - DQS	Short as possible	CK_t + 1.0 * ^{t}CK	
DM2	Byte 2 - Data	DQS2_t -10 ps	DQS2_t +10 ps	
DQ[23:16]				
DQS3_t/DQS3_c	Byte 3 - DQS	Short as possible	CK_t + 1.0 * ^{t}CK	
DM3	Byte 3 - Data	DQS3_t -10 ps	DQS3_t +10 ps	
DQ[31:24]				

Table 25. DDR4 delay matching example (Addr/Cmd/Ctrl/CK signals)

Net name	PCB delay (ps)	Pkg delay (ps)	Comment
DRAM_A0 U1.AD5:U2.P3	237.9	56.5	Vias are L1-> L6->L8->L1
	294.4		Total Net Delay
DRAM_A0 U1.AD5:U3.P3	239.3	56.5	Vias are L1-> L4->L6->L8
	295.8		Total Net Delay
DRAM_A1 U1.U1:U2.P7	248.4	42.2	Vias are L1-> L3->L1
	290.6		Total Net Delay
DRAM_A1 U1.U1:U3.P7	248.7	42.2	Vias are L1-> L3->L1
	290.9		Total Net Delay
DRAM_A2 U1.U2:U3.R3	249.3	41.8	Vias are L1-> L3->L1
	291.2		Total Net Delay
DRAM_A2 U1.U2:U2.R3	249.3	41.8	Vias are L1-> L3->L1
	291.2		Total Net Delay
DRAM_A3 U1.N6:U2.N7	269.1	22.4	Vias are L1-> L6->L3->L1
	291.5		Total Net Delay
DRAM_A3 U1.N6:U3.N7	268.6	22.4	Vias are L1-> L6->L3->L1
	291		Total Net Delay
DRAM_A4 U1.K5:U3.N3	248.5	43.1	Vias are L1-> L6->L8->L1
	291.6		Total Net Delay
DRAM_A4 U1.K5:U2.N3	247.6	43.1	Vias are L1-> L6->L8->L1
	290.7		Total Net Delay
DRAM_A5 U1.N5:U2.P8	265.7	32.0	Vias are L1-> L6->L8->L1
	297.7		Total Net Delay
DRAM_A5 U1.N5:U3.P8	265.8	32.0	Vias are L1-> L6->L8->L1
	297.8		Total Net Delay
DRAM_A6 U1.N4:U3.P2	258.7	33.8	Vias are L1-> L6->L3->L1
	292.5		Total Net Delay

DRAM_A6 U1.N4:U2.P2	258.5	33.8	Vias are L1-> L6->L3->L1
	292.4		Total Net Delay
DRAM_A7 U1.E4:U2.R8	237.1	54.8	Vias are L1-> L6->L8->L1
	291.9		Total Net Delay
DRAM_A7 U1.E4:U3.R8	238.2	54.8	Vias are L1-> L6->L8->L1
	293		Total Net Delay
DRAM_A8 U1.D5:U2.R2	238.1	59.7	Vias are L1-> L6->L3->L1
	297.7		Total Net Delay
DRAM_A8 U1.D5:U3.R2	240.2	59.7	Vias are L1-> L6->L3->L1
	299.9		Total Net Delay
DRAM_A9 U1.J5:U2.R7	256.8	35.8	Vias are L1-> L6->L8->L1
	292.5		Total Net Delay
DRAM_A9 U1.J5:U3.R7	257.5	35.8	Vias are L1-> L6->L8->L1
	293.3		Total Net Delay
DRAM_A10 U1.AC4:U2.M3	232.1	59.5	Vias are L1-> L6->L3->L1
	291.6		Total Net Delay
DRAM_A10 U1.AC4:U3.M3	231.1	59.5	Vias are L1-> L6->L3->L1
	290.6		Total Net Delay
DRAM_A11 U1.K6:U3.T2	263.8	29.1	Vias are L1-> L6->L3->L1
	292.9		Total Net Delay
DRAM_A11 U1.K6:U2.T2	263.9	29.1	Vias are L1-> L6->L3->L1
	293		Total Net Delay
DRAM_A12 U1.J6:U3.M7	251.3	39.6	Vias are L1-> L6->L8->L1
	290.9		Total Net Delay
DRAM_A12 U1.J6:U2.M7	251.2	39.6	Vias are L1-> L6->L8->L1
	290.8		Total Net Delay
DRAM_A13 U1.W6:U3.T8	262.2	31.9	Vias are L1-> L6->L8->L1
	294.1		Total Net Delay
DRAM_A13 U1.W6:U2.T8	263.2	31.9	Vias are L1-> L6->L8->L1
	295.1		Total Net Delay
DRAM_BA0 U1.V6:U2.N2	262.2	34.4	Vias are L1-> L6->L8->L1
	296.6		Total Net Delay
DRAM_BA0 U1.V6:U3.N2	261.8	34.4	Vias are L1-> L6->L8->L1
	296.1		Total Net Delay
DRAM_BA1 U1.N1:U3.N8	237.3	53.4	Vias are L1-> L3>L1
	290.7		Total Net Delay
DRAM_BA1 U1.N1:U2.N8	237.7	53.4	Vias are L1-> L3>L1
	291.1		Total Net Delay
DRAM_BG0 U1.L2:U3.M2	251.4	41.1	Vias are L1-> L3>L1
	292.6		Total Net Delay
DRAM_BG0 U1.L2:U2.M2	249.8	41.1	Vias are L1-> L3>L1
	290.9		Total Net Delay
DRAM_CK_C U1.M2:U2.K8	351.1	39.4	Vias are L1-> L8>L1
	390.5		Total Net Delay
DRAM_CK_C U1.M2:U3.K8	357.2	39.4	Vias are L1-> L8>L1
	396.5		Total Net Delay
DRAM_CK_T U1.M1:U3.K7	356.3	39.1	Vias are L1-> L8>L1
	395.4		Total Net Delay
DRAM_CK_T U1.M1:U2.K7	351.3	39.1	Vias are L1-> L8>L1
	390.5		Total Net Delay
DRAM_NACT U1.F6:U3.L3	246.8	45.7	Vias are L1-> L6->L3->L1
	292.5		Total Net Delay
DRAM_NACT U1.F6:U2.L3	247.8	45.7	Vias are L1-> L6->L3->L1
	293.5		Total Net Delay
DRAM_NALERT U1.R2:U3.P9	255.7	36.0	Vias are L1-> L3>L1
	291.7		Total Net Delay
DRAM_NALERT	255.2	36.0	Vias are L1-> L3>L1

U1.R2:U2.P9	291.2		Total Net Delay
DRAM_NCAS(A15)	260.3	38.6	Vias are L1-> L6->L8->L1
U1.R5:U3.M8	298.9		Total Net Delay
DRAM_NCAS(A15)	260.4	38.6	Vias are L1-> L6->L8->L1
U1.R5:U2.M8	299		Total Net Delay
DRAM_NCKE	241.0	51.2	Vias are L1-> L6->L3->L1
U1.F4:U2.K2	292.2		Total Net Delay
DRAM_NCKE	242.2	51.2	Vias are L1-> L6->L3->L1
U1.F4:U3.K2	293.4		Total Net Delay
DRAM_NCS	257.0	35.9	Vias are L1-> L6->L3->L1
U1.K4:U3.L7	292.9		Total Net Delay
DRAM_NCS	255.9	35.9	Vias are L1-> L6->L3->L1
U1.K4:U2.L7	291.8		Total Net Delay
DRAM_NRAS	240.4	51.2	Vias are L1-> L3>L1
U1.T2:U3.L8	291.7		Total Net Delay
DRAM_NRAS	240.9	51.2	Vias are L1-> L3>L1
U1.T2:U2.L8	292.1		Total Net Delay
DRAM_NRESET	255.7	38.1	Vias are L1-> L3>L1
U1.R1:U3.P1	293.8		Total Net Delay
DRAM_NRESET	252.4	38.1	Vias are L1-> L3>L1
U1.R1:U2.P1	290.5		Total Net Delay
DRAM_NWE(A14)	247.8	43.1	Vias are L1-> L3>L1
U1.T1:U2.L2	290.9		Total Net Delay
DRAM_NWE(A14)	247.8	43.1	Vias are L1-> L3>L1
U1.T1:U3.L2	290.9		Total Net Delay
DRAM_ODT	271.5	26.5	Vias are L1-> L6->L3->L1
U1.V5:U3.K3	298		Total Net Delay
DRAM_ODT	270.4	26.5	Vias are L1-> L6->L3->L1
U1.V5:U2.K3	296.9		Total Net Delay
DRAM_PARITY	264.9	29.0	Vias are L1-> L6->L3->L1
U1.R6:U3.T3	293.9		Total Net Delay
DRAM_PARITY	262.8	29.0	Vias are L1-> L6->L3->L1
U1.R6:U2.T3	291.8		Total Net Delay

Table 26. DDR4 delay matching example (Byte0 signals)

Net Name	PCB Delay (ps)	Pkg Delay (ps)	Comment
DRAM_DMI0	101.8	57.2	Vias are L1-> L3->L1
	159.0		Total Net Delay
DRAM_DQS0_N	102.6	58.9	Vias are L1-> L8->L1
	161.6		Total Net Delay
DRAM_DQS0_P	102.9	59.0	Vias are L1-> L8->L1
	161.9		Total Net Delay
DRAM_DQ0	114.0	47.2	Vias are L1-> L3->L1
	161.2		Total Net Delay
DRAM_DQ1	117.3	43.0	Vias are L1-> L3->L1
	160.4		Total Net Delay
DRAM_DQ2	104.5	54.6	Vias are L1-> L3->L1
	159.1		Total Net Delay
DRAM_DQ3	106.5	51.7	Vias are L1-> L3->L1
	158.2		Total Net Delay
DRAM_DQ4	98.9	59.9	Vias are L1-> L3->L1
	158.8		Total Net Delay
DRAM_DQ5	99.6	58.1	Vias are L1-> L3->L1
	157.7		Total Net Delay
DRAM_DQ6	101.9	64.6	Vias are L1-> L3->L1
	166.5		Total Net Delay
DRAM_DQ7	105.3	51.4	Vias are L1-> L3->L1

	156.7	Total Net Delay

3.4.3.2. DDR4-2400 Routing example (i.MX 8M Mini)

Figure 8 to Figure 11 show the placement and routing of the DDR4 signals on the i.MX8M Mini DDR4 EVK board.

The CK and DQS signals are routed on the bottom layer to save routing space of other signal layers. Data signals are all routed on the top layer and layer 3, which can minimize via crosstalk to achieve enough timing margin for the 2400 MT/s high-speed signals. This is to make the signal actually travel on the via as short as possible to minimize via crosstalk. Addr/Cmd/Ctrl signals are routed in T-topology, with trunk on the top layer and layer 6, and branch on layer 3 and the bottom layer. Applying the same principle of making the length that the signal actually travels on the via short to minimize via crosstalk, for the trunks routed on the top layer, their branches are all routed on layer 3, forming a layer transition of L1-> L3->L1, which means that no ground via is essentially needed. And for the trunks routed on layer 6, their branches are mostly routed on layer 3, forming a layer transition of L1->L6->L3->L1, so that ground vias are only needed under the 8M Mini package and at T-junction. The remaining branches are routed on the bottom layer, forming a layer transition of L1->L6->L8->L1, which means ground vias are needed under the 8M Mini package as well as both DRAM packages.

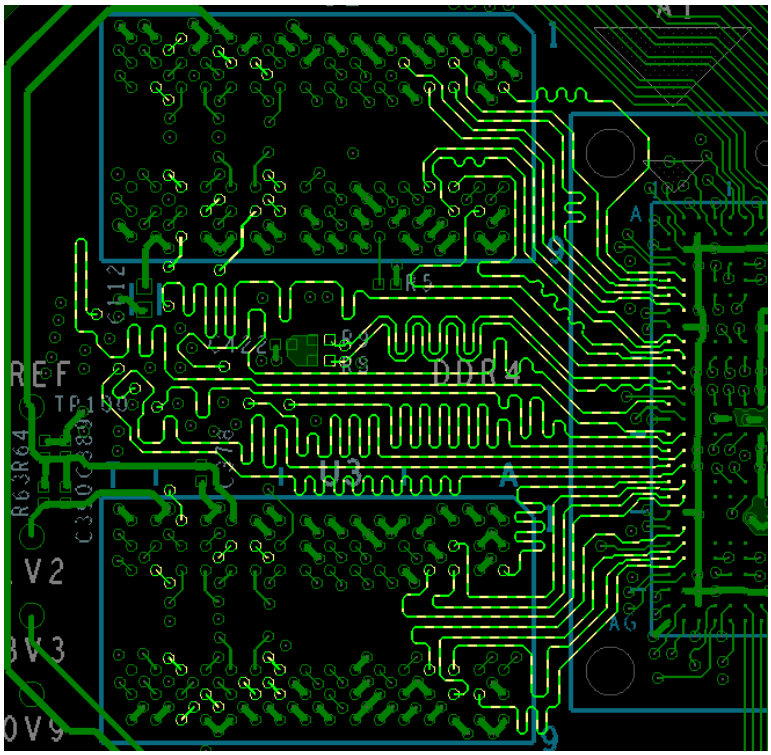

Figure 8. i.MX 8M Mini DDR4 EVK board DDR4 routing (Top Layer)

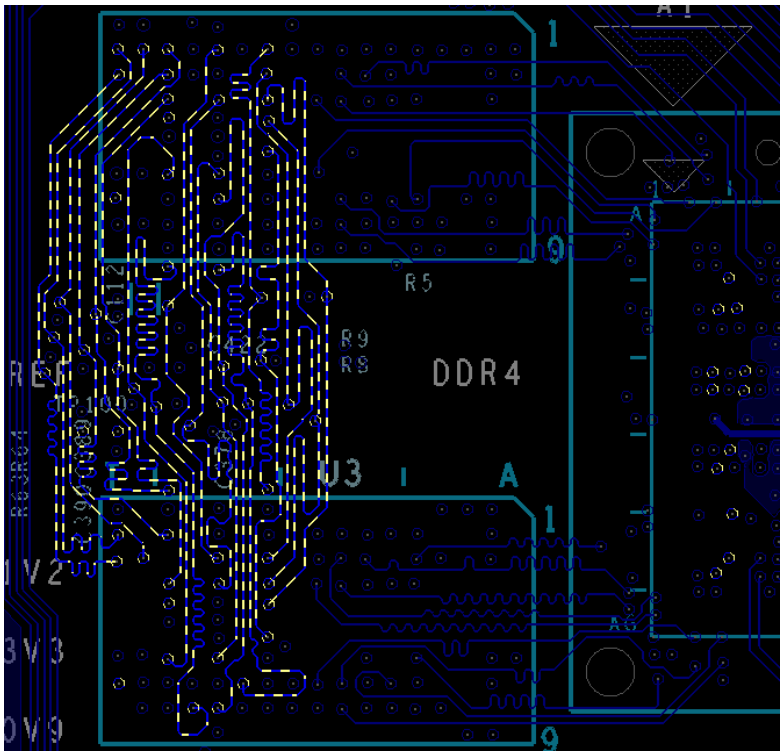

Figure 9. i.MX 8M Mini DDR4 EVK board DDR4 routing (Layer 3)

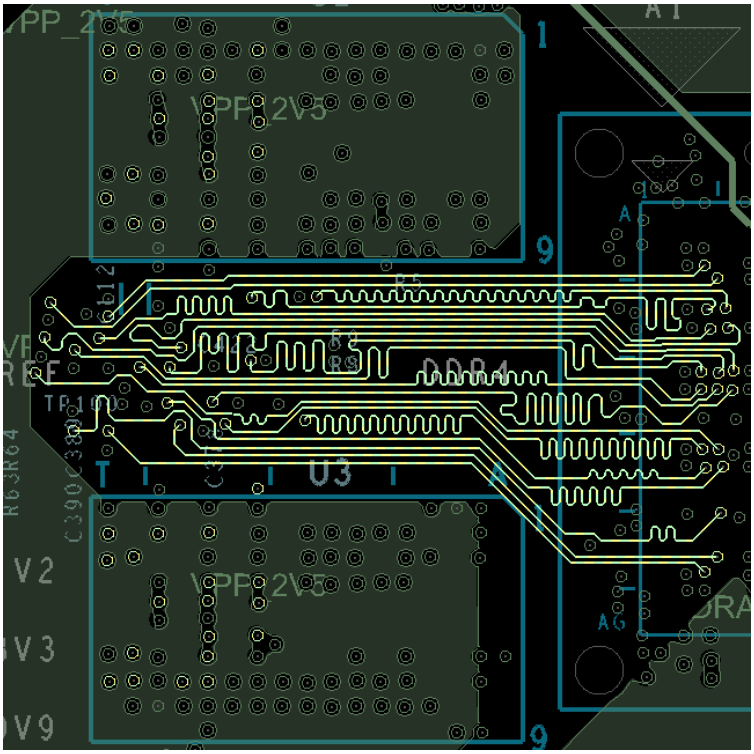

Figure 10. i.MX 8M Mini DDR4 EVK board DDR4 routing (Layer 6)

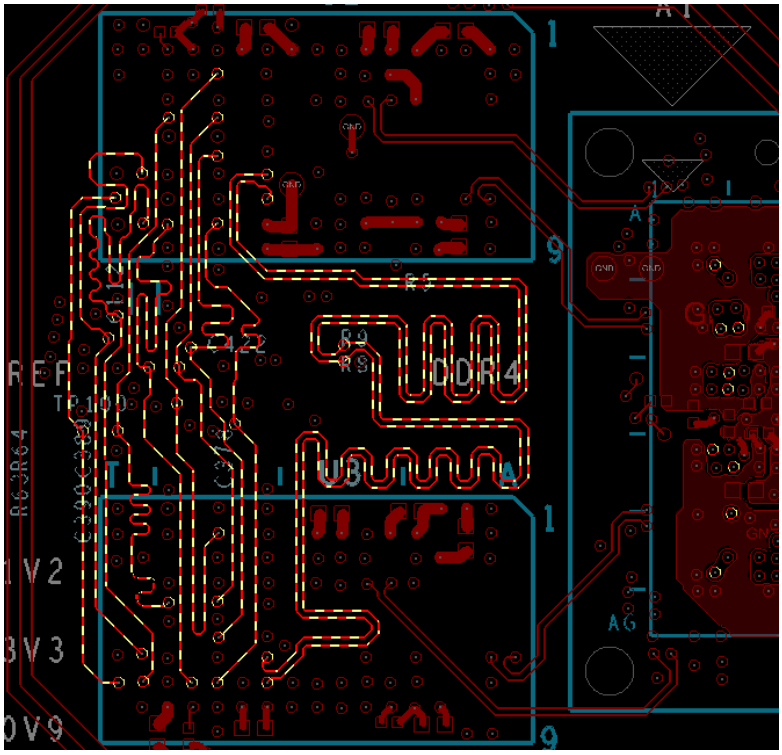

Figure 11. i.MX 8M Mini DDR4 EVK board DDR4 routing (Bottom Layer)

3.4.4. i.MX 8M Mini DDR3L-1600 design recommendations

The following list provides some generic guidelines for implementing an i.MX8M Mini design using DDR3L.

1. 4pcs x16 DRAM routed in T-topology forming a 2-rank system is recommended to achieve total 2GB density. And it would be best to mount each rank of SDRAM on the top and bottom of the board mirroring each in a clamshell design like they do for DIMM modules for highest performance.

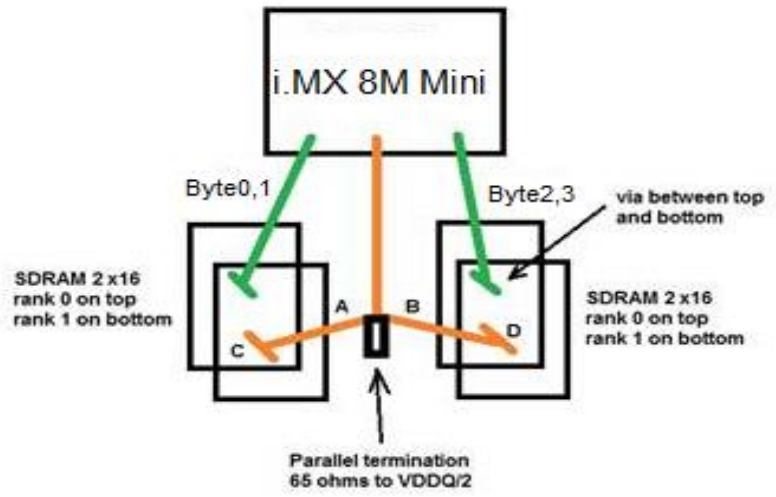

Figure 12. PCB routing topology for a 2-rank system

2. As illustrated in Figure 12, for data bytes, route straight from SoC to the SDRAM devices and via up and down with minimal stubs. For address/command signals, it is a T structure with branch to the SDRAM devices and via up and down with minimal stubs. And add a parallel termination (about 65 ohm to VDDQ/2 or VTT) at the branch point of the T.
3. The branch and stubs to the SDRAM pins must be the same length on both sides of the branch point (A+C=B+D); otherwise, the signal will show significant distortion. In addition, try to minimize the length of the branch as it is unterminated at the SDRAM devices.
4. All data signals within a byte lane should have the same number of vias/layer changes.
5. All the high-speed signal traces must be referred to solid GND or NVCC_DRAM (VDDQ) plane. Do not refer to other power planes.
6. For DQ nets, bit swapping within each slice/byte lane is allowed.
7. For Address nets, use address mirroring to minimize top-to-bottom stubs. i.MX 8M Mini supports address mirroring but the wiring from i.MX 8M Mini to the two DRAM ranks must conform to Figure 1.
8. For detailed information about Address Mirroring Feature, see Section 3.1 in DDR3 SDRAM Unbuffered DIMM Design Specification.

Table 27. Wiring definition for DDR3L address mirroring

DDR3L-1600		
i.MX 8M Mini pin	DRAM pin	
	Rank 0	Rank 1
A3	A3	A4
A4	A4	A3
A5	A5	A6
A6	A6	A5
A7	A7	A8

Table 27. Wiring definition for DDR3L address mirroring

A8	A8	A7
BA0	BA0	BA1
BA1	BA1	BA0

9. The DQ/DMI/DQS signal must follow 3 W rule (center to center) to minimize trace crosstalk.
10. Place at least one ground stitching via within 50 mils of signal via when switching reference planes to provide continuous return path and reduce crosstalk. If it is not possible to place enough ground stitching vias due to space limitation, try to make the length that the signal actually travels on the via as short as possible, as illustrated in Figure 13.

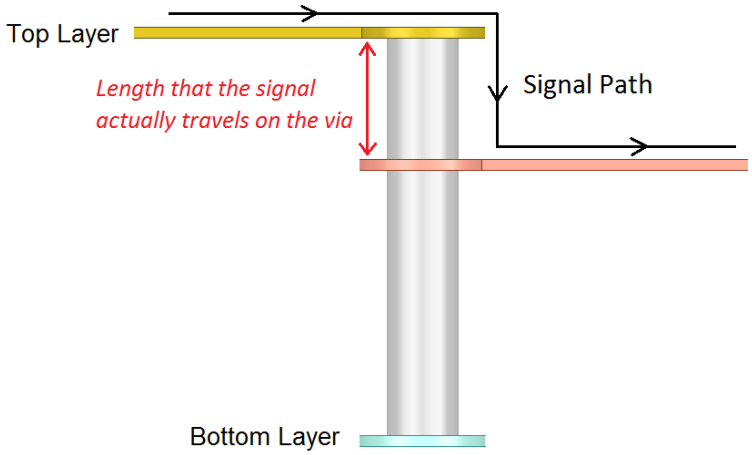

Figure 13. Length that the signal actually travels on the Via

11. Use time delay instead of length when performing the delay matching. The delay matching includes the PCB trace delay and the IC package delays. Incorporate the package pin delay into the CAD tool's constraint manager.
12. Consider the delay of vias when performing delay matching. This can be realized in the Allegro tool by enabling **Z Axis Delay** in **Setup** -> **Constraints** -> **Modes**.

3.4.4.1. i.MX 8M Mini DDR3L-1600 routing recommendations

DDR3L-1600 needs to be routed with signal fly times matched as shown in Table 28.

The delay of the via transitions needs to be included in the overall calculation. This can be realized in the Allegro tool by enabling **Z Axis Delay** in **Setup** -> **Constraints** -> **Modes**.

An example of the delay match calculation is shown for the i.MX 8M Mini validation board design in Table 29 and Table 30. This analysis is done for the DDR3L-1600 implementation using the i.MX 8M Mini. In Table 29 and Table 30, the **PCB Delay** column is obtained directly from the Allegro PCB file, and the **Pkg Delay** column is the package delay obtained from Table 31.

NXP recommends that users simulate their DDR implementation before fabricating PCBs.

Table 28. i.MX 8M Mini DDR3L-1600 routing recommendations

DDR3L-1600				
DDR4/DDR3L signal	Group	PCB + package prop delay		Considerations
		Min	Max	
CK_t/CK_c	Clock	Short as possible	500ps	Match the true/complement signals within 1 ps.
A[15:0] CS[1:0]/RAS/WE/CAS BA[2:0] CKE[1:0]/ ODT[1:0]	Address/ Command/ Control	CK_t - 25 ps	CK_t + 25 ps	-
DQS0_t/DQS0_c	Byte 0 - DQS	Short as possible	CK_t + 1.0 * ^{t}CK	Match the true/complement signals of DQS within 1 ps.
DM0 DQ[7:0]	Byte 0 - Data	DQS0_t -10 ps	DQS0_t +10 ps	
DQS1_t/DQS1_c	Byte 1 - DQS	Short as possible	CK_t + 1.0 * ^{t}CK	
DM1 DQ[15:8]	Byte 1 - Data	DQS1_t -10 ps	DQS1_t +10 ps	
DQS2_t/DQS2_c	Byte 2 - DQS	Short as possible	CK_t + 1.0 * ^{t}CK	
DM2 DQ[23:16]	Byte 2 - Data	DQS2_t -10 ps	DQS2_t +10 ps	
DQS3_t/DQS3_c	Byte 3 - DQS	Short as possible	CK_t + 1.0 * ^{t}CK	
DM3 DQ[31:24]	Byte 3 - Data	DQS3_t -10 ps	DQS3_t +10 ps	

Table 29. DDR3L delay matching example (CA/CTL/CMD/CK signals)

Net name	PCB delay (ps)	Pkg delay (ps)	Comment
A0 U101.AD5:U102.N3	307.9	56.5	Vias are L1-> L4->L3->L1
	364.4		Total Net Delay
A1 U101.U1:U102.P7	308.6	42.2	Vias are L1-> L8->L6->L1
	350.8		Total Net Delay
A2 U101.U2:U102.P3	306	41.8	Vias are L1-> L8->L3->L1
	347.8		Total Net Delay
A3 U101.N6:U102.N2	326.4	22.4	Vias are L1-> L4->L3->L1
	348.8		Total Net Delay
A4 U101.K5:U102.P8	304.6	43.1	Vias are L1-> L4->L6->L1
	347.7		Total Net Delay
A5 U101.N5:U102.P2	315.6	32.0	Vias are L1-> L4->L3->L1
	347.6		Total Net Delay
A6 U101.N4:U102.R8	316.4	33.8	Vias are L1-> L8->L6->L1
	350.2		Total Net Delay
A7 U101.E4:U102.R2	295.5	54.8	Vias are L1-> L4->L3->L1
	350.3		Total Net Delay
A8 U101.D5:U102.T8	304.8	59.7	Vias are L1-> L4->L6-> L1
	364.5		Total Net Delay
A9 U101.J5:U102.R3	311.2	35.8	Vias are L1-> L4->L6->L1
	347		Total Net Delay
A10 U101.AC4:U102.L7	290.5	59.5	Vias are L1-> L4->L6->L1
	350		Total Net Delay
A11 U101.K6:U102.R7	318.1	29.1	Vias are L1-> L4->L3->L1
	347.2		Total Net Delay

A12 U101.J6:U102.N7	307.1	39.6	Vias are L1-> L4->L6-> L1
	346.7		Total Net Delay
A13 U101.W6:U102.T3	329.9	31.9	Vias are L1-> L4->L6->L1
	361.8		Total Net Delay
A14 U101.L1:U102.T7	308.9	41.2	Vias are L1-> L8->L3->L1
	350.1		Total Net Delay
A15 U101.F6:U102.M7	302.8	45.7	Vias are L1-> L4->L3->L1
	348.5		Total Net Delay
BA0 U101.V6:U102.M2	314.6	34.4	Vias are L1-> L4->L3->L1
	349		Total Net Delay
BA1 U101.N1:U102.N8	295.8	53.4	Vias are L1-> L8->L6-> L1
	349.2		Total Net Delay
BA2 U101.L2:U102.M3	310.7	41.1	Vias are L1-> L8->L3-> L1
	351.8		Total Net Delay
CAS_N U101.R5:U102.K3	307	38.6	Vias are L1-> L4->L3->L1
	345.6		Total Net Delay
CKE0 U101.F4:U102.K9	294.6	51.2	Vias are L1-> L8->L6->L1
	345.8		Total Net Delay
CKE1 U101.F5:U104.K	306.7	39.9	Vias are L1-> L4->L3->L8
	346.6		Total Net Delay
CLK0_C U101.M2:U102.K7	316.2	39.4	Vias are L1->L6->L1
	355.6		Total Net Delay
CLK0_T U101.M1:U102.J7	316.2	39.1	Vias are L1->L6->L1
	355.3		Total Net Delay
CLK1_C U101.AB5:U104.K7	303.9	51.6	Vias are L1-> L6->L3->L8
	355.5		Total Net Delay
CLK1_T U101.AB4:U104.J7	303.2	51.6	Vias are L1-> L6->L3->L8
	354.8		Total Net Delay
CS0_N U101.K4:U102.L2	309.8	35.9	Vias are L1-> L4->L3->L1
	345.7		Total Net Delay
CS1_N U101.AB6:U104.L2	306.2	42.1	Vias are L1-> L4->L6->L8
	348.3		Total Net Delay
ODT0 U101.V5:U102.K1	320.8	26.5	Vias are L1-> L4->L6->L1
	347.3		Total Net Delay
ODT1 U101.W5:U104.K1	311.7	35.1	Vias are L1-> L4->L3-> L8
	346.8		Total Net Delay
RAS_N U101.T2:U102.J3	303.4	51.2	Vias are L1-> L8->L6->L1
	.354.6		Total Net Delay
WE_N U101.T1:U102.L3	304.2	43.1	Vias are L1-> L4->L6->L1
	347.3		Total Net Delay

Table 30. DDR3L delay matching example (CA/CTL/CMD/CK signals)

Net Name	PCB Delay (ps)	Pkg Delay (ps)	Comment
DM0	149.2	57.2	Vias are L1-> L3->L1
	206.4		Total Net Delay
DQS0_C	149.7	58.9	Vias are L1-> L3->L1
	208.6		Total Net Delay
DQS0_T	149.9	59	Vias are L1-> L3->L1
	208.9		Total Net Delay
DQ0	157.5	47.2	Vias are L1-> L3->L1
	204.7		Total Net Delay
DQ1	162.9	43	Vias are L1-> L3->L1
	205.9		Total Net Delay

DQ2	150.4	54.6	Vias are L1-> L3->L1
	205		Total Net Delay
DQ3	153	51.7	Vias are L1-> L3->L1
	204.7		Total Net Delay
DQ4	149.6	59.9	Vias are L1-> L3->L1
	209.5		Total Net Delay
DQ5	152.6	58.1	Vias are L1-> L3->L1
	210.7		Total Net Delay
DQ6	148.1	64.6	Vias are L1-> L3->L1
	212.7		Total Net Delay
DQ7	158.9	51.4	Vias are L1-> L3->L1
	210.3		Total Net Delay

3.4.4.2. DDR3L-1600 Routing example (i.MX 8M Mini)

Figure 14 to Figure 18 show the placement and routing of the DDR3L signals on the i.MX 8M Mini validation board.

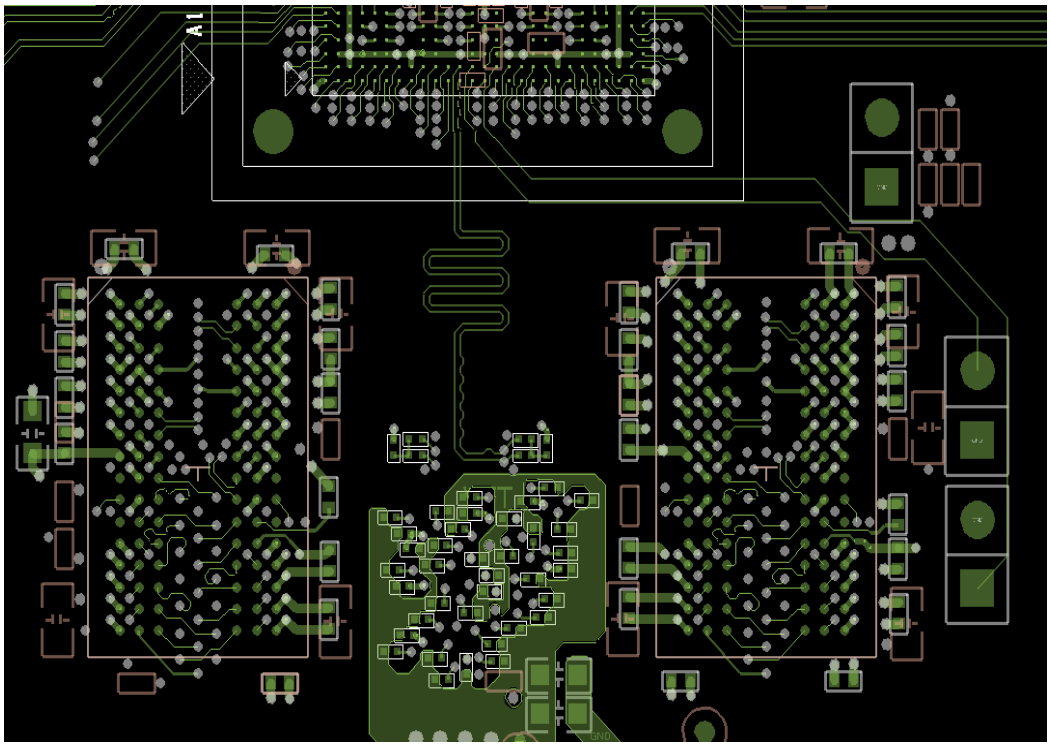

Figure 14. i.MX 8M Mini validation board DDR3L routing (top layer)

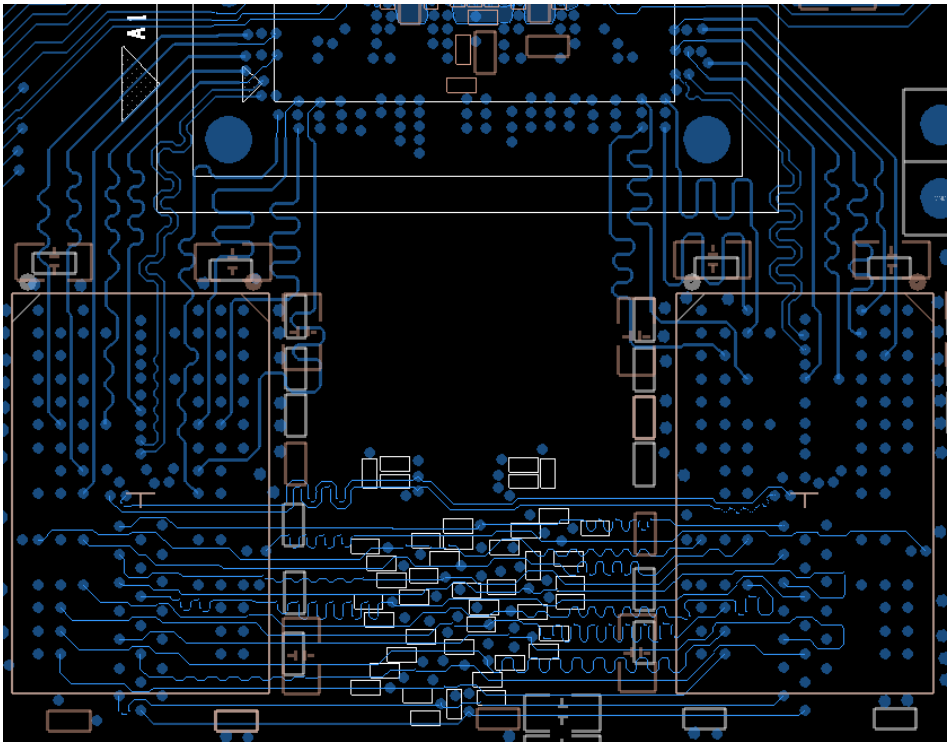

Figure 15. i.MX 8M Mini validation board DDR3L routing (Layer 3)

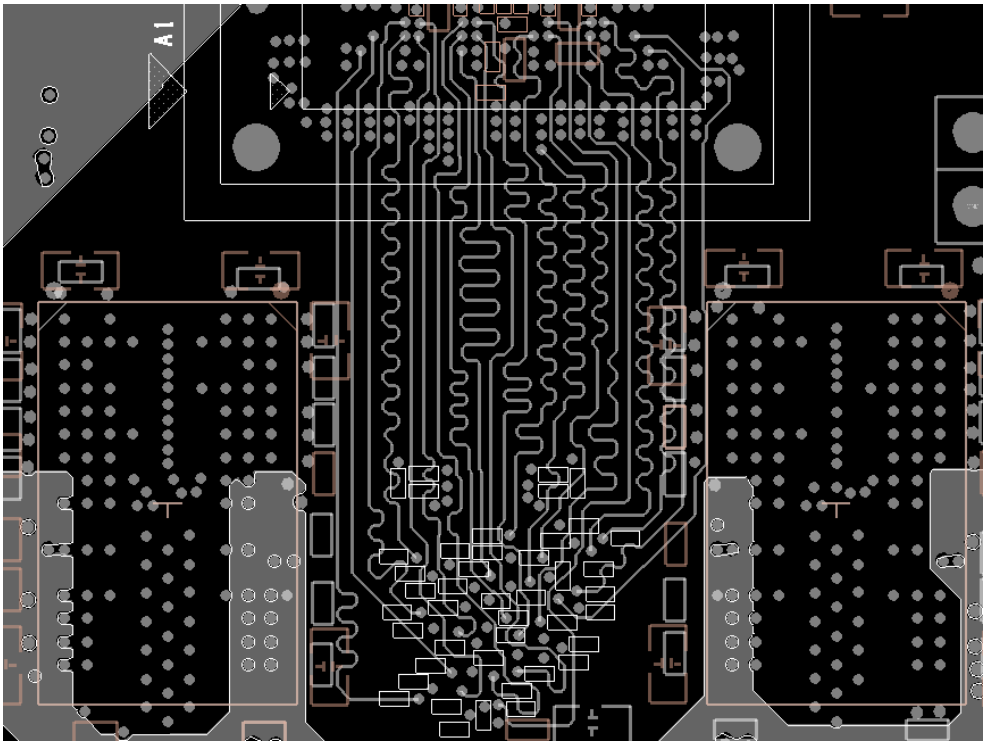

Figure 16. i.MX 8M Mini validation board DDR3L routing (Layer 4)

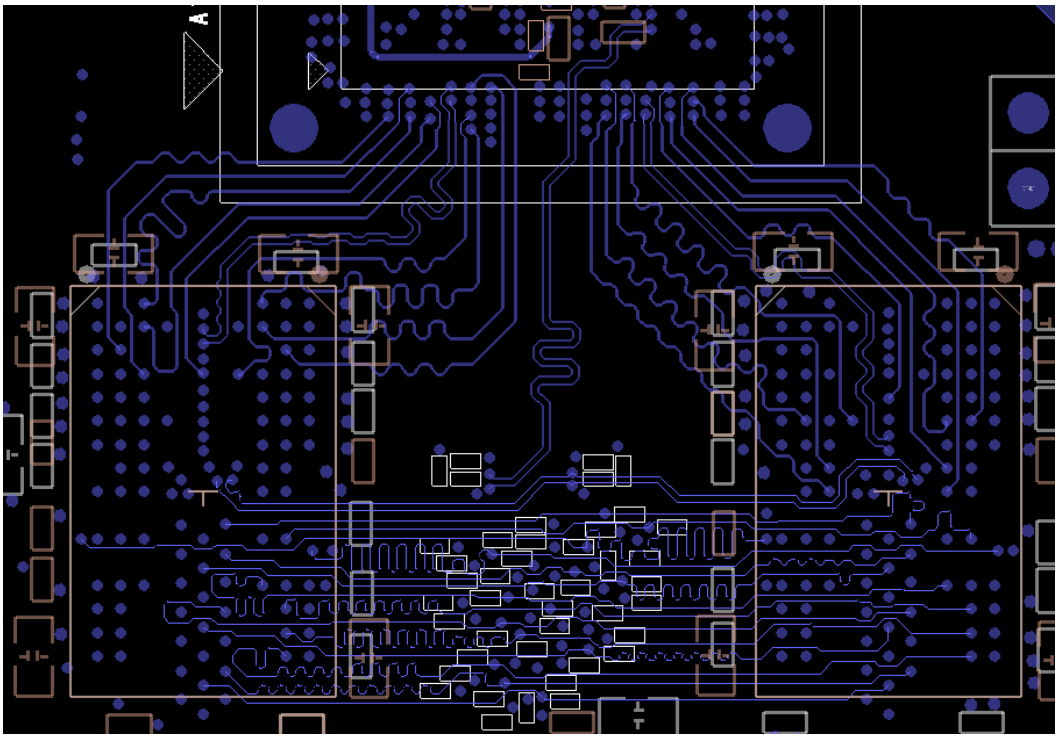

Figure 17. i.MX 8M Mini validation board DDR3L routing (Layer 6)

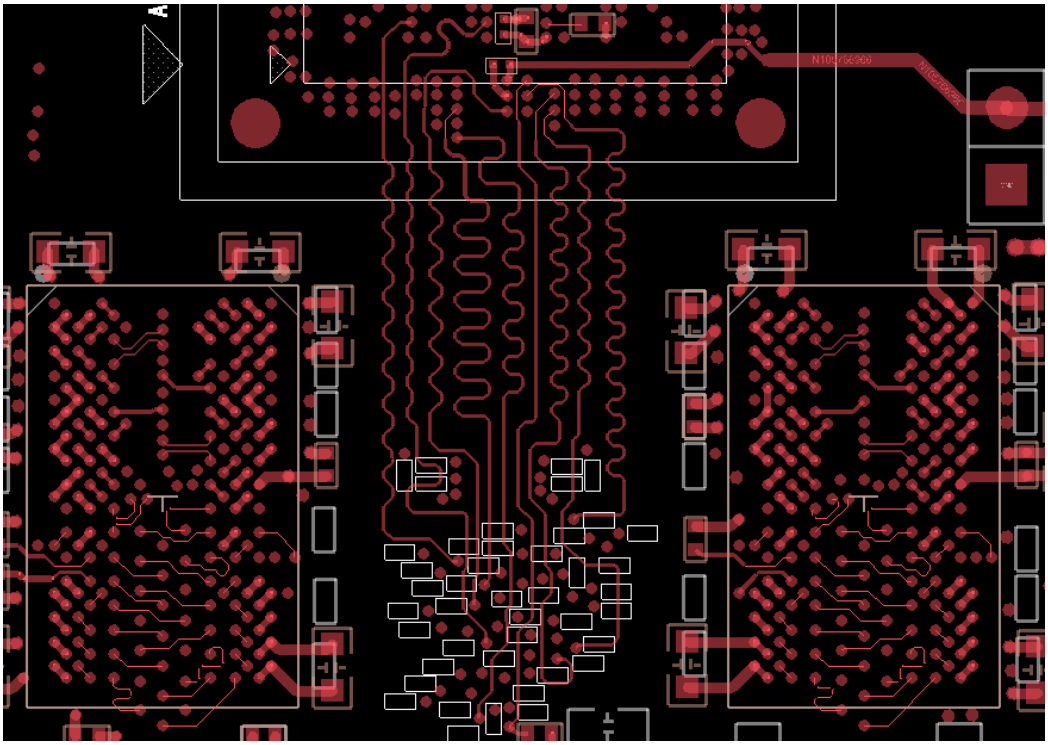

Figure 18. i.MX 8M Mini validation board DDR3L routing (Layer 8)

3.4.5. i.MX 8M Mini DDR SI simulation guide

The simulation architecture includes the DDR controller (i.e., the i.MX 8M Mini processor), the PCB and the DRAM device. The IBIS model for the i.MX 8M Mini processor is available from NXP. The DRAM device IBIS model must be obtained from the memory vendor.

This section describes how to check SI performance of the layout for a DDR design using the i.MX 8M Mini.

- Firstly, perform S-parameter extraction:
  - It requires a 2.5D full-wave extraction tool, such as PowerSI from Cadence.
  - Set the extraction bandwidth to 20 GHz.
  - Port reference impedance: 50 Ω for signal ports, and 0.1 Ω for power ports.
  - Coupled mode: Set the rise time to 20 ps and coupling coefficient to 1%.
- Secondly, perform time domain simulation:
  - Stimulus pattern: 500-bit random code and different pattern for each signal within the same byte.
  - Ideal power.
  - Probe at the die.
  - Simulation at slow corner (worst case).
  - Eye waveform triggered by aligning with the timing reference (DQS/CLK).

When the simulation is done, find the simulated worst eye width and compare with following requirements to see if it can pass:

- For LPDDR4-3000
  - DQ Write: Eye width @V_{REF} ±70mV should be over 248 ps.
  - DQ Read: Eye width @V_{REF} ±70mV should be over 201 ps.
  - Cmd/Addr/Ctrl: Eye width @V_{REF} ±77.5mV should be over 563 ps.
- For DDR4-2400
  - DQ Write: Eye width @V_{REF} ±65mV should be over 276 ps.
  - DQ Read: Eye width @V_{REF} ±70mV should be over 225 ps.
  - Cmd/Addr/Ctrl: Eye width at threshold should be over 579 ps.
- For DDR3L-1600
  - DQ Write: Eye width at threshold should be over 395 ps.
  - DQ Read: Eye width @641.5 ±70mV should be over 370 ps.
  - Cmd/Addr/Ctrl: Eye width at threshold should be over 727 ps.

Figure 19 shows an example of simulated eye width of LPDDR4-3000 DQ write.

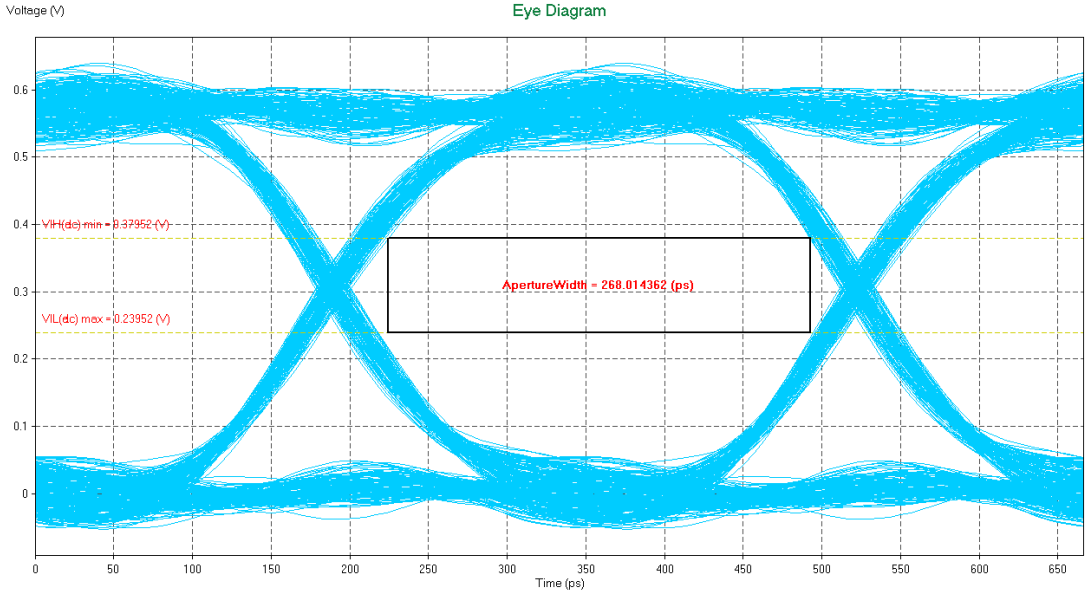

Figure 19. Example of simulated eye width

3.4.6. i.MX 8M Mini DDR package delay

When performing the required delay matching for LPDDR4/DDR4 routing, the bond wires within the i.MX 8M Mini package need to be accounted for and included in the match calculation. Table 31 lists the propagation/fly time from the die I/O to the package ball.

Table 31. i.MX 8M Mini DDR package trace delays

Ball Name	Delay (ps)	Ball name	Delay (ps)
DRAM_AC00	51.2	DRAM_DM2	52.8
DRAM_AC01	39.9	DRAM_DM3	53.1
DRAM_AC02	35.9	DRAM_DQS0_N	58.9
DRAM_AC03	44.2	DRAM_DQS0_P	59.0
DRAM_AC04	41.1	DRAM_DQS1_N	47.2
DRAM_AC05	41.2	DRAM_DQS1_P	48.6
DRAM_AC06	45.7	DRAM_DQS2_N	48.6
DRAM_AC07	35.8	DRAM_DQS2_P	49.9
DRAM_AC08	39.6	DRAM_DQS3_N	55.0
DRAM_AC09	29.1	DRAM_DQS3_P	55.5
DRAM_AC10	54.8	DRAM_DQ00	47.2
DRAM_AC11	59.7	DRAM_DQ01	43.0
DRAM_AC12	33.8	DRAM_DQ02	54.6
DRAM_AC13	32.0	DRAM_DQ03	51.7
DRAM_AC14	43.1	DRAM_DQ04	59.9
DRAM_AC15	22.4	DRAM_DQ05	58.1
DRAM_AC16	39.1	DRAM_DQ06	64.6
DRAM_AC17	39.4	DRAM_DQ07	51.4
DRAM_AC19	43.4	DRAM_DQ08	45.0
DRAM_AC20	51.6	DRAM_DQ09	50.1
DRAM_AC21	51.6	DRAM_DQ10	46.2
DRAM_AC22	47.7	DRAM_DQ11	47.2
DRAM_AC23	40.0	DRAM_DQ12	40.3
DRAM_AC24	41.8	DRAM_DQ13	48.8

Table 31. i.MX 8M Mini DDR package trace delays

Ball Name	Delay (ps)	Ball name	Delay (ps)
DRAM_AC25	42.2	DRAM_DQ14	58.4
DRAM_AC26	53.4	DRAM_DQ15	52.4
DRAM_AC27	29.0	DRAM_DQ16	51.4
DRAM_AC28	31.9	DRAM_DQ17	49.9
DRAM_AC29	34.4	DRAM_DQ18	54.5
DRAM_AC30	59.5	DRAM_DQ19	42.0
DRAM_AC31	56.5	DRAM_DQ20	53.6
DRAM_AC32	34.3	DRAM_DQ21	49.8
DRAM_AC33	38.6	DRAM_DQ22	54.7
DRAM_AC34	43.1	DRAM_DQ23	48.0
DRAM_AC35	51.2	DRAM_DQ24	60.2
DRAM_AC36	26.5	DRAM_DQ25	51.3
DRAM_AC37	35.1	DRAM_DQ26	48.8
DRAM_AC38	42.1	DRAM_DQ27	58.0
DRAM_ALERT_N	36.0	DRAM_DQ28	59.1
DRAM_RESET_N	38.1	DRAM_DQ29	58.1
DRAM_DM0	57.2	DRAM_DQ30	50.0
DRAM_DM1	58.6	DRAM_DQ31	44.2

3.4.7. High-speed routing recommendations

The following lists the routing traces for high-speed signals. The propagation delay and the impedance control should match to ensure the correct communication with the devices.

- High-speed signals (DDR, PCIe, RGMII, MIPI, etc.) must not cross gaps in the reference plane.
- Avoid creating slots, voids, and splits in reference planes. Review via placements to ensure that they do not inadvertently create splits/voids (i.e., space vias out to eliminate this possibility).
- Ensure that ground stitching vias are present within 50 mils from signal layer transition vias on high-speed signals when transitioning between different reference ground planes.
- A solid GND plane must be directly under crystals, associated to components and traces.
- Clocks or strobes that are on the same layer need at least 2.5x height from reference plane spacing from adjacent traces to reduce crosstalk.
- All synchronous interfaces should have appropriate bus delay matching.
- The true and complementary signal of a differential pair must have delay matched to within 1ps.

3.4.8. Reset architecture/routing

A reset button may be connected to PWRON_B pin of the PMIC (BD71847MWV) for development purposes. This allows all voltages to be put to their initial default power-on state when depressing the reset button.

Pressing the reset button causes the PMIC to trigger a cold reset event. This will cause all the power supplies except for the SNVS domain to be OFF. During this time, the POR_B driven by the PMIC will also keep asserted (low). This state will keep several hundred milliseconds to provide enough time for the power supplies to be completely powered down, and then the power supplies will start to ramp up again in defined sequence. When all the power supplies have reached their operating voltages, POR_B will be de-asserted, and the CPU may begin booting from reset.

3.5. Trace impedance recommendations

Table 32 is a reference when you are updating or creating constraints in the PCB design tool to set up the impedances/trace widths.

Table 32. Trace impedance recommendations

Signal group	Impedance	PCB manufacturer tolerance (+/-)
All single-ended signals, unless specified	50 Ω Single-ended	10%
DDR DQS/CLK, PCIe TX/RX data pairs and reference clock	85 Ω Differential	10%
USB differential signals	90 Ω Differential	10%
Differential signals, including Ethernet, MIPI (CSI and DSI)	100 Ω Differential	10%

3.6. Power connectivity/routing

Delivering clean, reliable power to the i.MX 8M Mini internal power rails is critical to a successful board design. The PCB PDN should be designed to accommodate the maximum output current from each SMPS into the i.MX 8M Mini supply balls. Table 33 lists the design goals for each high-current i.MX 8M Mini power rail.

Table 33. i.MX 8M Mini maximum current design levels

Supply input	i.MX 8M Mini Max current (mA)
VDD_ARM	2200
VDD_SOC	1000
VDD_DRAM&VPU&GPU	2500
NVCC_DRAM	1000

3.6.1. i.MX 8M Mini power distribution block diagram

There are companion PMICs that provide a low-cost and efficient solution for powering the i.MX 8M Mini processor, for example, ROHM BD71847.

The default output of BUCK8 is 1.1 V, which is for LPDDR4 NVCC_DRAM. You can modify the voltage to 1.2 V for DDR4, and 1.35 V for DDR3L by programming PMIC in SPL code before the U-Boot or kernel image is loaded onto DDR. This function has been fully verified, so you can use the **ONE** PMIC part for all kinds of DDR memories.

Figure 20 shows a block diagram of the power tree of the NXP i.MX 8M Mini EVK board. It uses a single BD71847MWV PMIC to power ON rails of the processor.

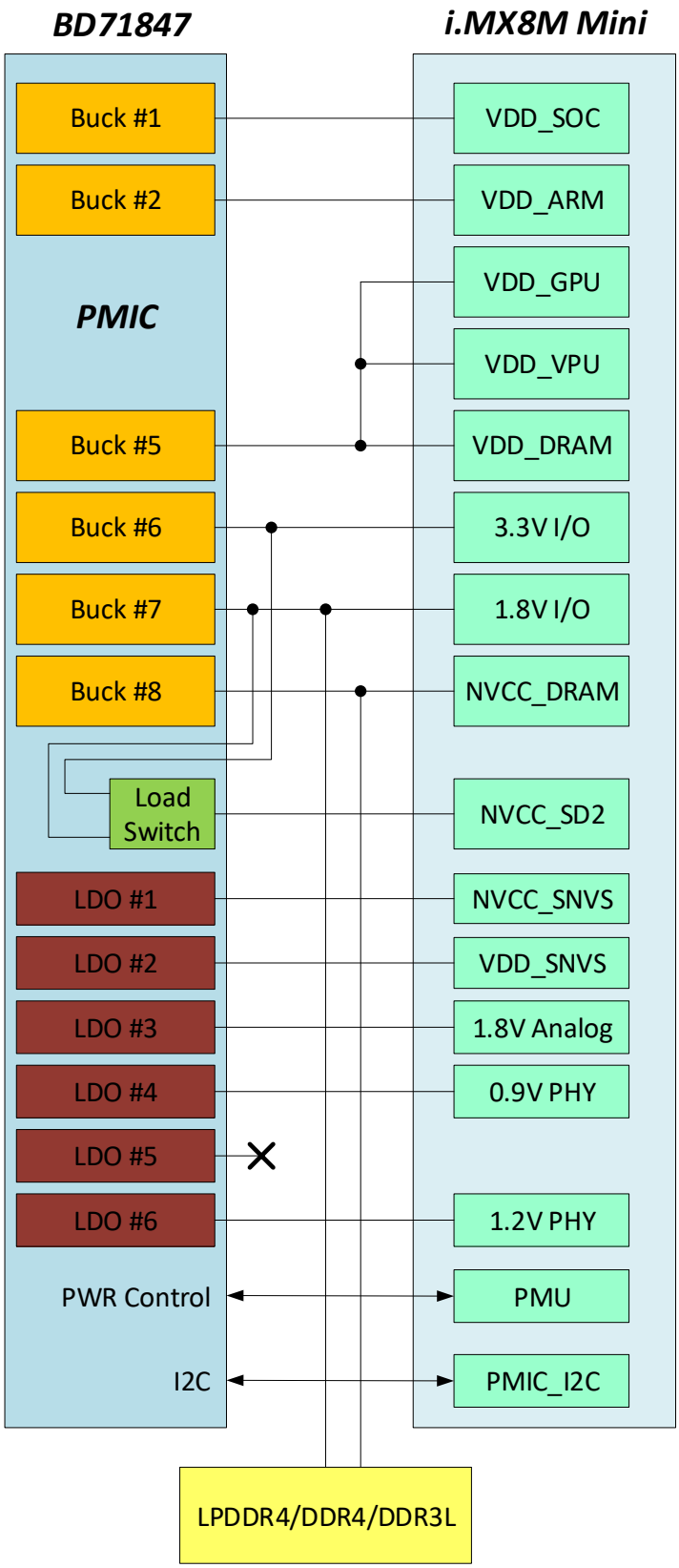

Figure 20. i.MX 8M Mini development platform power distribution block diagram

3.6.2. Power routing/distribution requirements

The designing for a good Power Delivery Network (PDN) is complicated. It includes:

1. Choose a good PCB stack-up (adequate Cu thicknesses, and layer assignments/utilization).
2. Optimize the placement and routing of the PDN. This includes good placement of the decoupling capacitors and connecting them to the power ground planes with as short and wide a trace as possible (as the increased inductance of a longer etch will degrade the effectivity of the capacitor). Use the number/placement of capacitors on the NXP development platforms.
3. Optimize DC IR drop. This involves using very wide traces/plane fills to route high-current power nets and ensure an adequate number of vias on power net layer transitions. Neck down of fill areas should be minimized and current density minimized. The maximum DC IR drop on a board should be 2% (preferably 1%) of the voltage rail (i.e., on a 1.1V rail, the maximum voltage drop should be less than 0.022 V, preferably less than 0.011 V). See Table 34 for the DC IR drop requirement.
4. AC impedance check – the target impedance at different frequencies should be below specified values. See Table 35 for the impedance targets vs. frequency for specified power rail for the i.MX 8M Mini PCB design.

Table 34. i.MX 8M Mini DC IR drop requirements

Supply input	Nominal voltage (V)	Max current (mA)	IR drop target	Corresponding power path resistance requirement (mΩ)
VDD_ARM	0.85/0.95/1.0	2200	<2%	< 7.7
VDD_SOC	0.85	1000	<2%	< 17
VDD_DRAM&VPU&GPU	0.975	2500	<2%	< 7.8
NVCC_DRAM	1.1	1000	<2%	< 22

Table 35. i.MX 8M Mini PDN target impedance

Supply Input	< 20 MHz (mΩ)	20 - 100 MHz (mΩ)
VDD_ARM	36	170
VDD_SOC	24	117
VDD_DRAM&VPU&GPU	24	110
NVCC_DRAM	15	70

3.7. USB connectivity

The i.MX 8M Mini provides two complete USB2.0 interfaces and the following configurations (or any subset) are supported:

- Dedicated host or device using Type-A connector or Type-B connector;
- Dual role using Type-C connector.

To implement a USB Type-C interface (UFP, DFP, or DRP), external hardware must be added to manage the two configuration channel IOs (CC1 and CC2) as well as monitor the plug orientation.

See the NXP development platform schematic for an example USB Type-C implementation.

3.8. PCIE connectivity

The i.MX 8M Mini has one PCIE interface. There is a pair of pins with the name of PCIE _CLK_P/N. These pins are bi-directional which can either be used to feed 100 MHz reference clock to the PHY from external clock source, or to output an internal generated 100 MHz reference clock to PCIE connector or PCIE device.

On EVK, a PCIE clock generator chip (9FGV0241) is used to feed high-quality clock to both the PHY and connecter/device. If a PCIE clock generator is not available, use the internal clock of the chip. Note that the internal clock exhibits larger jitter than that from PCIE clock generator.

3.9. Unused input/output terminations

3.9.1. i.MX 8M Mini unused input/output guidance

For the i.MX 8M Mini, the I/Os and power rails of an unused function can be terminated to reduce overall board power. Table 36 lists connectivity examples for unused power supply rails and Table 37 list connectivity examples for unused signal contacts/interfaces.

Table 36. i.MX 8M Mini unused power rail strapping recommendations

Function	Ball name	Recommendation if unused
MIPI-CSI & MIPI-DSI	VDD_MIPI_1P8, VDD_MIPI_1P2, VDD_MIPI_0P9	Leave unconnected[1]
PCIe	VDD_PCI_1P8, VDD_PCI_0P8	Leave unconnected
USB	VDD_USB_3P3, VDD_USB_1P8, VDD_USB_0P8	Leave unconnected[2]
VPU	VDD_VPU	Leave unconnected
GPU	VDD_GPU	Leave unconnected
Digital I/O supplies	NVCC_CLK, NVCC_ECSPI, NVDD_ENET, NVCC_GPIO1, NVCC_I2C, NVCC_JTAG, NVCC_NAND, NVCC_SAI1, NVCC_SAI2, NVCC_SAI3, NVCC_SAI5, NVCC_SD1, NVCC_SD2, NVCC_UART, NVCC_SNVS_1P8, PVCC0_1P8, PVCC1_1P8, PVCC2_1P8	All digital I/O supplies listed in this table must be powered under normal conditions whether the associated I/O pins are in use or not, and associated I/O pins need to enable pull in pad control register to limit any floating gate current.

1. These balls supply both MIPI-CSI and MIPI-DSI interfaces and must be connected/powered if either is used.
2. These balls supply all the USB interfaces (USB1, USB2) and must be connected/powered if any USB port is used.

Table 37. i.MX 8M Mini unused signal strapping recommendations

Function	Ball name	Recommendation if unused
MIPI-CSI	MIPI_CSI_CLK_P/N, MIPI_CSI_Dx_P/N	Tie all signals to ground
MIPI-DSI	MIPI_DSI_CLK_P/N, MIPI_DSI_Dx_P/N, MIPI_VREG_CAP	Leave unconnected
PCIe	PCIE_TXN_P/N, PCIE_RXN_P/N, PCIE_CLK_P/N, PCIE_RESREF	Leave unconnected
USB1	USB1_VBUS, USB1_DN/DP, USB1_ID, USB1_TXRTUNE	Leave unconnected
USB2	USB2_VBUS, USB2_DN/DP, USB2_ID, USB2_TXRTUNE	Leave unconnected

4. Avoiding board bring-up problems

4.1. Introduction

This chapter describes how to avoid mistakes when bringing up a board for the first time. The recommendations below consist of basic techniques for detecting board issues and preventing/locating the three issues encountered: power, clocks, and reset.

4.2. Avoiding power pitfalls—current

Excessive current can damage the board. Use a current-limiting laboratory supply set to the expected main current draw (at most). Monitor the main supply current with an ammeter when powering up the board for the first time. You can use the supply's internal ammeter if there is. By monitoring the main supply current and controlling the current limit, any excessive current can be detected before permanent damage occurs.

Before the board test, you can ohm out the board power rails to the ground to verify that there are no short circuits. Then, you can power on the board and there will not be any damage to the board and/or components.

4.3. Avoiding power pitfalls—voltage

To avoid incorrect voltage rails, create a basic table called a voltage report prior to board bring up/testing. The table helps to validate that all the supplies are reaching the expected levels.

To create a voltage report, list the following:

- Board voltage sources
- Default power-up values for the board voltage sources
- Best location on the board to measure the voltage level of each supply

Determine the best measurement location for each power supply to avoid a large voltage drop (IR drop) on the board. The drop causes inaccurate voltage values. The following guidelines help produce the best voltage measurements:

- Measure closest to the load (in the case of the i.MX 8M Mini processor).
- Make two measurements: the first after initial board power-up and the second while running a heavy use-case that stresses the i.MX 8M Mini processor.

Ensure that the i.MX 8M Mini power supply meets the DC electrical specifications as listed in the chip-specific data sheet. See Table 38 for a sample voltage report table.

NOTE

This report table is for the i.MX 8M Mini EVK board. Sample voltage reports for customer PCBs will be different from this, depending on the Processor and Power Management IC (PMIC) used and the assignment of the PMIC power resources.

Table 38. Sample voltage report table

Source	Net name	Expected (V)	Measured (V)	Measure point	Comment
DC jack input	VSYS	5	-	C703.1	Main supply for board
BD71847_BUCK1	VDD_SOC_0V8	0.85[1]	-	TP22	-
BD71847_BUCK2	VDD_ARM_0V9	0.85/0.95/1.0[2]	-	TP23	-
BD71847_BUCK5	VDD_DRAM&PU_0V9	0.975[3]	-	TP24	-
BD71847_BUCK6	VDD_3V3/NVCC_3V3	3.3	-	TP25	-
BD71847_BUCK7	VDD_1V8/NVC_1V8	1.8	-	TP26	-
BD71847_BUCK8	NVCC_DRAM_1V1	1.1/1.2/1.35[4]	-	TP27	-
BD71847_LDO1	NVCC_SNVS_1V8	1.8	-	TP28	-
BD71847_LDO2	VDD_SNVS_0V8	0.8	-	TP29	-
BD71847_LDO3	VDDA_1V8	1.8	-	TP32	-
BD71847_LDO4	VDD_PHY_0V9	0.9	-	TP30	-
BD71847_LDO6	VDD_PHY_1V2	1.2	-	TP31	-
BD71847_MUXSW	NVCC_SD2	3.3/1.8	-	TP33	Can be either under SW control

1. The default output voltage of BD71847 BUCK1 is 0.8 V. The software will change it to 0.85 V in SPL before DDR initialization.
2. The default output voltage of BD71847 BUCK2 is 0.9 V. The software will change it to 0.85 V for 1.2 GHz operation, 0.95 V for 1.6 GHz, 1.0 V for 1.8 GHz.
3. The default output voltage of BD71847 BUCK5 is 0.9 V. The software will change it to 0.975 V (BD71847 BUCK5 does not support 0.95 V output) in SPL before DDR initialization.
4. 1.1V for LPDDR4, 1.2V for DDR4, 1.35V for DDR3L, BD71847_BUCK8 default output voltage is 1.1V. Software will change it to the required value in SPL before DDR initialization

4.4. Checking for clock pitfalls

Problems with the external clocks are another board bring-up issue. Ensure that all the clock sources are running as expected.

The 24M_XTALI/24M_XTALO, and the RTC clocks are the main clock sources for 24 MHz and 32.768 kHz reference clocks. Although not required, the use of low jitter external oscillators to feed CLK1_P/N can be an advantage if low jitter or special frequency clock sources are required by modules driven by CLKIN_1/2. See the CCM chapter in the i.MX 8M Mini chip reference manual for details.

When checking crystal frequencies, using an active probe is recommended to avoid excessive loading. A passive probe might inhibit the 24 MHz oscillators from starting up. Use the following guidelines:

- RTC clock is running at 32.768 kHz.
- 24M_XTALI/24M_XTALO is running at 24 MHz (used for the PLL reference).

4.5. Avoiding reset pitfalls

Follow these guidelines to ensure that you are booting correctly.

- During initial power-on while asserting the POR_B reset signal, ensure that 24 MHz and 32.768 kHz clock is active before releasing POR_B.
- Follow the recommended power-up sequence specified in the i.MX 8M Mini data sheet.

- Ensure the POR_B signal remains asserted (low) until all voltage rails associated with bootup are ON.

The SAI_TXD[0:7], SAI_RXD[0:7], BOOT_MODE[0:1] balls and internal fuses control boot. For a more detailed description about the boot modes, see the system boot chapter in the chip reference manual.

4.6. Sample board bring-up checklist

The checklist incorporates the recommendations described in the previous sections. Blank cells should be filled in during the bring-up.

Table 39. Board bring-up checklist

Checklist item	Details	Owner	Findings &Status
Note: The following items must be completed serially.			
1. Perform a visual inspection	Check major components to make sure nothing has been misplaced or rotated before powering ON.		
2. Verify all i.MX 8M Mini voltage rails	Confirm that the voltages match the data sheet's requirements. Be sure to check voltages as close to the i.MX 8M Mini as possible (like on a bypass capacitor). This reveals any IR drops on the board that could cause issues later. Ideally, all the i.MX 8M Mini voltage rails should be checked, but see guidance below for important rails to check for the i.MX 8M Mini.		
	VDD_SNVS, NVCC_SNVS, VDD_SOC, VDD_ARM, VDD_DRAM, NVCC_DRAM are particularly important voltages, and must fall within the parameters provided in the i.MX 8M Mini data sheet.		
3. Verify power-up sequence	Verify that power on reset (POR_B) is deserted (high) after all power rails have come up and are stable. See the i.MX 8M Mini data sheet for details about power-up sequencing.		
4. Measure/probe input clocks (32.768 kHz, 24 MHz, others)	Without proper clocks, the i.MX 8M Mini will not function correctly.		
5. Check JTAG connectivity	This is one of the most fundamental and basic access points to the i.MX 8M Mini to allow the debug and execution of low level code, and probe/access processor memory.		
Note: The following items may be worked on in parallel with other bring-up tasks.			
Access internal RAM	Verify basic operation of the i.MX 8M Mini in system. The on-chip internal RAM starts at address 0x0090 0000 and is 128 Kbytes in density. Perform a basic test by performing a write-read-verify operation to the internal RAM. No software initialization is required to access internal RAM.		
Verify CLKO outputs (measure and verify default clock frequencies for desired clock output options) if the board design supports the probing of clock output balls.	This ensures that the corresponding clock is working and that the PLLs are working. This step requires chip initialization, for example, via the JTAG debugger, to properly set up the IOMUX to output clocks to I/O balls and to set up the clock control module to output the desired clock. See the chip reference manual for more details.		
Measure boot mode frequencies. Set the boot configure switch for each boot mode and measure the following	This verifies the connectivity of signals between the i.MX 8M Mini and boot device and that the boot mode signals are properly set. See the "System Boot" chapter in the chip reference manual for details for boot mode configurations.		

Table 39. Board bring-up checklist

Checklist item	Details	Owner	Findings &Status
(depending on system availability): • NAND (probe CE to verify boot, measure RE frequency) • SPI-NOR (probe slave select and measure clock frequency) • MMC/SD (measure clock frequency)			
Run basic DDR initialization and test memory	1. Assuming the use of a JTAG debugger, run the DDR initialization and open a debugger memory window pointing to the DDR memory map starting address. 2. Try writing a few words and verify if they can be read correctly. 3. If not, recheck the DDR initialization sequence and whether the DDR has been correctly soldered onto the board. Users should recheck the schematic to ensure that the DDR memory has been connected to the i.MX 8M Mini correctly.		

5. Using BSDL for board-level testing

5.1. BSDL overview

The Boundary Scan Description Language (BSDL) is used for board-level testing after the components are assembled. The interface for this test uses the JTAG pins. The definition is contained within IEEE Std 1149.1.

5.2. How BSDL works

A BSDL file defines the internal scan chain, which is the serial linkage of the IO cells, within a particular device. The scan chain looks like a large shift register, which provides a means to read the logic level applied to a pin or to output a logic state on that pin. Using JTAG commands, the test tool uses the BSDL file to control the scan chain so that device-board connectivity can be tested.

For example, when using an external ROM test interface, the test tool does the following:

1. It outputs a specific set of addresses and controls to the pins connected to the ROM.
2. It performs a read command and scans out the values of the ROM data pins.
3. It compares the values read with the known golden values.

Based on this procedure, the tool determines whether the interface between the two parts is connected properly and does not contain shorts or opens.

5.3. Downloading the BSDL file

The BSDL file for each i.MX processor is stored at the NXP website upon product release. Contact your local sales office or field applications engineer to check the availability of information before product releases.

5.4. Pin coverage of BSDL

Each pin is defined as a port within the BSDL file. You can open the file with a text editor (such as Wordpad) to review how each pin functions. The BSDL file defines these functions:

```
-- PORT DESCRIPTION TERMS
-- in         = input only
-- out        = three-state output (0, Z, 1)
-- buffer     = two-state output (0, 1)
-- inout      = bidirectional

-- linkage    = OTHER (vdd, vss, analog)
```

The appearance of a “linkage” in a pin’s file means that the pin cannot be used with a boundary scan. These are usually power pins or analog pins that cannot be defined by a digital logic state.

5.5. Boundary scan operation

The boundary scan operation is controlled by:

- BOOT_MODE0, BOOT_MODE1, and JTAG_MOD pins.
- On-chip Fuse bits.

The JTAG_MOD pin state controls the selection of the JTAG to the core logic or boundary scan operation. See the following references for further information:

- The “System JTAG Controller (SJC)” chapter in the chip reference manual for the definitions of the JTAG interface operations.
- The “JTAG Security Modes” section in the same chapter for an explanation of the operation of the e-Fuse bit definitions in Table 40.
- The “Fusemap” chapter in the chip reference manual for the fusemap tables.

Table 40. System considerations for BSDL

Pin name	Logic state	Description
JTAG_MOD	1	IEEE 1149.1 JTAG compliant mode
BOOT_MODE[1:0]	[0:0] [0:1] [1:0] [1:1]	Boot From Fuses Serial Downloader Internal Boot (Development) Reserved for Boundary Scan
POR_B	1	Power On Reset for the device
e-Fuse bits		
JTAG_SMODE[1:0]	[0:0] [0:1]	JTAG enable mode Secure JTAG mode
SJC_DISABLE	0	Secure JTAG Controller is enabled

NOTE

When using the BSDL file to force the i.MX8MM enter the boundary scan mode on the 8MMINILPD4 EVK:

1. COMPLIANCE_PATTERNS of IMX8MM: entity is "(BOOT_MODE0, BOOT_MODE1, JTAG_MOD, TEST_MODE) (1101)". BOOT_MODE0(G26)/ BOOT_MODE1(G27) & TEST_MODE(D26) should be high. Set the SWITCH SW1101 [1-10]: 1111110001.
2. GPIO1_IO02 is used as WDOG_B in the EVK board design. This PIN should add 4.7-kΩ pull-up to NVCC_GPIO1 (install R106). Without the 4.7-kΩ pull-up resistor, this pin is floating when entering the boundary scan mode and may cause system reboot due to the watchdog RESET.
3. In the BSDL file, XTALI_24M(B27)/XTALO_24M(B25) “PIN Name” does not match the datasheet because the JTAG1149 specification does not allow a number as the first character. The “PIN Name” is an inversion in the BSDL file.

5.6. I/O pin power considerations

The boundary scan operation uses each of the available device pins to drive or read values within a given system. Therefore, the power supply pin for each specific module must be powered for the IO buffers to operate. This is straightforward for the digital pins within the system.

NOTE

The BSDL was only tested at 1.8 V.

6. Revision history

Table 41. Revision history

Revision number	Date	Substantive changes
0	02/2019	Initial release.
1	08/2019	Added Section 5, “Using BSDL for board-level testing”. Updated design recommendations for PMIC, QSPI, and JTAG in Section 2.1, “Design checklist table”.

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