18×8 DOTS MATRIX LED DRIVER

October 2018

GENERAL DESCRIPTION

The IS31FL3745 is a general purpose 18×n (n=1~8) LED Matrix programmed via 1MHz I2C compatible interface. Each LED can be dimmed individually with 8-bit PWM data and 8-bit DC scaling data which allowing 256 steps of linear PWM dimming and 256 steps of DC current adjustable level.

Additionally each LED open and short state can be detected, IS31FL3745 store the open or short information in Open-Short Registers. The Open-Short Registers allowing MCU to read out via I2C compatible interface. Inform MCU whether there are LEDs open or short and the locations of open or short LEDs.

The IS31FL3745 operates from 2.7V to 5.5V and features a very low shutdown and operational current.

IS31FL3745 is available in WLCSP-36 (2.93mm×2.93mm, 0.5mm ball pitch, 0.25mm ball diameter) package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +125°C.

FEATURES

- Supply voltage range: 2.7V to 5.5V
- 18 Current sink (Maximum)
- Support 18 × n (n=1~8) LED matrix configurations
- Individual 256 PWM control steps
- Individual 256 DC current steps
- Global 256 current setting
- SDB rising edge reset I2C module
- Programmable H/L logic:1.4/0.4, 2.4/0.6
- 29kHz PWM frequency
- 1MHz I2C-compatible interface
- State lookup registers
- Individual open and short error detect function
- 180 degree phase delay operation to reduce power noise
- De-Ghost
- Cascade for synchronization of chips
- WLCSP-36 (2.93mm×2.93mm, 0.5mm ball pitch, 0.25mm ball diameter) package

APPLICATIONS

- AI-speakers and smart home devices
- LED display for hand-held devices

TYPICAL APPLICATION CIRCUIT

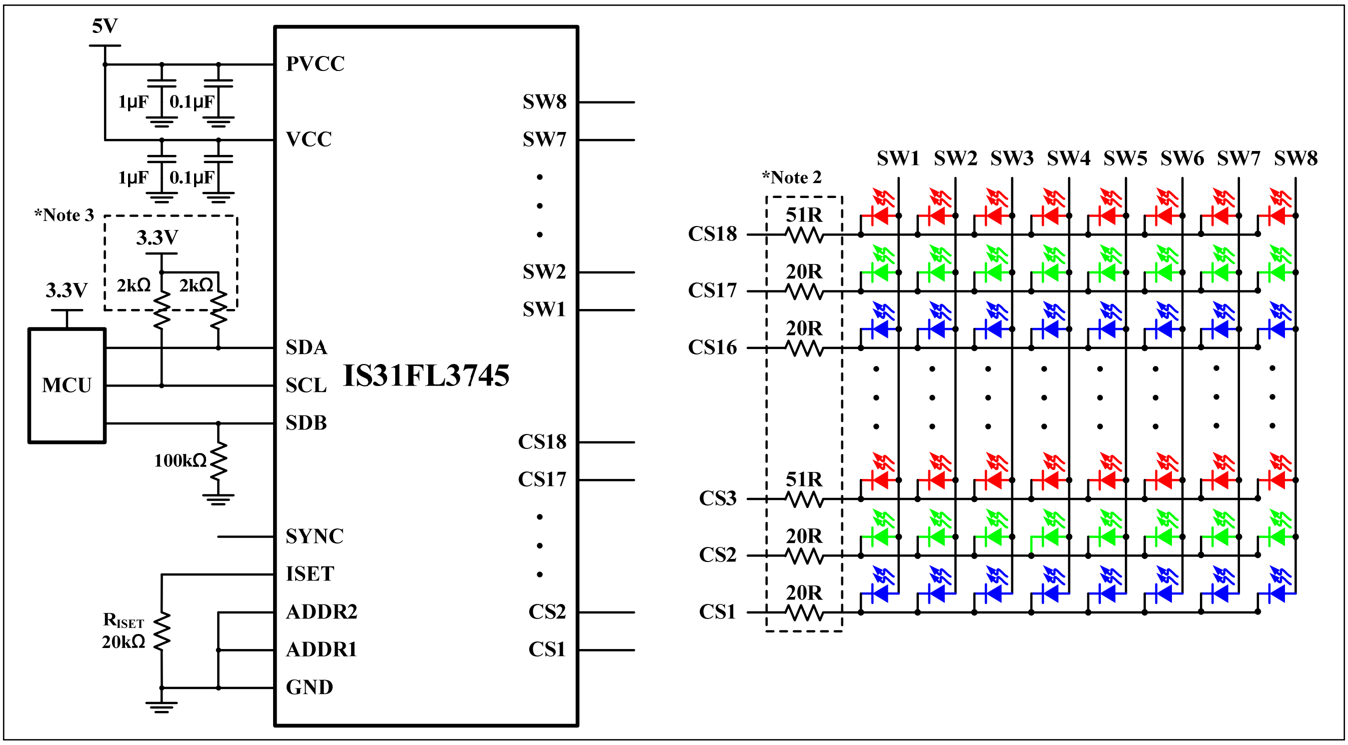


Figure 1 Typical Application Circuit: 48 RGBs

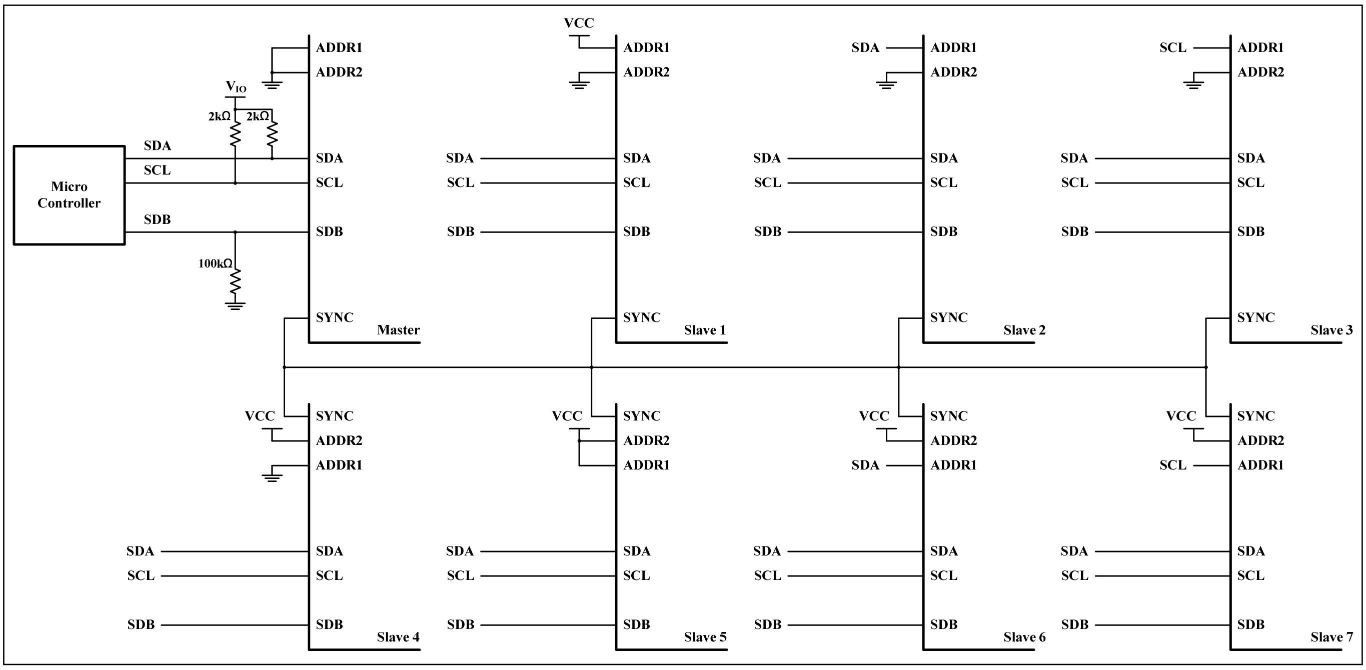


Figure 2 Typical Application Circuit (Eight Parts Synchronization-Work)

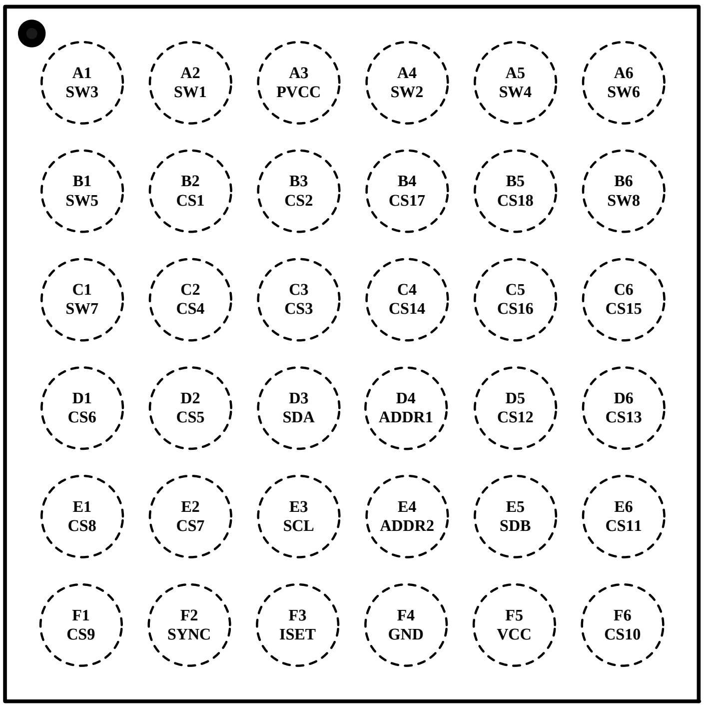
Note 1: IC should be placed far away from the antenna in order to prevent the EMI.

Note 2: The 20R between LED and IC is only for thermal reduction, for mono red LED, if $PV_{CC}=V_{CC}$=3.3V, don't need these resistors.

Note 3: The VIH of I2C bus should be smaller than VCC. And if VIH is lower than 3.0V, it is recommended add a level shift circuit to avoid extra shutdown current.

Note 4: One system should contain only one master, all slave parts should be configured as slave mode before the master is configured as master mode. Work as master mode or slave mode specified by Configuration Register (SYNC bits, register 25h, Page 2). Master part output master clock, and all the other parts which work as slave input this master clock.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
WLCSP-36	

PIN DESCRIPTION

No.	Pin	Description
A1, A2	SW3,SW1	Power SW.
A3	PVCC	Power for current source.
A4~A6,B1	SW2,SW4,SW6,SW5	Power SW.
B2~B5	CS1,CS2,CS17,CS18	Current sink pin for LED matrix.
B6, C1	SW8,SW7	Power SW.
C2~C6,D1,D2	CS4,CS3,CS14,CS16, CS15,CS6,CS5	Current sink pin for LED matrix.
D3	SDA	I2C compatible serial data.
D4, E4	ADDR1, ADDR2	I2C address select pin.
D5,D6,E1,E2	CS12,CS13,CS8,CS7	Current sink pin for LED matrix.
E3	SCL	I2C compatible serial clock.
E5	SDB	Shutdown pin.
E6,F1	CS11,CS9	Current sink pin for LED matrix.
F2	SYNC	System clock output/input.
F3	ISET	Set the maximum IOUT current.
F4	GND	Power GND and analog GND.
F5	VCC	Power for digital circuits.
F6	CS10	Current sink pin for LED matrix.

ORDERING INFORMATION
Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS31FL3745-CLS4-TR	WLCSP-36, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~+6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~+150°C
Operating temperature range, T_A=T_J	-40°C ~ +125°C
Package thermal resistance, junction to ambient (4 layer standard test PCB based on JESD 51-2A), θ_{JA}	47.49°C/W
ESD (HBM) ESD (CDM)	±7kV ±1kV

Note 5: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{CC}= 3.6V, T_A= 25°C, unless otherwise noted.

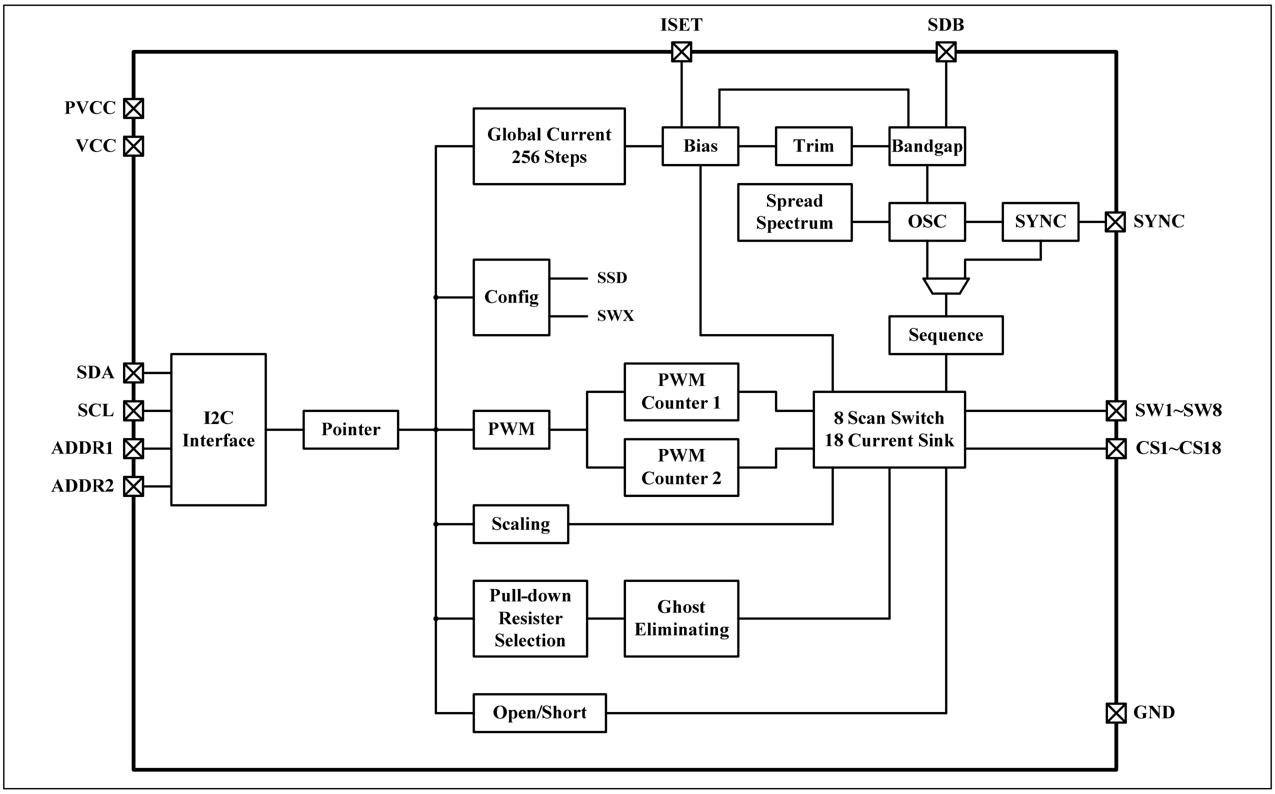
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent power supply current	V_{SDB}= $V_{CC,}$ all LEDs off		1.9	3	mA
I_{SD}	Shutdown current	V_{SDB}= 0V		1.3	2.5	μA
		V_{SDB}= V_{CC}, Configuration Register written “0000 0000 (Software SD)		1.3	2.5	
I_{OUT}	Maximum constant current of CSx	R_{ISET}= 10kΩ, GCC= 0xFF, SL= 0xFF	32.08	34.5	36.92	mA
I_{LED}	Average current on each LED I_{LED}= $I_{OUT(PEAK)}$×Duty (Duty=1/8.27)	R_{ISET}= 10kΩ, GCC= 0xFF, SL= 0xFF		4.21		mA
V_{HR}	Current switch headroom voltage SWx	I_{SWITCH}= 306mA, R_{ISET}= 10kΩ, GCC= 0x80, SL= 0xFF		250		mV
	Current sink headroom voltage CSx	I_{SINK}= 34mA, R_{ISET}= 10kΩ, GCC= 0xFF, SL= 0xFF (Note 6)		300		
t_{SCAN}	Period of scanning			33		μs
t_{NOL1}	Non-overlap blanking time during scan, the SWx and CSy are all off during this time			0.83		μs
t_{NOL2}	Delay total time for CS1 to CS 18, during this time, the SWx is on but CSx is not all turned on	(Note 6)		0.3		μs
Logic Electrical Characteristics (SDA, SCL, ADDR1, ADDR2, SDB)						
V_{IL}	Logic “0” input voltage	V_{CC}=2.7V, LGC=0			0.4	V
V_{IH}	Logic “1” input voltage	V_{CC}=5.5V, LGC=0	1.4			V
V_{HYS}	Input Schmitt trigger hysteresis	V_{CC}=3.6V, LGC=0		0.2		V
V_{IL}	Logic “0” input voltage	V_{CC}=2.7V, LGC=1			0.6	V
V_{IH}	Logic “1” input voltage	V_{CC}=5.5V, LGC=1	2.4			V
V_{HYS}	Input Schmitt trigger hysteresis	V_{CC}=3.6V, LGC=1		0.2		V
I_{IL}	Logic “0” input current	V_{INPUT} = L (Note 6)		5		nA
I_{IH}	Logic “1” input current	V_{INPUT} = H (Note 6)		5		nA

DIGITAL INPUT SWITCHING CHARACTERISTICS (NOTE 6)

Symbol	Parameter	Fast Mode			Fast Mode Plus			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Serial-clock frequency	-		400	-		1000	kHz
t_{BUF}	Bus free time between a STOP and a START condition	1.3		-	0.5		-	μs
$t_{HD, STA}$	Hold time (repeated) START condition	0.6		-	0.26		-	μs
$t_{SU, STA}$	Repeated START condition setup time	0.6		-	0.26		-	μs
$t_{SU, STO}$	STOP condition setup time	0.6		-	0.26		-	μs
$t_{HD, DAT}$	Data hold time	-		-	-		-	μs
$t_{SU, DAT}$	Data setup time	100		-	50		-	ns
t_{LOW}	SCL clock low period	1.3		-	0.5		-	μs
t_{HIGH}	SCL clock high period	0.7		-	0.26		-	μs
t_R	Rise time of both SDA and SCL signals, receiving	-		300	-		120	ns
t_F	Fall time of both SDA and SCL signals, receiving	-		300	-		120	ns

Note 6: Guaranteed by design.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

I2C INTERFACE

When I2C/SPI=H, the IS31FL3745 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3745 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A1 and A2 are decided by the connection of the ADDRx pin.

Table 1 Slave Address:

ADDR2	ADDR1	A7:A5	A4:A3	A2:A1	A0
GND	GND	010	00	00	0/1
GND	SCL		00	01	
GND	SDA		00	10	
GND	VCC		00	11	
SCL	GND		01	00	
SCL	SCL		01	01	
SCL	SDA		01	10	
SCL	VCC		01	11	
SDA	GND		10	00	
SDA	SCL		10	01	
SDA	SDA		10	10	
SDA	VCC		10	11	
VCC	GND		11	00	
VCC	SCL		11	01	
VCC	SDA		11	10	
VCC	VCC		11	11	

ADDR1/2 connected to GND, (A2:A1)/(A4:A3)=00;

ADDR1/2 connected to VCC, (A2:A1)/(A4:A3)=11;

ADDR1/2 connected to SCL, (A2:A1)/(A4:A3)=01;

ADDR1/2 connected to SDA, (A2:A1)/(A4:A3)=10;

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 400kHz I2C with 4.7kΩ, 1MHz I2C with 1kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3745.

The timing diagram for the I2C is shown in Figure 3. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3745's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3745 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3745, the register address byte is sent, most significant bit first. IS31FL3745 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3745 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3745, load the address of the data register that the first data byte is intended for. During the IS31FL3745 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3745 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3745 (Figure 7).

READING OPERATION

Most of the registers can be read.

To read the FCh, FEh, after I2C start condition, the bus master must send the IS31FL3745 device address with the R/$\overline{W}$ bit set to "0", followed by the register address (FEh or F1h) which determines which register is accessed. Then restart I2C, the bus master should send the IS31FL3745 device address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3745 to the master (Figure 8).

To read the registers of Page 0 thru Page 3, the FDh should write with 00h before follow the Figure 8 sequence to read the data. That means, when you want to read registers of Page 0, the FDh should point to Page 0 first and you can read the Page 0 data.

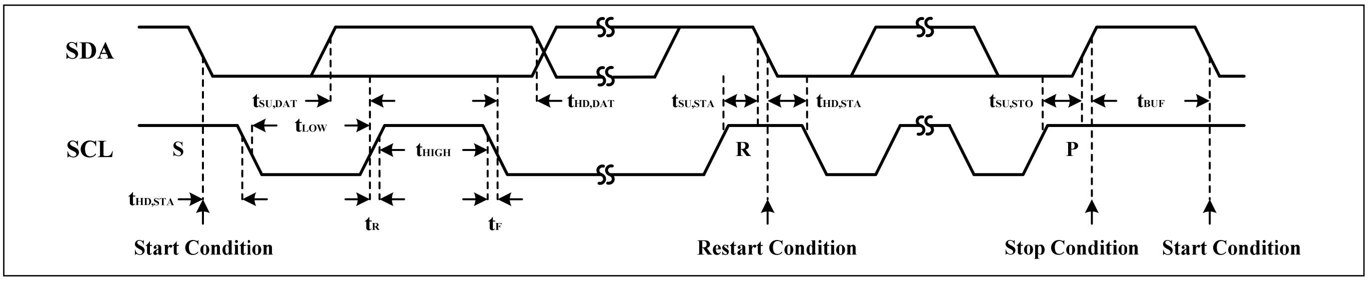


Figure 4 I2C Interface Timing

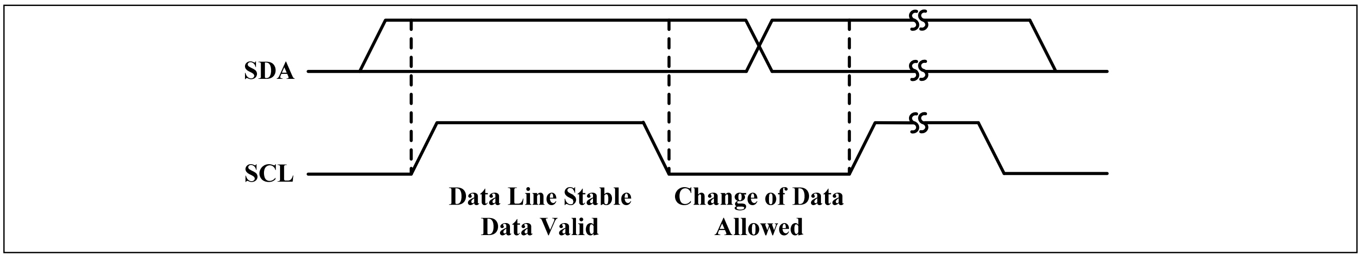


Figure 5 I2C Bit Transfer

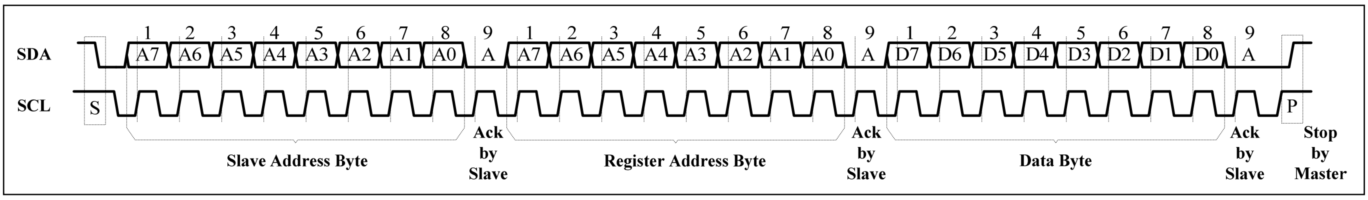


Figure 6 I2C Writing to IS31FL3745 (Typical)

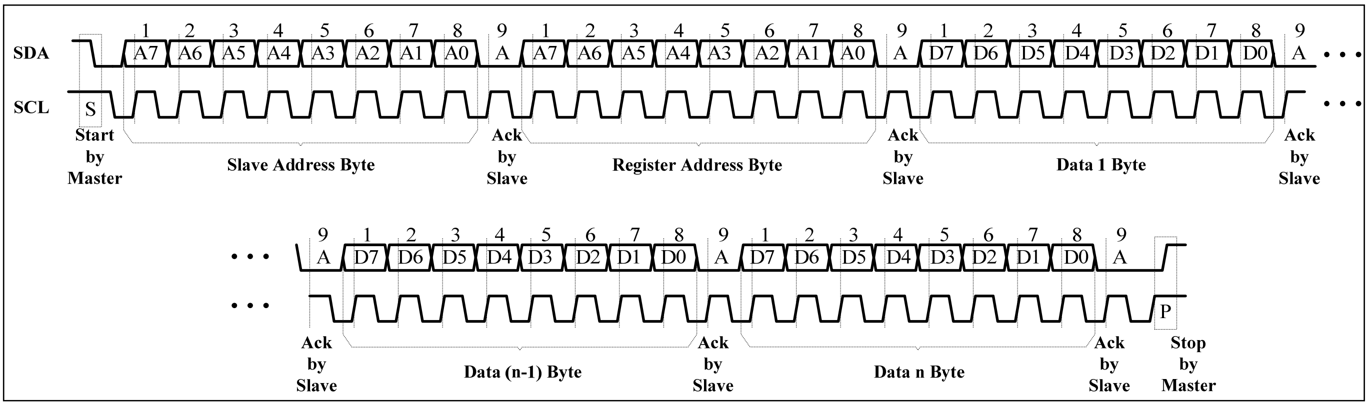


Figure 7 I2C Writing to IS31FL3745 (Automatic Address Increment)

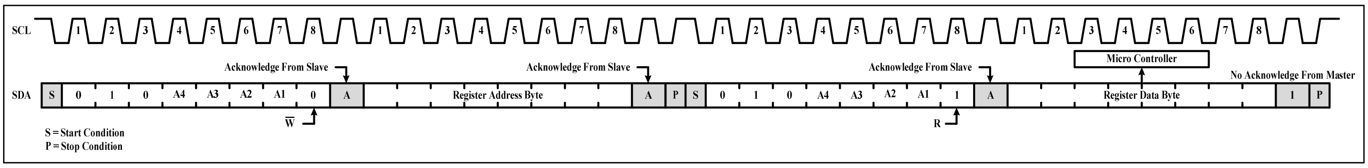


Figure 8 I2C Reading From IS31FL3745

Table 2 Command Register Definition

Address	Name	Function	Table	R/W	Default
FEh	Command Register Write lock	To unlock Command Register	4	R/W	0000 0000
FDh	Command Register	Available Page 0 to Page 2 Registers	3	W	xxxx xxxx
FCh	ID Register	For read the product ID only Read result is the slave address	-	R	Slave Address

REGISTER CONTROL

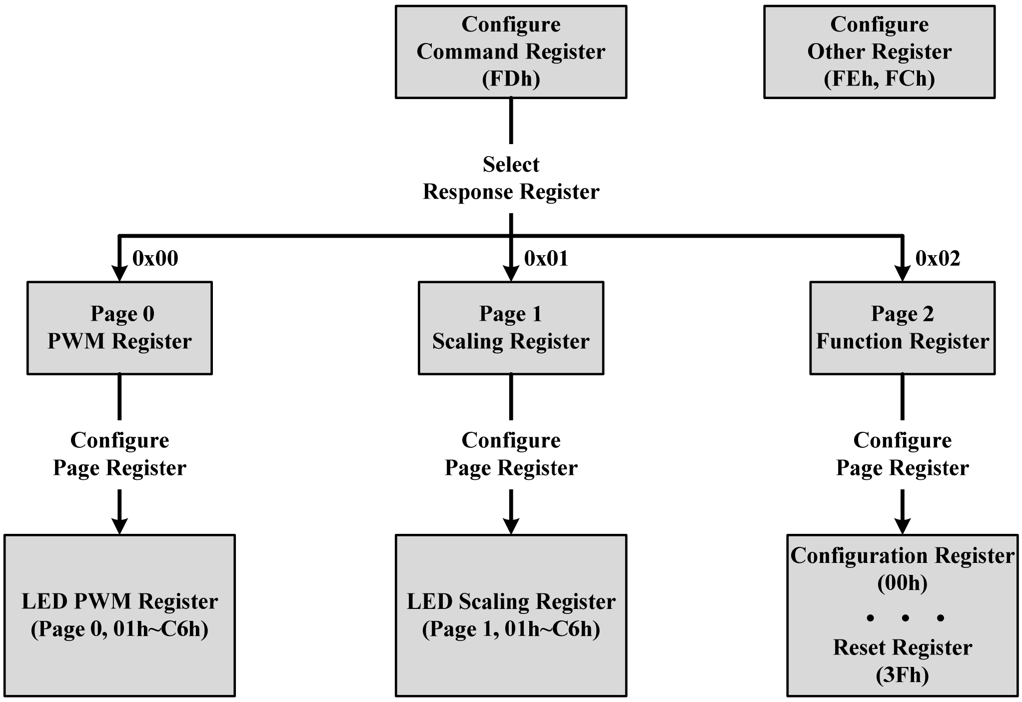


Table 3 FDh Command Register

Data	Function
0000 0000	Point to Page 0 (PG0, PWM Register is available)
0000 0001	Point to Page 1 (PG1, White balance Scaling Register is available)
0000 0010	Point to Page 2 (PG2, Function Register is available)
Others	Reserved

Note: FDh is locked when power up, need to unlock this register before write command to it. See Table 4 for detail.

The Command Register should be configured first after writing in the slave address to choose the available register. Then write data in the choosing register. Power up default state is “0000 0000”.

For example, when write “0000 0001” in the Command Register (FDh), the data which writing after will be stored in Page1 (PG1).

Table 4 FEh Command Register Write Lock (Read/Write)

Bit	D7:D0
Name	CRWL
Default	0000 0000 (FDh write disable)

To select the PG0~PG2, need to unlock this register first, with the purpose to avoid mis-operation of this register. When FEh is written with 0xC5, FDh is allowed to modify once, after the FDh is modified the FEh will reset to be 0x00 at once.

Table 5 Register Definition

Address	Name	Function	Table	R/W	Default
PG0 (0x00): PWM Register					
01h~90h	PWM Register	Set PWM for each LED	6	R/W	0000 0000
PG1 (0x01): LED Scaling					
01h~90h	Scaling Register	Set Scaling for each LED	7	R/W	0000 0000
PG2 (0x02): Function Register					
00h	Configuration Register	Configure the operation mode	9	R/W	0000 0000
01h	Global Current Control Register	Set the global current	10	R/W	0000 0000
02h	Pull Down/Up Resistor Selection Register	Set the pull down resistor for SWx and pull up resistor for CSy	11	R/W	0101 0101
03h~1Ah	Open/Short Register	Store the open or short information	12	R	0000 0000
24h	Temperature Status	Store the temperature point of the IC	13	R/W	0000 0000
25h	Spread Spectrum Register	Spread spectrum function enable	14	R/W	0000 0000
2Fh	Reset Register	Reset all register to POR state	-	W	0000 0000

Page 0 (PG0, FDh= 0x00): PWM Register

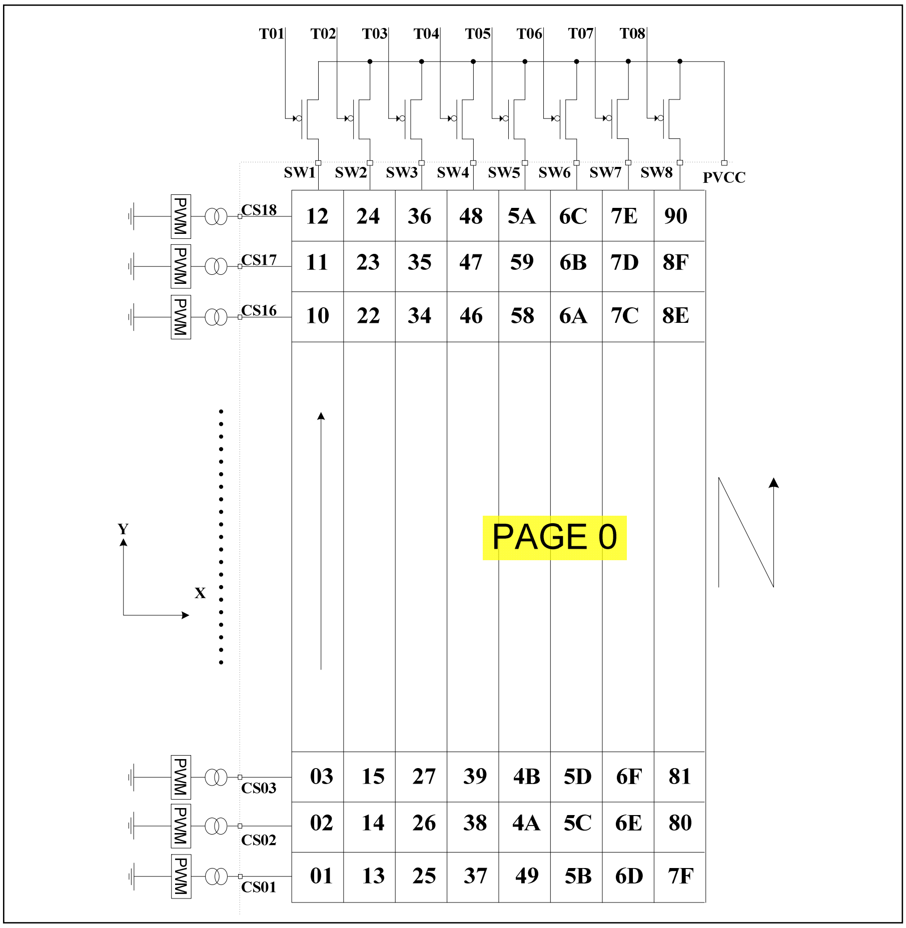


Figure 9 PWM Register

Table 6 PG0: 01h ~ 90h PWM Register

Bit	D7:D0
Name	PWM
Default	0000 0000

Each dot has a byte to modulate the PWM duty in 256 steps.

The value of the PWM Registers decides the average current of each LED noted I_{LED}.

I_{LED} computed by Formula (1):

$$I_{LED} = \frac{PWM}{256} \times I_{OUT(PEAK)} \times Duty \quad (1)$$

$$PWM = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Where Duty is the duty cycle of SWx,

$$Duty = \frac{33\mu s}{(33\mu s + 0.83\mu s + 0.3\mu s)} \times \frac{1}{8} = \frac{1}{8.27} \quad (2)$$

I_{OUT} is the output current of CSy (y=1~18),

$$I_{OUT(PEAK)} = \frac{343}{R_{ISET}} \times \frac{GCC}{256} \times \frac{SL}{256} \quad (3)$$

GCC is the Global Current Control register (PG2, 01h) value, SL is the Scaling Register value as Table 9 and R_{ISET} is the external resistor of ISET pin. D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if D7:D0=1011 0101 (0xB5, 181), GCC=1111 1111, R_{ISET}=10kΩ, SL=1111 1111:

$$I_{LED} = \frac{343}{10k\Omega} \times \frac{255}{256} \times \frac{255}{256} \times \frac{1}{8.27} \times \frac{181}{256}$$

Page 1 (PG1, FDh= 0x01): Scaling Register

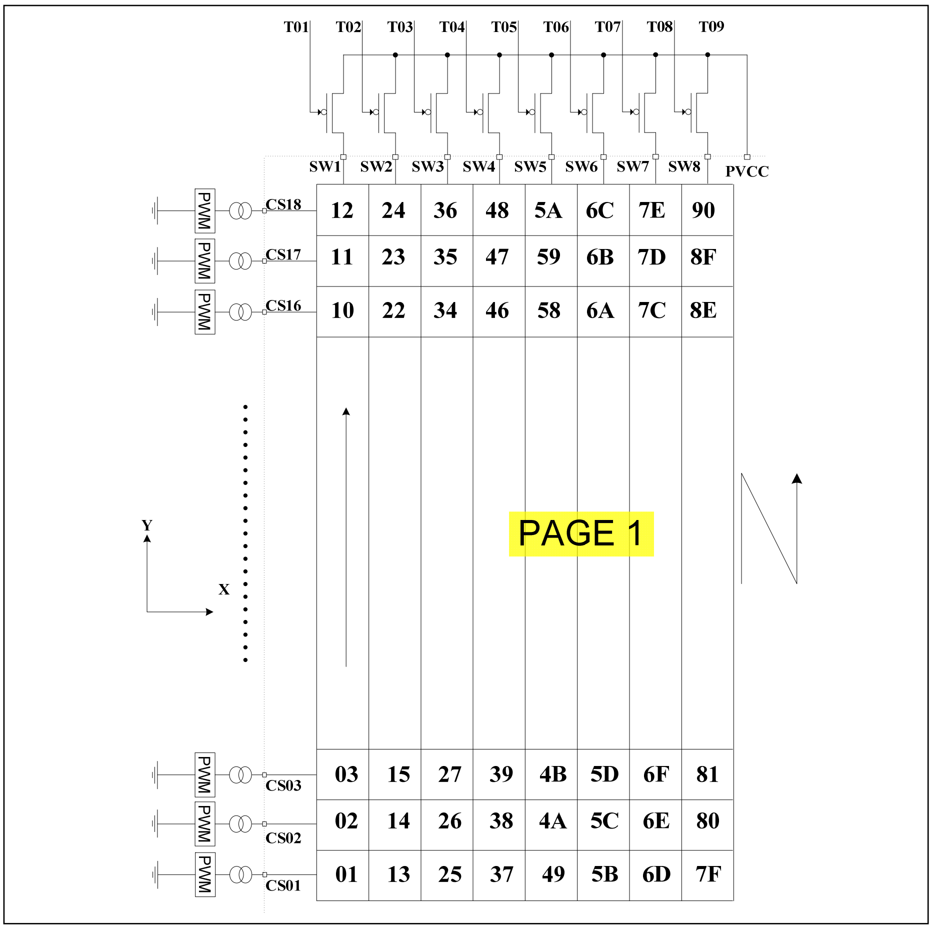


Figure 10 Scaling Register

Table 7 PG1: 01h ~ 90h Scaling Register

Bit	D7:D0
Name	SL
Default	0000 0000

Scaling register control the DC output current of each dot. Each dot has a byte to modulate the scaling in 256 steps.

The value of the Scaling Register decides the peak current of each LED noted $I_{OUT(PEAK)}$.

$I_{OUT(PEAK)}$ computed by Formula (3):

$$I_{OUT(PEAK)} = \frac{343}{R_{ISET}} \times \frac{GCC}{256} \times \frac{SL}{256} \quad (3)$$

$$SL = \sum_{n=0}^{7} D[n] \cdot 2^n$$

I_{OUT} is the output current of CSy (y=1~18), GCC is the Global Current Control Register (PG2, 01h) value and R_{ISET} is the external resistor of ISET pin. D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if R_{ISET}=10kΩ, GCC=1111 1111, SL=0111 1111:

$$SL = \sum_{n=0}^{7} D[n] \cdot 2^n = 127$$

$$I_{OUT} = \frac{343}{10k\Omega} \times \frac{255}{256} \times \frac{127}{256} = 16.8mA$$

$$I_{LED} = 16.8mA \times \frac{1}{8.27} \times \frac{PWM}{256}$$

Table 8 Page 2 (PG2, FDh= 0x02): Function Register

Register	Name	Function	Table	R/W	Default
00h	Configuration Register	Configure the operation mode	10	R/W	0000 0000
01h	Global Current Control Register	Set the global current	11	R/W	0000 0000
02h	Pull Down/Up Resistor Selection Register	Set the pull down resistor for SWx and pull up resistor for CSy	12	R/W	0101 0101
03h~1Ah	Open/Short Register	Store the open or short information	13	R	0000 0000
24h	Temperature Status	Store the temperature point of the IC	14	R/W	0000 0000
25h	Spread Spectrum Register	Spread spectrum function enable	15	R/W	0000 0000
2Fh	Reset Register	Reset all register to POR state	-	W	0000 0000

Table 9 00h Configuration Register

Bit	D7:D4	D3	D2:D1	D0
Name	SWS	LGC	OSDE	SSD
Default	0000	0	00	0

The Configuration Register sets operating mode of IS31FL3745.

SSD Software Shutdown Control
0 Software shutdown
1 Normal operation

OSDE Open Short Detection Enable
00 Disable open/short detection
01/11 Enable open detection
10 Enable short detection

LGC H/L Logic
0 1.4V/0.4V
1 2.4V/0.6V

SWS SWx Setting
0000 1/11 (default, not recommend)
0001 SW1~SW8, 1/10, (not recommend)
0010 SW1~SW8, 1/9, (not recommend)
0011 SW1~SW8, 1/8
0100 SW1~SW7, 1/7, SW8 no-active
0101 SW1~SW6, 1/6, SW7~SW8 no-active
0110 SW1~SW5, 1/5, SW6~SW8 no-active
0111 SW1~SW4, 1/4, SW5~SW8 no-active
1000 SW1~SW3, 1/3, SW4~SW8 no-active
1001 SW1~SW2, 1/2, SW3~SW8 no-active
1010 All CSx work as current sinks only, no scan
Others Not allowed

When OSDE set to "01", open detection will be trigger once, the user could trigger open detection again by set OSDE from "00" to "01".

When OSDE set "10", short detection will be trigger once, the user could trigger short detection again by set OSDE from "00" to "10".

When SSD is "0", IS31FL3745 works in software shutdown mode and to normal operate the SSD bit should set to "1".

SWS control the duty cycle of the SW, default mode is 1/11.

Table 10 01h Global Current Control Register

Bit	D7:D0
Name	GCC
Default	0000 0000

The Global Current Control Register modulates all CSy (x=1~18) DC current which is noted as I_{OUT} in 256 steps.

I_{OUT} is computed by the Formula (3):

$$I_{OUT(PEAK)} = \frac{343}{R_{ISET}} \times \frac{GCC}{256} \times \frac{SL}{256} \tag{3}$$

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

Table 11 02h Pull Down/Up Resistor Selection Register

Bit	D7	D6:D4	D3	D2:D0
Name	PHC	SWPDR	-	CSPUR
Default	0	011	0	011

Set pull down resistor for SWx and pull up resistor for CSy.

PHC Phase choice
0 0 degree phase delay
1 180 degree phase delay

SWPDR SWx Pull down Resistor Selection Bit
000 No pull down resistor
001 0.5kΩ only in SWx off time
010 1.0kΩ only in SWx off time
011 2.0kΩ only in SWx off time
100 1.0kΩ all the time
101 2.0kΩ all the time
110 4.0kΩ all the time
111 8.0kΩ all the time

CSPUR CSy Pull up Resistor Selection Bit
000 No pull up resistor
001 0.5kΩ only in CSx off time
010 1.0kΩ only in CSx off time
011 2.0kΩ only in CSx off time
100 1.0kΩ all the time
101 2.0kΩ all the time
110 4.0kΩ all the time
111 8.0kΩ all the time

Table 12 Open/Short Register (Read Only)
03h~1Ah Open/Short Information

Bit	D7:D6	D5:D0
Name	-	CS18:CS13, CS12:CS07,CS06:CS01
Default	00	00 0000

When OSDE (PG2, 00h) is set to “01”, open detection will be trigger once, and the open information will be stored at 03h~1Ah.

When OSDE (PG2, 00h) set to “10”, short detection will be trigger once, and the short information will be stored at 03h~1Ah.

Before set OSDE, the GCC should set to 0x01.

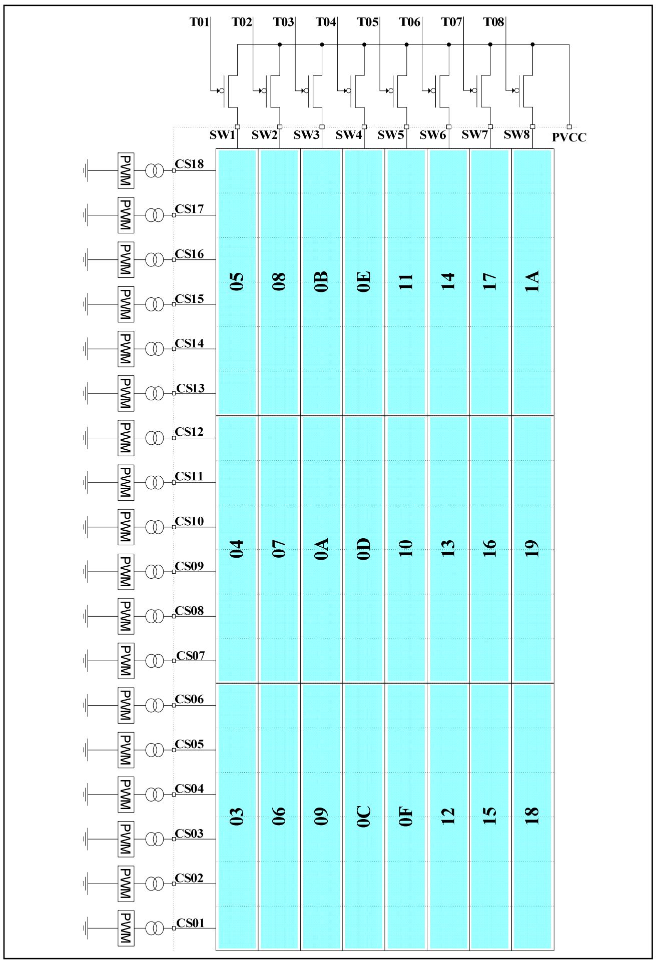


Figure 11 Open/Short Register

Table 13 24h Temperature Status

Bit	D7:D4	D3:D2	D1:D0
Name	-	TS	TROF
Default	0000	00	00

TS store the temperature point of the IC. If the IC temperature reaches the temperature point the IC will trigger the thermal roll off and will decrease the current as TROF set percentage.

TROF percentage of output current
00 100%
01 75%
10 55%
11 30%

TS Temperature Point, Thermal roll off start point
00 140°C
01 120°C
10 100°C
11 90°C

Table 14 25h Spread Spectrum Register

Bit	D7:D6	D4	D3:D2	D1:D0
Name	SYNC	SSP	RNG	CLT
Default	00	0	00	00

When SYNC bits are set to “11”, the IS31FL3745 is configured as the master clock source and the SYNC pin will generate a clock signal distributed to the clock slave devices. To be configured as a clock slave device and accept an external clock input the slave device’s SYNC bits must be set to “10”.

When SSP enable, the spread spectrum function will be enabled and the RNG & CLT bits will adjust the range and cycle time of spread spectrum function.

SYNC Enable of SYNC function
0x Disable SYNC function, about 30kΩ pull-low
10 Slave, clock input
11 Master, clock output

SSP Spread spectrum function enable
0 Disable
1 Enable

RNG Spread spectrum range
00 ±5%
01 ±15%
10 ±24%
11 ±34%

CLT Spread spectrum cycle time
00 1980μs
01 1200μs
10 820μs
11 660μs

2Fh Reset Register

Once user writes the Reset Register with 0xAE, IS31FL3745 will reset all the IS31FL3745 registers to their default value. On initial power-up, the IS31FL3745 registers are reset to their default values for a blank display.

APPLICATION INFORMATION

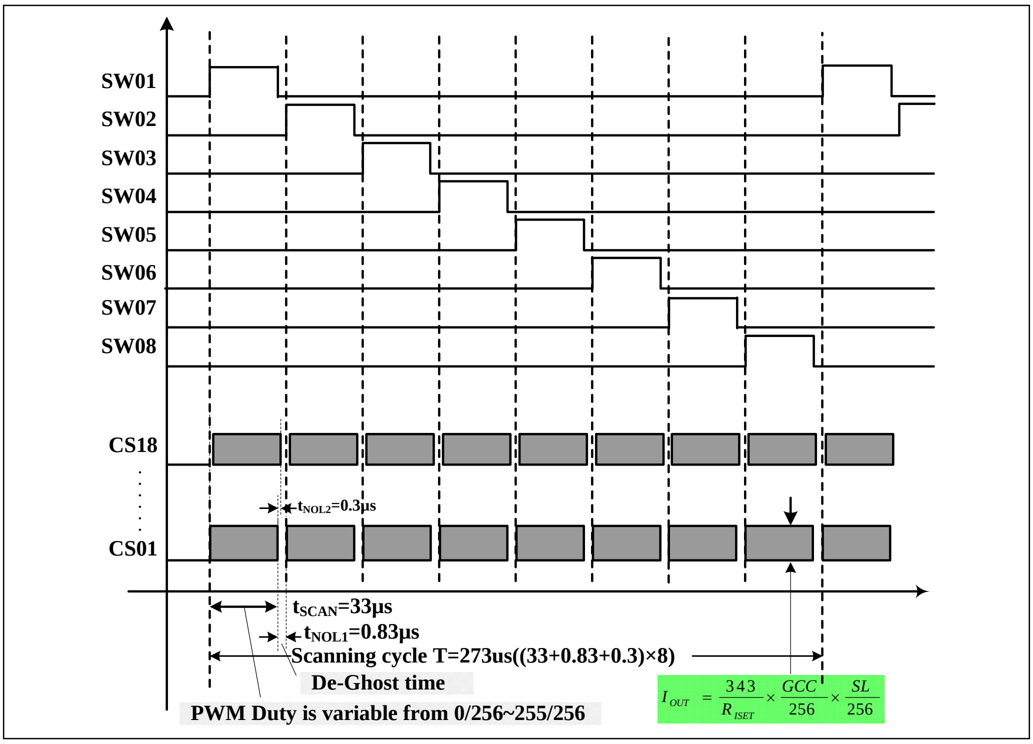


Figure 12 Scanning Timing

SCANING TIMING

As shown in Figure 12, the SW1~SW8 is turned on by serial, LED is driven 8 by 8 within the SWx (x=1~8) on time (SWx, x=1~8 is source and it is high when LED on) , including the non-overlap blanking time during scan, the duty cycle of SWx (active high, x=1~8) is:

$$Duty = \frac{33\mu s}{(33\mu s + 0.83\mu s + 0.3\mu s)} \times \frac{1}{8} = \frac{1}{8.27} \qquad (2)$$

Where 33µs is t_{SCAN}, the period of scanning, 0.83µs is t_{NOL1}, 0.3µs is t_{NOL2}, the non-overlap time and CSx delay time.

PWM CONTROL

After setting the I_{OUT} and GCC, the brightness of each LEDs (LED average current (I_{LED})) can be modulated with 256 steps by PWM Register, as described in Formula (1).

$$I_{LED} = \frac{PWM}{256} \times I_{OUT(PEAK)} \times Duty \qquad (1)$$

Where PWM is PWM Registers (PG0, 00h~B3h /PG1, 00h~AAh) data showing in Table 6.

For example, in Figure 1, if R_{ISET}= 10kΩ, PWM= 255, and GCC= 255, SL= 255, then

$$I_{OUT(PEAK)} = \frac{343}{10k\Omega} \times \frac{255}{256} \times \frac{255}{256} = 34mA$$

$$I_{LED} = I_{OUT(PEAK)} \times \frac{1}{8.27} \times \frac{PWM}{256}$$

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

GAMMA CORRECTION

In order to perform a better visual LED breathing effect we recommend using a gamma corrected PWM value to set the LED intensity. This results in a reduced number of steps for the LED intensity setting, but causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Since the IS31FL3745 can modulate the brightness of the LEDs with 256 steps, a gamma correction function can be applied when computing each subsequent LED intensity setting such that the changes in brightness matches the human eye's brightness curve.

Table 15 32 Gamma Steps with 256 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	4	6	10	13	18
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
22	28	33	39	46	53	61	69
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
78	86	96	106	116	126	138	149
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
161	173	186	199	212	226	240	255

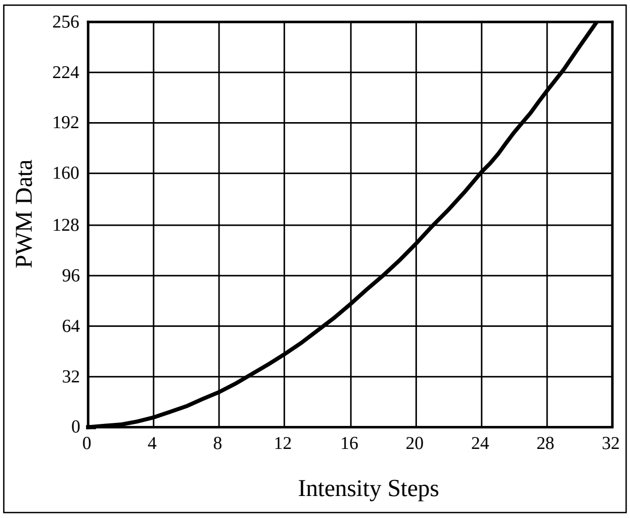


Figure 13 Gamma Correction (32 Steps)

Choosing more gamma steps provides for a more continuous looking breathing effect. This is useful for very long breathing cycles. The recommended configuration is defined by the breath cycle T. When T=1s, choose 32 gamma steps, when T=2s, choose 64 gamma steps. The user must decide the final number of gamma steps not only by the LED itself, but also based on the visual performance of the finished product.

Table 16 64 Gamma Steps with 256 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	3	4	5	6	7
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
8	10	12	14	16	18	20	22
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
24	26	29	32	35	38	41	44
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
47	50	53	57	61	65	69	73
C(32)	C(33)	C(34)	C(35)	C(36)	C(37)	C(38)	C(39)
77	81	85	89	94	99	104	109
C(40)	C(41)	C(42)	C(43)	C(44)	C(45)	C(46)	C(47)
114	119	124	129	134	140	146	152
C(48)	C(49)	C(50)	C(51)	C(52)	C(53)	C(54)	C(55)
158	164	170	176	182	188	195	202
C(56)	C(57)	C(58)	C(59)	C(60)	C(61)	C(62)	C(63)
209	216	223	230	237	244	251	255

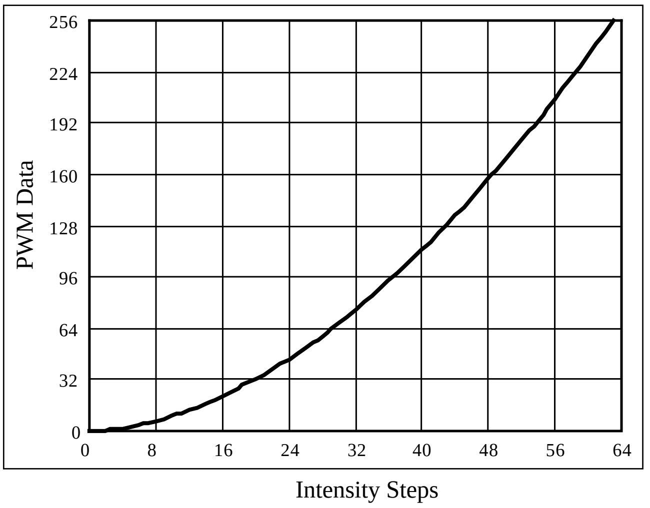


Figure 14 Gamma Correction (64 Steps)

Note: The data of 32 gamma steps is the standard value and the data of 64 gamma steps is the recommended value.

OPERATING MODE

IS31FL3745 can only operate in PWM Mode. The brightness of each LED can be modulated with 256 steps by PWM registers. For example, if the data in PWM Register is “0000 0100”, then the PWM is the fourth step.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

OPEN/SHORT DETECT FUNCTION

IS31FL3745 has open and short detect bit for each LED.

By setting the OSD bits of the Configuration Register (PG2, 00h) from “00” to “01” or “10”, the LED Open/short Register will start to store the open/short information and after at least 2 scanning cycles and the MCU can get the open/short information by reading the 03h~1Ah, for those dots are turned off via LED Scaling Registers (PG1, 00h~90h), the open/short data will not get refreshed when setting the OSD bit of the Configuration Register.

To get the correct open and short information, two configurations need to set before setting the OSD bits:

1 0x0F≤ GCC≤ 0x40
2 02h= 0x00

Where GCC is the Global Current Control Register (PG2, 01h) and 02h is the Pull Down/UP Resistor Selection Register and set to 0x00 is to disable the SWx pull-down and CSy pull-up function.

The detect action is one-off event and each time before reading out the open/short information, the OSD bit of the Configuration Register (PG2, 00h) need to be set from “0” to “1” (clear before set operation).

De-Ghost Function

The “ghost” term is used to describe the behavior of an LED that should be OFF but instead glows dimly when another LED is turned ON. A ghosting effect typically can occur when multiplexing LEDs. In matrix architecture any parasitic capacitance found in the constant-current outputs or the PCB traces to the LEDs may provide sufficient current to dimly light an LED to create a ghosting effect.

To prevent this LED ghost effect, the IS31FL3745 has integrated Pull down resistors for each SWx (x=1~8) and Pull up resistors for each CSy (y=1~18). Select the right SWx Pull down resistor (PG2, 02h) and CSy Pull up resistor (PG2, 02h) which eliminates the ghost LED for a particular matrix layout configuration.

Typically, selecting the 2kΩ will be sufficient to eliminate the LED ghost phenomenon.

The SWx Pull down resistors and CSy Pull up resistors are active only when the CSy/SWx output working the OFF state and therefore no power is lost through these resistors.

When IS31FL3745 works in hardware shutdown mode, the de-ghost function should be disabled, otherwise it will be extra about 1μA shutdown current.

I2C RESET

The I2C will be reset if the SDB pin is pull-high from 0V to logic high, at the operating SDB rising edge, the I2C operation is not allowed.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting SSD bit of the Configuration Register (PG2, 00h) to “0”, the IS31FL3745 will operate in software shutdown mode. When the IS31FL3745 is in software shutdown, all current sources are switched off, so that the matrix is blanked. All registers can be operated. Typical current consume is 1μA.

Hardware Shutdown

The chip enters hardware shutdown when the SDB pin is pulled low. All analog circuits are disabled during hardware shutdown, typical the current consume is 1μA.

The chip releases hardware shutdown when the SDB pin is pulled high. During hardware shutdown state Function Register can be operated.

If V_{CC} has risk drop below 1.75V but above 0.1V during SDB pulled low, please re-initialize all Function Registers before SDB pulled high.

LAYOUT

The IS31FL3745 consumes lots of power so good PCB layout will help improve the reliability of the chip. Please consider below factors when layout the PCB.

Power Supply Lines

When designing the PCB layout pattern, the first step should consider about the supply line and GND connection, especially those traces with high current, also the digital and analog blocks’ supply line and GND should be separated to avoid the noise from digital block affect the analog block.

At least one 0.1μF capacitor, if possible with a 1μF capacitor is recommended to connected to the ground at each power supply pins of the chip, and it needs to close to the chip and the ground net of the capacitor should be well connected to the GND plane.

R_{ISET}

R_{ISET} should be close to the chip and the ground side should well connect to the GND plane.

Thermal Consideration

The over temperature of the chip may result in deterioration of the properties of the chip. IS31FL3745 does not have thermal pad, so for thermal radiation, increase the board size and GND copper area, especially near the GND pins and the opposite layer of the chip.

Current Rating Example

For a R_{ISET}=20kΩ application, the current rating for each net is as follows:

• PVCC and SWx pins = 17.3×18=311.4mA, recommend trace width: 0.2032mm~0.5mm

• CSy pins = 17.3mA, recommend trace width: 0.0762mm~0.254mm

• VCC and all other pins< 3mA, recommend trace width: 0.0762mm~0.254mm

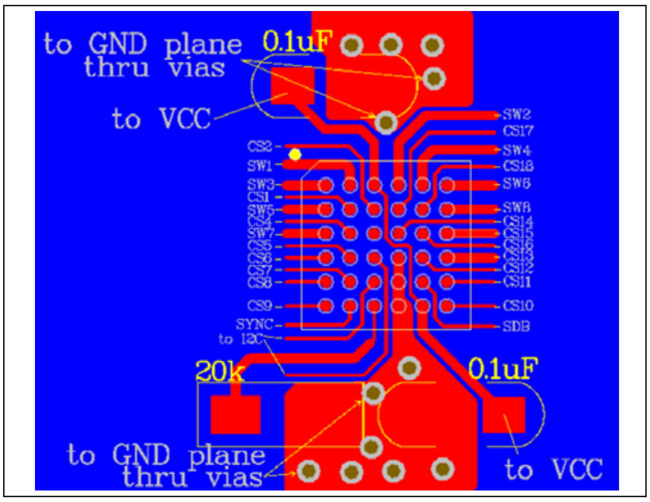


Figure 15 Layout Example

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

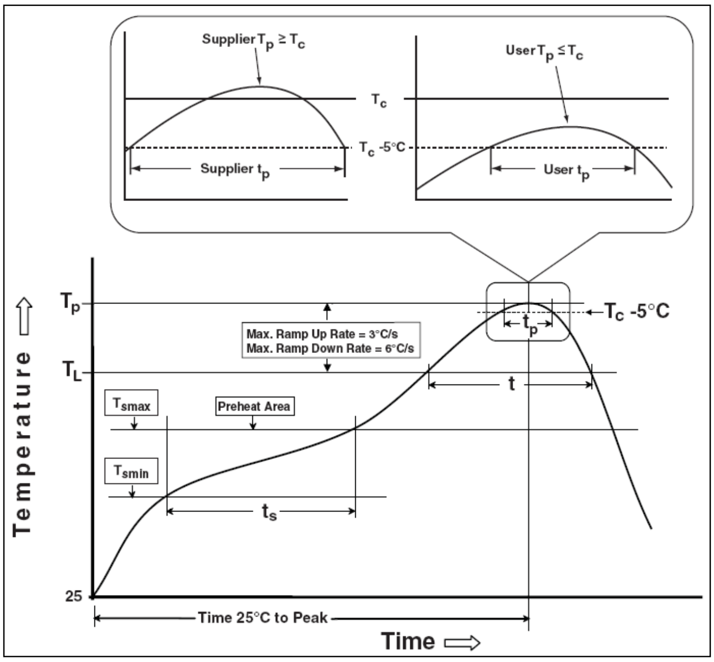
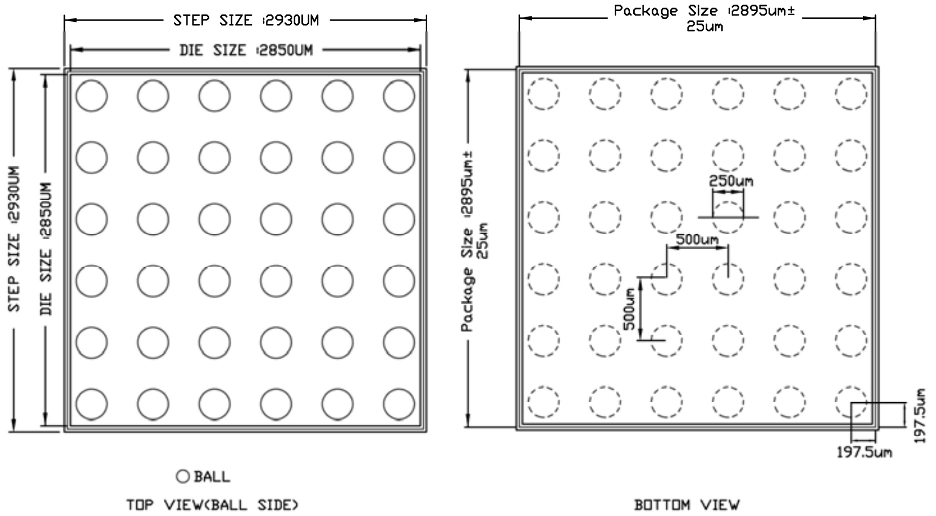


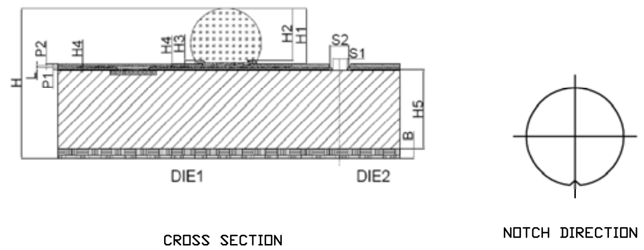
Figure 16 Classification Profile

PACKAGE INFORMATION

WLCSP-36

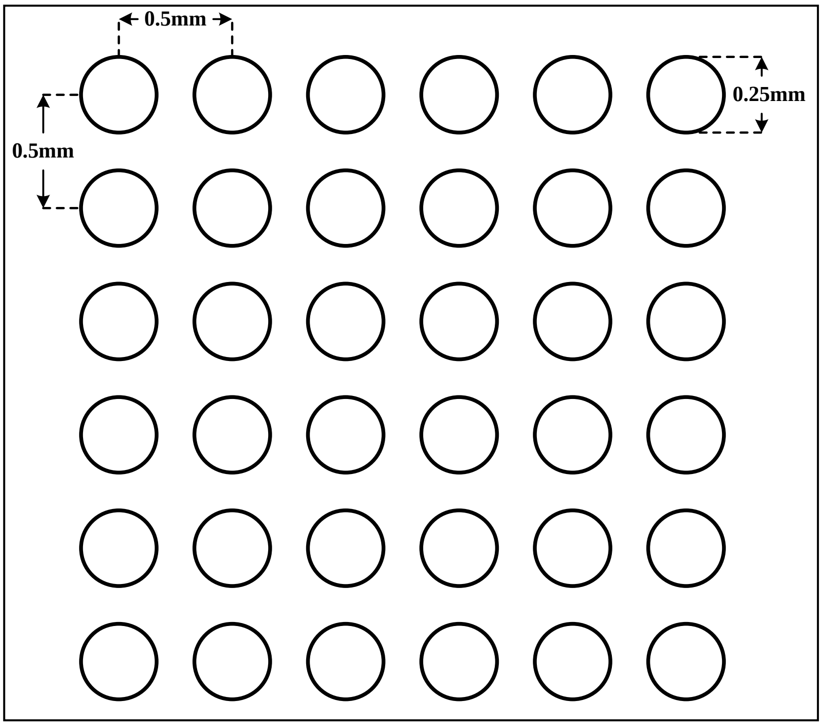


SYMBOL	ITEM	DATA(UM)
H1	BALL HEIGHT	60±9
H2	SNAG HEIGHT	52
H3	CU THICKNESS	8
H4	TI/CU SEED LAYER THICKNESS	1000Å 3000Å
H5	SI THICKNESS	300±10
P1	PI1 THICKNESS	5±1.5
L	RDL THICKNESS	8±2
P2	PI2 THICKNESS	10±2
S1	PI1 OPENING IN SL	70±7
S2	PI2 OPENING IN SL	80±8
B	BACKSIDE COATING THICKNESS	25±10
H	PACKAGE HEIGHT	400±33



RECOMMENDED LAND PATTERN

WLCSP-36



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release	2018.06.04
A	Update EC table and add detail description	2018.10.08