MP6570

3-Phase BLDC Controller with a High-Accuracy Angular Sensor

DESCRIPTION

The MP6570 is a high-performance motor controller that incorporates field-oriented control (FOC) algorithms, SVPWM modulation technology, and an accurate embedded angle sensor. The MP6570 is used for applications with three-phase PMSM and BLDC motors.

The operation of the MP6570 supports three modes, including speed mode, position mode, and torque mode. The reference command comes from either the digital interface or the pulse-width modulation (PWM)/clock input pin. A 10-bit ADC is employed for accurate sampling of each phase current. The three-phase voltage of the motor is modulated through an SVPWM module, which has up to 12-bit resolution at a 20kHz switching frequency.

A high-speed high-accuracy magnetic angular sensor is embedded in the IC for rotor position and speed feedback. The position sensor has a data refresh rate up to 1MHz and up to 14-bit position resolution, ideal for BLDC and PMSM motor controls, especially in applications that require high speed or position accuracy.

Non-volatile memory (NVM) is employed in the MP6570 to store parameters programmed through the selectable I^2C, SPI, or RS485 digital interface.

Application design is aided by the MPS e.Motion Family Virtual Bench online developer tool.

Full protection features include over-current protection (OCP), rotor-lock protection, and input bus over-voltage (OVP) and over-current protection (OCP).

The MP6570 is available in a QFN-32 (4mmx4mm) package.

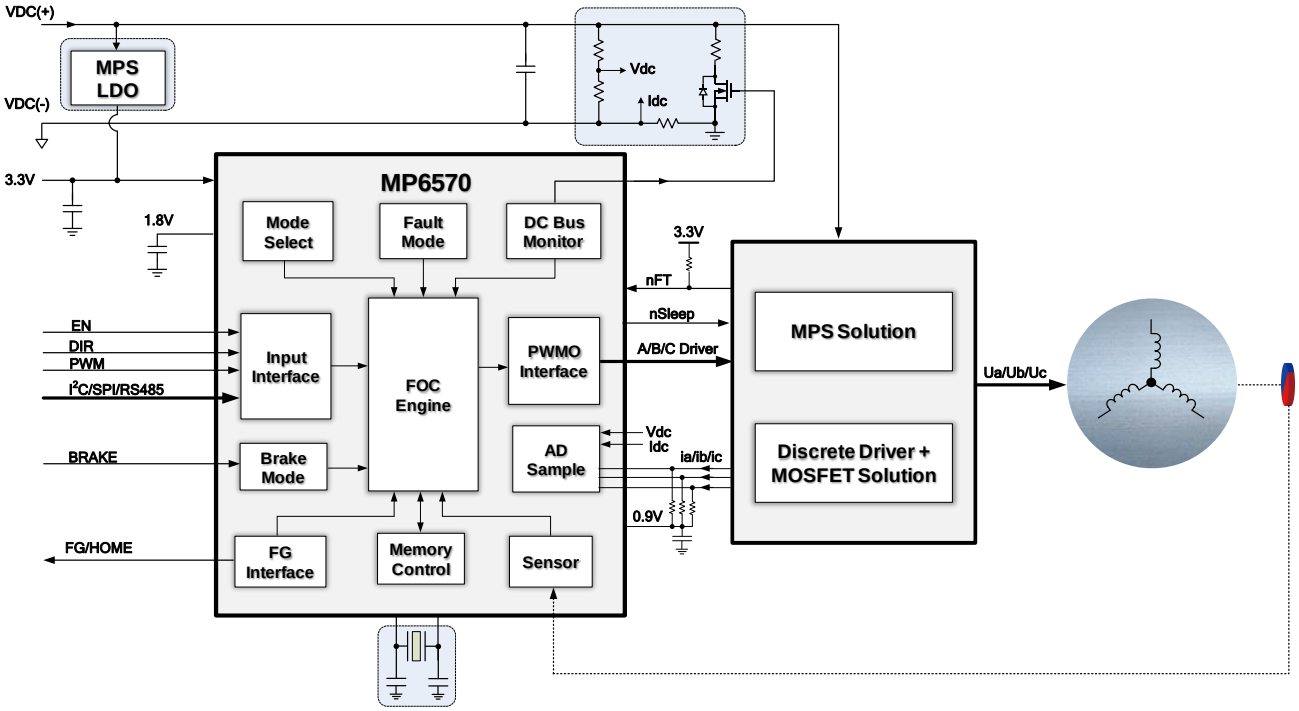
FEATURES

- 3.3V Operating Supply Voltage
- Flexible Parameter Configuration with Non-Volatile Memory and Selectable SPI/I^2C/RS485 Interface
- Embedded Accurate Angular Sensor with Up to 14-Bit Resolution
- Field-Oriented Control (FOC) Method
- Position/Speed/Torque Operation Modes
- PWM/Clock/Digital Interface Reference Input
- Energy Regeneration Braking Mode
- 10-Bit ADC with Programmble Gain
- Up to 80kHz Programmble Switching Frequency
- A/B/Z Output with Internal Sensor Mode
- Up to 32 Progarmmble Slave Addresses
- Selectable Oscillator Source:
  - Internal On-Chip Oscillator
  - External Passive Crystal Input
- Input Bus Over-Current (OCP) and Over-Voltage Protection (OVP)
- Low-Power Standby Mode
- Locked Rotor Detection and Restart
- Programmable Over-Current Limit (OCL) Threshold
- Available in a QFN-32 (4mmx4mm) Package

APPLICATIONS

- PMSM Motor, BLDC Motor

TYPICAL SYSTEM APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP6570GR-xxxx**	QFN-32 (4mmx4mm)	*See Below*

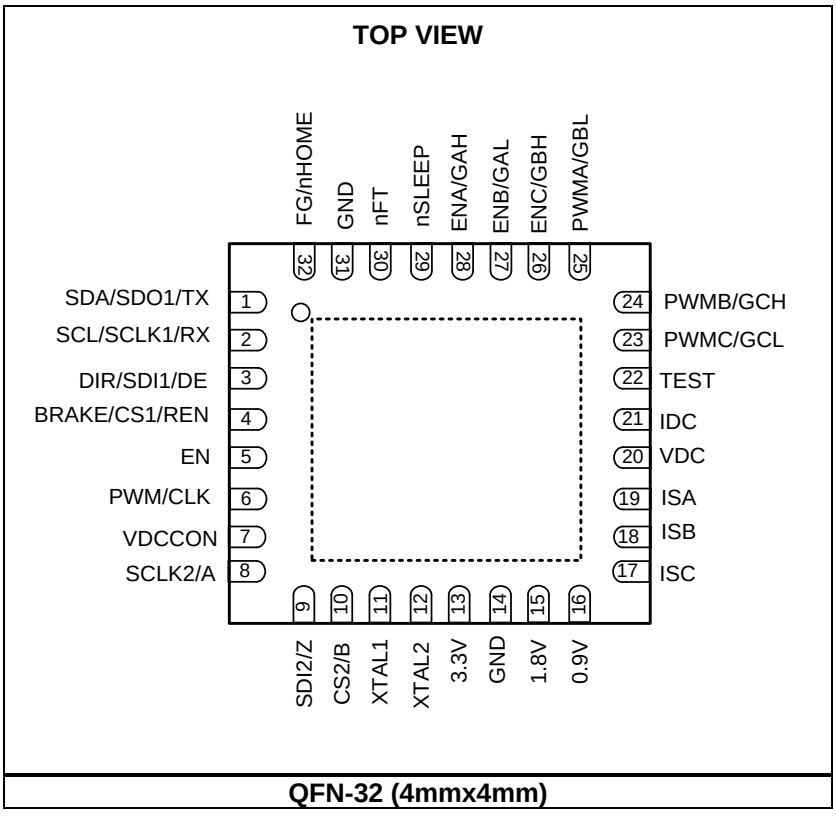
* For Tape & Reel, add suffix –Z (e.g. MP6570GR-0000–Z)
**"xxxx" is the register setting option. The factory default is "0000". For customized options, please contact an MPS FAE to obtain a "xxxx" value.

TOP MARKING

MPSYWW
MP6570
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP6570: Part number
LLLLLL: Lot number

PACKAGE REFERENCE



QFN-32 (4mmx4mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{VCC})..... 5V
All other pins .....-0.3V to +5.5V
Continuous power dissipation (T_A = +25°C) (2)
QFN-32 (4mmx4mm) 3.1W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) 3.3V
Operating junction temp. (T_J)... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-32 (4mmx4mm)	40	8	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operation conditions.
4) Measured on JESD51-7 4-layer board.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.3V, T_A = +25°C, EN = high, nFT = high, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage						
V_{IN} operating range	V_{IN}		3		3.6	V
Turn-on threshold	V_{IN_ON}	V_{IN} rising edge		2.65	2.75	V
Turn-on hysteretic voltage	V_{IN_HY}			0.1		V
IC Supply						
Shutdown current	I_{IN_ST}	EN = low			1	μA
Sleep current	I_{IN_SBY}	EN = high		600		μA
Quiescent current	I_{IN_Q}	External OSC		26		mA
		Internal OSC		23		mA
Logic Input						
Logic high threshold	V_{L_High}				1.8	V
Logic low threshold	V_{L_Low}		0.6			V
Pull-down resistor		PWM/DIR/BRAKE/EN		200		kΩ
Open-Drain Output						
Low logic output voltage	V_{OL}	2mA load		0.1		V
Output leakage current	I_{OH}	3.3V output			0.1	μA
Internal Clock Oscillator						
160MHz	f_{160M}		-1.6%	160	+1.6%	MHz
ADC and Sample Hold						
Resolution (5)					10	bit
1.6V supply voltage	V_{1V6}		-1%	1.6	+1%	V
0.9V supply voltage	V_{BIAS}			900		mV
Angular Sensor						
Resolution				14		bit
Refresh rate (6)	f_{RATE}	Internal sensor		1000		kHz
		External sensor		500		
Intrinsic non-linearity (INL)		End-shaft mounting		±0.6		deg
PWM Output						
Dead time	T_{DB}	DTPWM = 101000		1		μs

NOTE:

5) Guaranteed by character data.

6) Guaranteed by design.

PIN FUNCTIONS

Pin #	Name	Description
1	SDA/SDO1/TX	Selectable for: • I^2C data signal • SPI port 1 data output signal • RS485 TX output signal
2	SCL/SCKL1/RX	Selectable for: • I^2C clock signal • SPI port 1 clock signal • RS485 RX input signal
3	DIR/SDI1/DE	Selectable for: • Direction input • SPI port 1 data input signal • RS485 write enable (DE) signal
4	BRAKE/CS1/REN	Selectable for: • Brake input • SPI port 1 CS signal, low level activates the interface • RS485 read enable (REN) signal
5	EN	**IC enable.**
6	PWM/CLK	Selectable for: • PWM input for speed control • PWM input for torque control • Clock input for speed/position control
7	VDCCON	**Input bus protection control output.**
8	SCLK2/A	Selectable for: • SPI port 2 clock signal for external angular sensor data input • Internal sensor A signal output
9	SDI2/Z	Selectable for: • SPI port 2 data signal for external angular sensor data input • Internal sensor Z signal output
10	CS2/B	Selectable for: • SPI port 2 chip select signal for external angular sensor data input • Internal sensor B signal output
11	XTAL1	**External crystal oscillator signal input.**
12	XTAL2	**External crystal oscillator signal output.** Float XTAL2 if it is not being used.
13	3.3V	**IC power supply input.**
14, 31	GND	**Ground.**
15	1.8V	**1.8V reference output.**
16	0.9V	**0.9V reference output for ADC bias.**
17	ISC	**Phase C current detection input of motor winding.**
18	ISB	**Phase B current detection input of motor winding.**
19	ISA	**Phase A current detection input of motor winding.**
20	VDC	**Input power bus voltage detection input.**
21	IDC	**Input power bus current detection input.**
22	TEST	**IC test pin.** Leave TEST floating in normal applications.

PIN FUNCTIONS *(continued)*

Pin #	Name	Description
23	PWMC/GCL	Selectable for: • Phase C PWM output, which is compatible with the MP653x/4x power stage • Low-side gate drive output of phase C
24	PWMB/GCH	Selectable for: • Phase B PWM output, which is compatible with the MP653x/4x power stage • High-side gate drive output of phase C
25	PWMA/GBL	Selectable for: • Phase A PWM output, which is compatible with the MP653x/4x power stage • Low-side gate drive output of phase B
26	ENC/GBH	Selectable for: • Phase C enable output, which is compatible with the MP653x/4x power stage • High-side gate drive output of phase B
27	ENB/GAL	Selectable for: • Phase B enable output, which is compatible with the MP653x/4x power stage • Low-side gate drive output of phase A
28	ENA/GAH	Selectable for: • Phase A enable output, which is compatible with the MP653x/4x power stage • High-side gate drive output of phase A
29	nSLEEP	**Sleep mode enable output for power stage.**
30	nFT	**Fault indication input from power stage and internal fault output.**
32	FG/HOME	Selectable for: • Speed indication signal (FG) • Rotor position HOME output signal

BLOCK DIAGRAM

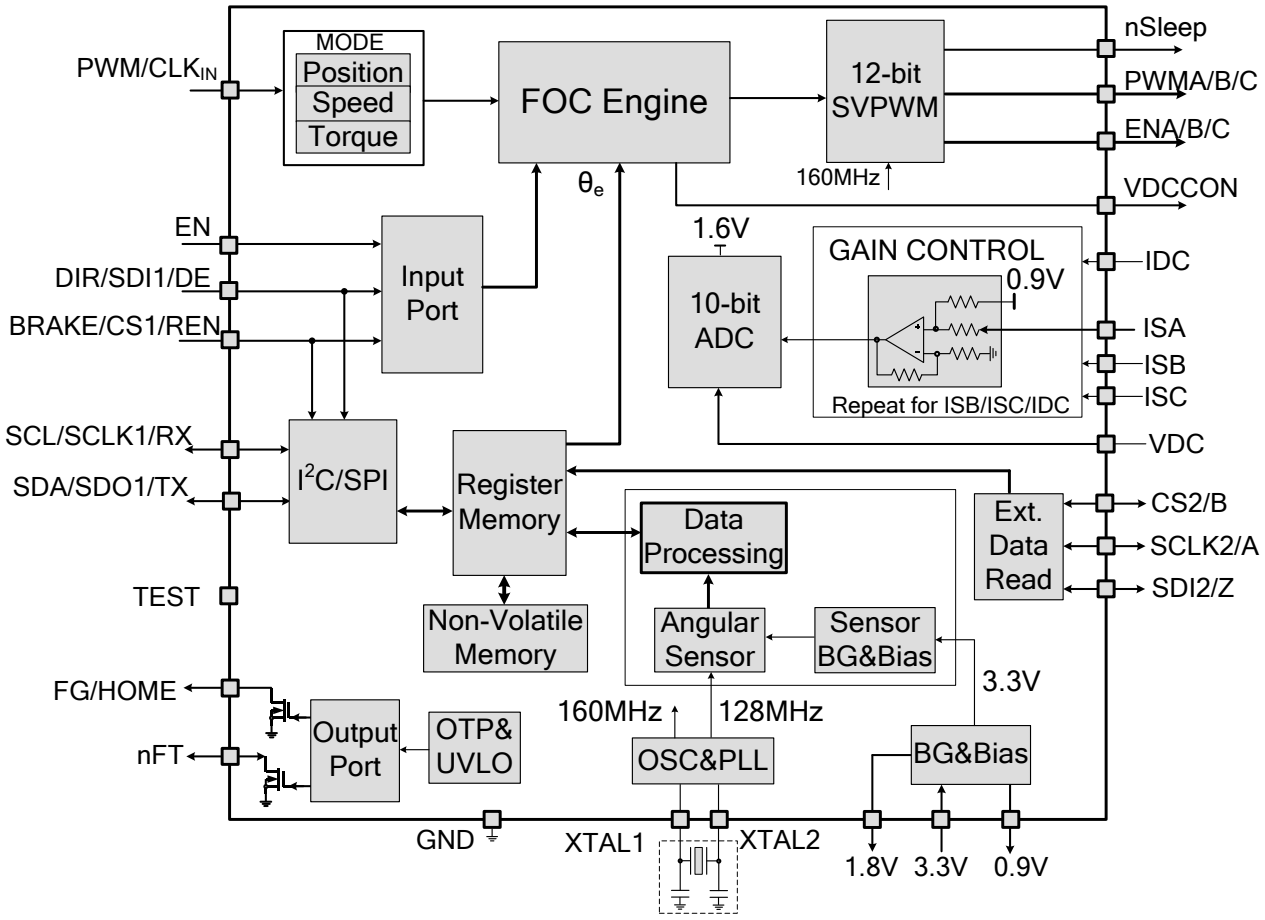


Figure 1: Functional Block Diagram

OPERATION

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Application design is aided by the MPS e.Motion Family Virtual Bench online developer tool.

Angular Sensor

End-Shaft Mounting

The embedded angular sensor is a magnetic sensor designed to measure the rotor position with high accuracy and resolution by detecting the absolute angular position of a two-pole diametrically magnetized cylinder attached to the rotor end of a shaft. The internal angular sensor has a 1MHz data refresh rate, which allows for accurate angle measurement over a wide speed range. The resolution of the angular sensor is up to 14-bit and intrinsic non linearity (INL) down to ±0.1° can be achieved via MPS's internal proprietary AccuFilter™ filter when using end-of-shaft magnet mounting.

The sensor detects the angle of the magnet field projected in a plane parallel to the upper surface of the package. This means that only the magnet field of the in-plane components (X and Y components) at the package center point is measured. A field amplitude between 30mT and 150mT is recommended for the best performance. Note that the sensor can work with fields smaller than 30mT, but the linearity and resolution performance may deviate from the specifications.

The typical solution is to place the IC on the radial axis of a diametrically magnetized permanent cylinder magnet (see Figure 2).

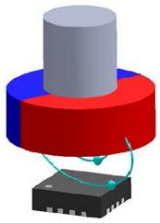


Figure 2: End of Shaft Mounting

Side-Shaft Mounting

When end-of-shaft mounting is unavailable, the sensor can be positioned away the ration axis of the cylinder or ring magnet (see the ring magnet example in Figure 3). In this case, the mechanical angle is no longer directly proportional to the magnet field angle. The sensor can be adjusted to compensate for this effect. With multiple pole pairs, the sensor can detect multiple rotations for each mechanical turn.

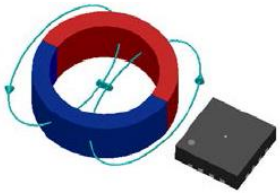


Figure 3: Side-Shaft Mounting

Sensor Angle Direction

By default, the angle increases when the magnetic field rotates clockwise (CW) looking from the top of the package (see Figure 4).

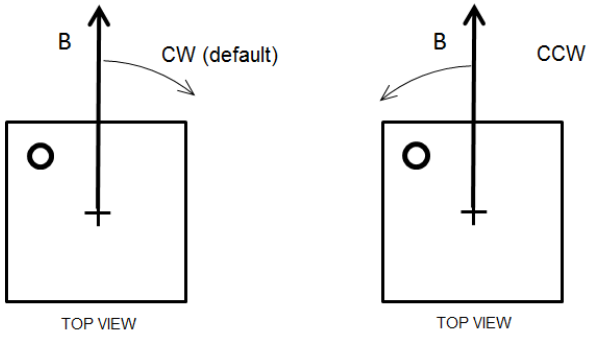


Figure 4: Sensor Angle Direction

Data from the angular sensor used for system control can be configured in two modes: original mode or complementary mode. This is controlled by register bit THETA_DIR.

Bias Current Trimming (BCT)

When the MP6570 is mounted in a side-shaft configuration, the relation between the field angle and the mechanical angle is no longer directly linear. This effect is related to the fact that the tangential magnetic field is usually smaller than the radial field. Define the field ratio (*k*) with Equation (1):

$$k = B_{rad} / B_{tan} \quad (1)$$

Where B_{rad} is the maximum radial magnetic field, and B_{tan} is the maximum tangential magnetic field (see Figure 5).

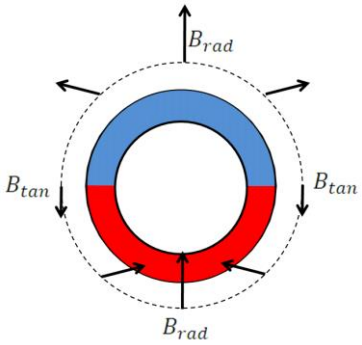


Figure 5: Side-Shaft Field

The ratio *k* depends on the magnet geometry and the distance to the sensor.

Having a *k* ratio different than 1 results in an error of the sensor output. Note that the error curve has the shape of a double sine-wave.

The X-axis or the Y-axis bias current can be reduced by programming to recover an equal Hall signal for all angles and therefore suppress the error. The parameters ETX and ETY control the direction in which sensitivity is reduced. Current reduction is set by the parameter bias current trimming BCT(7:0), which is an integer from 0 to 255.

In side-shaft configuration (i.e.: the sensor center is located beyond the magnet outer diameter), *k* is greater than 1. For optimum compensation, the sensitivity of the radial axis should be reduced by setting the BCT parameter as shown in Equation (2):

$$BCT(7,0) = 258\left(1 - \frac{1}{k}\right) \quad (2)$$

Equation (2) is plotted in Figure 6.

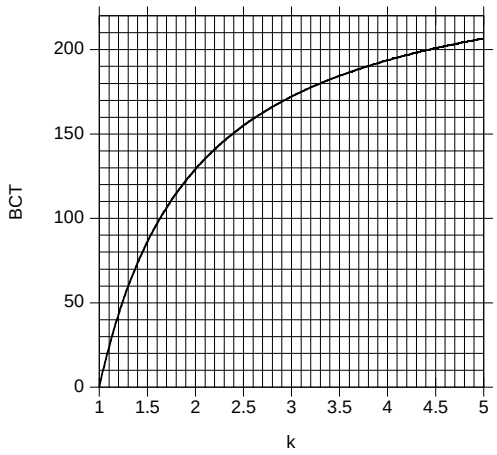


Figure 6: Relation between the *k* Ratio and the Optimum BCT to Recover Linearity

What if k is Unknown?

It is possible to deduce the *k* ratio from the error curve obtained with the default BCT setting (BCT = 0). For this purpose, rotate the magnet over one revolution, record the MP6570 angle sensor output, plot the error curve (i.e.: the sensor output minus the real mechanical position vs. the real mechanical position), and extract two parameters: the maximum error (E) and the position of this maximum with respect to a zero crossing a_m (see Figure 7).

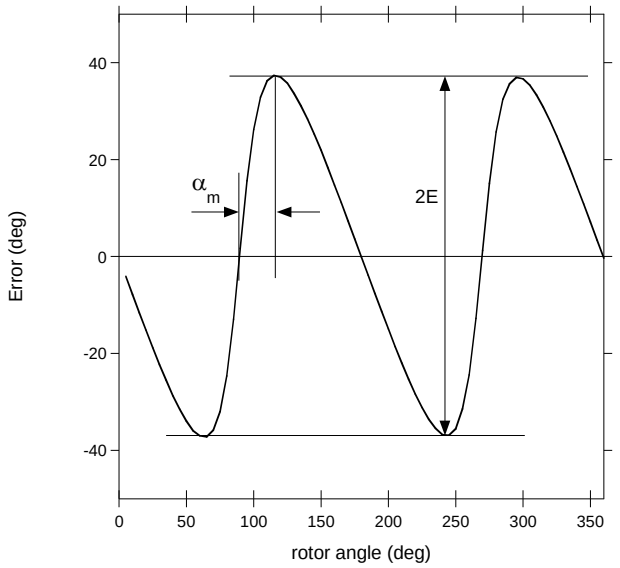


Figure 7: Error Curve in Side-Shaft Configuration with BCT = 0

The *k* parameter can then be obtained from the graph in Figure 8 and Table 1.

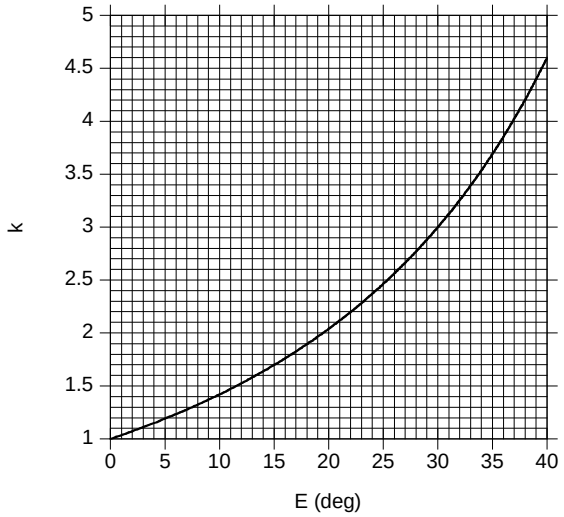


Figure 8: Relation between the Error Measured with BCT = 0 and the Magnet Ratio *k*

This relation between INL and the *k* ratio is expressed in Equation (3):

$$k = \frac{\tan(E + \alpha_m)}{\tan(\alpha_m)} \quad (3)$$

Table 1: Example of BCT Setting

E (deg)	Magnet Ratio *k*	BCT(7:0)
0	1.0	0
11.5	1.5	86
19.5	2.0	129
25.4	2.5	155
30.0	3.0	172
33.7	3.5	184
36.9	4.0	194
39.5	4.5	201
41.8	5.0	207

Sensor X/Y Orientation

From the dot marked on the package, it is possible to know whether the radial field is aligned with the sensor coordinate X or Y (see Figure 9).

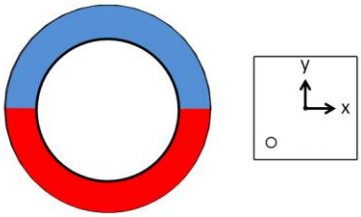


Figure 9: Package Top View with X- and Y-Axes

Determine which axis needs to be reduced. For instance, with the arrangement depicted in Figure 9, the field along the sensor Y direction is tangential and therefore weaker. This means that the X-axis should be reduced: ETX = 1 and ETY = 0. Note that if both ETX and ETY are set to 1, the current bias is reduced in both directions the same way (i.e.: without side-shaft correction).

Zero Offset for ABZ

If the internal sensor is selected, the sensor data supports an A, B, Z format output to show the rotor position. With this function, the zero offset can be added to trim the zero (Z) position of the rotor. The zero offset function is enabled through setting bit ZERO_OFFSET. The data offset is set through bits ZERO[9:0] (10MSB of 16-bit data).

Sensor Data Source

The MP6570 also supports an external angle data input mode for its internal position feedback. The mode is selected by the register EXANG bit. By setting the EXANG bit to 0, the MP6570 uses its internal on-chip angular sensor. By setting the EXANG bit to 1, external position feedback is selected. In external sensor mode, the MP6570 reads back the angular position data from an external MPS angular sensor IC in the MA3xx/7xx family through the SPI port 2 interface.

SPI Port 2 Interface

During data communication, one data stream consists of 16 bits of data with the MSB of the angle first. The data bit read-back is on the SCLK rising edge when CS is pulled low. Figure 10 shows the interface between the MP6570 and an MPS angle sensor IC. For detailed communication information, refer to the MP30x/70x datasheets.

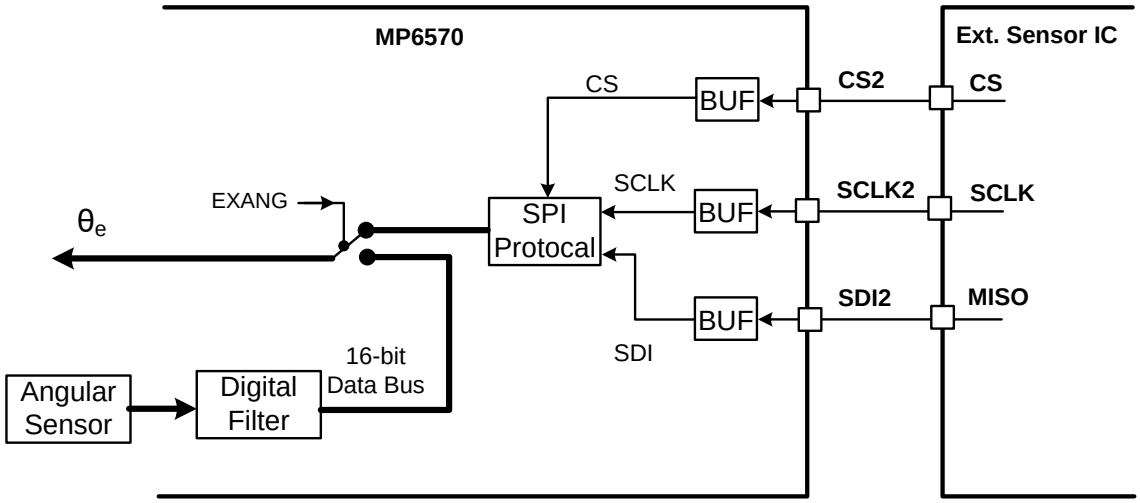


Figure 10: MP6570 with Angle Sensor IC

Address: 05h			
Bit[15:0]	**Name**	**Default**	**Description**
[15]	THETA_DIR	0	0: IC uses the original data value from the angular sensor 1: IC uses the complementary data value from the angular sensor

Address: 33h			
Bit[15:0]	**Name**	**Default**	**Description**
[4]	EXANG	1	0: use internal angular sensor as rotor position feedback. 1: use external angular sensor as rotor position feedback. The data is read back through SPI port 2.

Address: 35h			
Bit[15:0]	**Name**	**Default**	**Description**
[9]	ETX	0	When enabled, the X-axis bias current is trimmed by the quantity BCT.
[8]	ETY	0	When enabled, the Y-axis bias current is trimmed by the quantity BCT.
[7:0]	BCT	00H	For side-shaft configuration: reduce the Hall device bias current of X- and/or Y-axis.

Address: 36h			
Bit[15:0]	**Name**	**Default**	**Description**
[10]	ZERO_OFFSET	0	Zero offset enable of the A/B/Z output.
[9:0]	ZERO	000H	Sets the zero point of sensor the A/B/Z output.

AccuFilter and Calibration

To improve the intrinsic non-linearity (INL) of the sensor data, the MP6570 embeds an AccuFilter function with 32 data points (DATA0 to DATA31) stored in the NVM for calibration. The calibration sequence is described below.

1. Run the motor at a steady speed and sample the real sensor data and reference encoder data in one mechanical round. The perfect reference is from the high-accuracy encoder output. If an encoder is not available, a high-accuracy timing signal can be taken as a reference assuming that the motor speed is constant. To provide a stable speed, it is better to run the motor with a high speed and a large inertial load.
2. Save the error data reference minus the sensor data to the 32 data bytes from DATA0 to DATA31. The error data for calibration can be calculated with Equation (3) if ($\theta_{ref} \geq \theta_{sensor}$) or Equation (4) if ($\theta_{ref} < \theta_{sensor}$):

$$DATA_X[7:0] = (\theta_{ref} - \theta_{sensor}) \times \frac{2^{13}}{360} \quad (3)$$

$$DATA_X[7:0] = 256 - (\theta_{sensor} - \theta_{ref}) \times \frac{2^{13}}{360} \quad (4)$$

The MSB of DATA0-31 is a sign bit, and the maximum calibration range is ±360°/2^6.

This data is shown graphically in Figure 11.

The sensor position for the system control is the sum of the sensor raw data and the calibration data. When INTERPOLATION is set to 1, the MP6570 performs linear interpolation between two adjacent calibration data points.

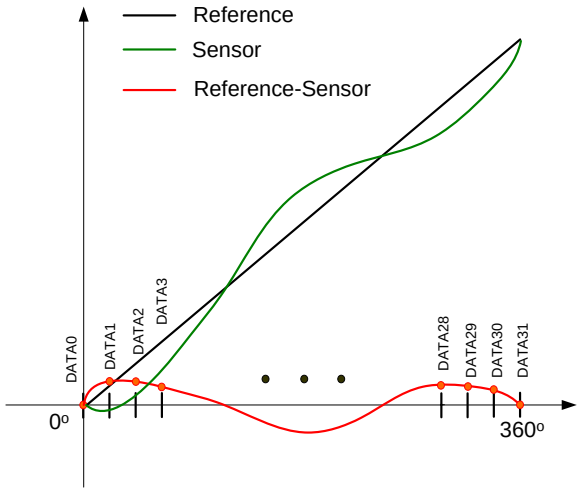


Figure 11: Sensor Error Calibration

Address: 35h			
Bit[15:0]	**Name**	**Default**	**Description**
[13]	INTERPOLATION	0	1: use linear interpolation for calibration 0: disable linear interpolation function

Address: 40h			
Bit[15:0]	**Name**	**Default**	**Description**
[15:8]	DATA1	00H	Calibration data 1.
[7:0]	DATA0	00H	Calibration data 0.

Address: 41h			
Bit[15:0]	**Name**	**Default**	**Description**
[15:8]	DATA3	00H	Calibration data 3.
[7:0]	DATA2	00H	Calibration data 2.

Address: 42h			
Bit[15:0]	**Name**	**Default**	**Description**
[15:8]	DATA5	00H	Calibration data 5.
[7:0]	DATA4	00H	Calibration data 4.

Address: 43h			
Bit[15:0]	**Name**	**Default**	**Description**
[15:8]	DATA7	00H	Calibration data 7.
[7:0]	DATA6	00H	Calibration data 6.

Address: 44h			
Bit[15:0]	**Name**	**Default**	**Description**
[15:8]	DATA9	00H	Calibration data 9.
[7:0]	DATA8	00H	Calibration data 8.

Address: 45h			
Bit[15:0]	**Name**	**Default**	**Description**
[15:8]	DATA11	00H	Calibration data 11.
[7:0]	DATA10	00H	Calibration data 10.

Address: 46h			
Bit[15:0]	**Name**	**Default**	**Description**
[15:8]	DATA13	00H	Calibration data 13.
[7:0]	DATA12	00H	Calibration data 12.

Address: 47h			
Bit[15:0]	**Name**	**Default**	**Description**
[15:8]	DATA15	00H	Calibration data 15.
[7:0]	DATA14	00H	Calibration data 14.

Address: 48h			
Bit[15:0]	**Name**	**Default**	**Description**
[15:8]	DATA17	00H	Calibration data 17.
[7:0]	DATA16	00H	Calibration data 16.

Address: 49h			
Bit[15:0]	**Name**	**Default**	**Description**
[15:8]	DATA19	00H	Calibration data 19.
[7:0]	DATA18	00H	Calibration data 18.

Address: 4Ah			
Bit[15:0]	**Name**	**Default**	**Description**
[15:8]	DATA21	00H	Calibration data 21.
[7:0]	DATA20	00H	Calibration data 20.

Address: 4Bh			
Bit[15:0]	**Name**	**Default**	**Description**
[15:8]	DATA23	00H	Calibration data 23.
[7:0]	DATA22	00H	Calibration data 22.

Address: 4Ch			
Bit[15:0]	**Name**	**Default**	**Description**
[15:8]	DATA25	00H	Calibration data 25.
[7:0]	DATA24	00H	Calibration data 24.

Address: 4Dh			
Bit[15:0]	**Name**	**Default**	**Description**
[15:8]	DATA27	00H	Calibration data 27.
[7:0]	DATA26	00H	Calibration data 26.

Address: 4Eh			
Bit[15:0]	**Name**	**Default**	**Description**
[15:8]	DATA29	00H	Calibration data 29.
[7:0]	DATA28	00H	Calibration data 28.

Address: 4Fh			
Bit[15:0]	**Name**	**Default**	**Description**
[15:8]	DATA31	00H	Calibration data 31.
[7:0]	DATA30	00H	Calibration data 30.

Control and Reference Input Mode

The MP6570 supports three operational modes: position, speed, and torque mode. The mode can be selected by setting the MODE register bits. In each mode, the reference input mode is selected by setting the CMD_MOD register bits. When the reference input mode is set as the digital register input mode, the reference for the torque and speed supports the sync-up command. The sync-up function is enabled through CMD_SYNC_EN. When the sync-up function is enabled, the reference is not active until a reference sync-up command is sent. In position mode with a digital reference input, the sync-up function is enabled automatically regardless of the state of CMD_SYNC_EN.

Reference Sync-Up Command

Writing 0000H to register 67H triggers the reference command update (see Figure 12).

Torque Control Mode

The control block diagram is shown in Figure 13.

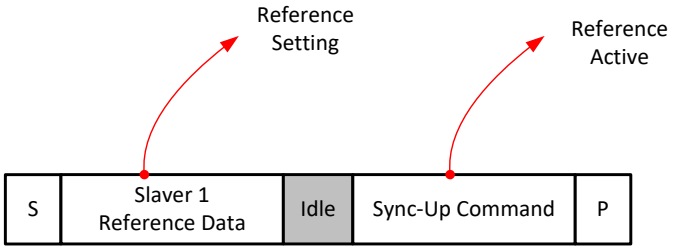


Figure 12: Reference Command in Sync-Up Mode

Address: 33h			
Bit[15:0]	**Name**	**Default**	**Description**
[13:12]	MODE	00	Defines the motor control mode. 00: speed control mode 01: position control mode 10: torque control mode
[11:10]	CMD_MOD	00	Defines the reference signal source. 00: reference is from register setting value 01: reference is from external PWM signal input 10: reference is from external clock signal input

Address: 3Bh			
Bit[15:0]	**Name**	**Default**	**Description**
[12]	CMD_SYNC_EN	00	0: disables digital reference sync-up function. 1: enables digital reference sync-up function

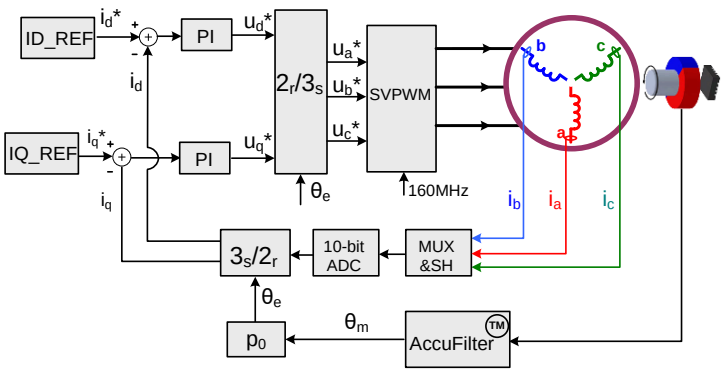


Figure 13: Torque Control Mode

PWM Input Mode

In this mode (set CMD_MOD to 01), a 100Hz - 100kHz input pulse-width modulation (PWM) frequency is recommended. The duty cycle of the input PWM signal sampled with a maximum 40MHz internal clock is calculated and digitized to provide the torque reference. The 100% duty cycle torque reference corresponds to the torque current set by the register IQ_LMT bits.

Digital Interface Input Mode

In this mode (set CMD_MOD to 00), the ID and IQ current reference are set through the ID_REF and IQ_REF bits.

Address: 06h			
Bit[15:0]	**Name**	**Default**	**Description**
[10:0]	IQ_LMT	352H	In torque control mode, it defines the maximum iq current reference corresponding to 100% PWM input duty cycle. IQ_LMT[10:0] is set according to: Iq_limit* sqrt(3/2)*gain_ad*1023/1.6 Where gain_ad is Rsense*Kad when ADMOD is set to 0, and gain_ad is Rpull/Kcs when ADMOD is set to 1. Kad: refer to the AD gain description section. Kcs: current sense ratio. Refer to the MPS MP654x datasheet.

Address: 10h			
Bit[15:0]	**Name**	**Default**	**Description**
[10:0]	ID_REF	000H	Defines the d axis current reference. MSB is a sign bit. When id is positive: ID_REF[11:0] = id* sqrt(3/2)*gain_ad*1023/1.6 When ID is negative: ID_REF[11:0] = 4096 - abs(id)* sqrt(3/2) * gain_ad * 1023/1.6 Where gain_ad is Rsense*Kad when ADMOD is set to 0, and gain_ad is Rpull/Kcs when ADMOD is set to 1. Kad: refer to the AD gain description section. Kcs: current sense ratio. Refer to the MPS MP654x datasheet.

Address: 11h			
Bit[15:0]	**Name**	**Default**	**Description**
[10:0]	IQ_REF	0AAH	Defines the q axis current reference. MSB is a sign bit. When iq is positive, IQ_REF[11:0] = iq* sqrt(3/2)*gain_ad*1023/1.6 When IQ is negative, IQ_REF[11:0] = 4096 - abs(iq)* sqrt(3/2) * gain_ad * 1023/1.6 Where gain_ad is Rsense*Kad when ADMOD is set to 0, and gain_ad is Rpull/Kcs when ADMOD is set to 1. Kad: refer to the AD gain description section. Kcs: current sense ratio. Refer to the MPS MP654x datasheet.

Loop Compensation

The current loop PI filter is set through register CURRENT_KI and CURRENT_KP.

It is recommended to use the MPS e.Motion Family Virtual Bench online developer tool for design.

Calculate CURRENT_KI and CURRENT_KP with Equation (5) and Equation (6):

$$CURRENT\_KP = \frac{51.2}{\sqrt{3}\cdot Vin}\cdot\frac{Lq(\mu H)}{gain\_ad} \quad (5)$$

$$CURRENT\_KI = \frac{819.2}{\sqrt{3}\cdot Vin}\cdot\frac{Rs(\Omega)\cdot Ts(\mu s)}{gain\_ad} \quad (6)$$

Where gain_ad is the current sample gain coefficient. See the ADC Sample and Hold section on page 29 for more detail.

When AD_MOD = 0, calculate gain_ad with Equation (7):

$$gain\_ad = Rs\cdot Kad \quad (7)$$

When AD_MOD = 1, calculate gain_ad with Equation (8):

$$gain\_ad = \frac{R_{pull}(\Omega)}{K_{cs}} \quad (8)$$

Where Kcs is the current sense ratio. Refer to the MPS MP654x datasheet for more detail.

Address: 12h			
Bit[15:0]	**Name**	**Default**	**Description**
[15:0]	CURRENT_KI	03E8H	Defines the integrator gain of current loop.

Address: 13h			
Bit[15:0]	**Name**	**Default**	**Description**
[15:0]	CURRENT_KP	07D0H	Defines the proportion gain of current loop.

Speed Control Mode

Clock Input Mode

In clock input mode (set CMD_MOD to 10 for the clock signal input), the IC controls the rotor speed reference by detecting the input signal rising edge (see Figure 14). The position reference moves forward one step, programmable with register bits NSTEP, with one input clock pulse. Therefore, with a fixed clock input frequency, the rotor rotation speed is controlled exactly. The speed accuracy is directly dependent on the input clock frequency accuracy.

The relationship between the speed (r/min) and input clock frequency is shown in Equation (9):

$$Speed(r/min.) = \frac{60\cdot NSTEP\cdot f_{clk}}{2^{14}} \quad (9)$$

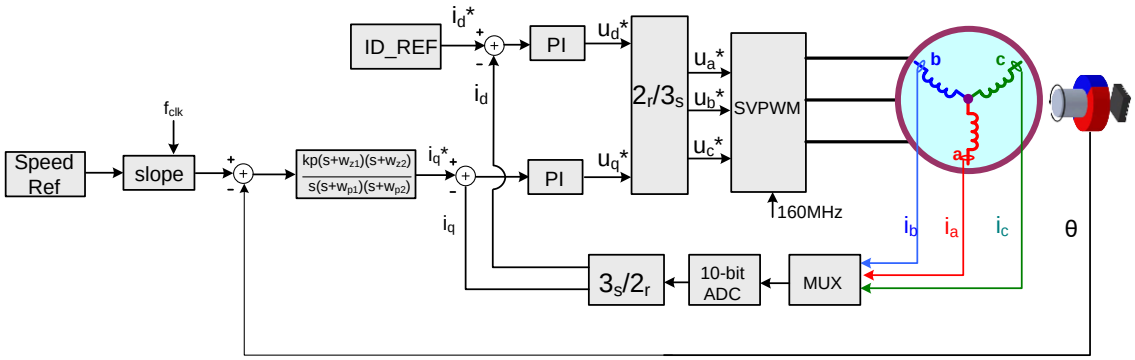


Figure 14: Speed Control Block Diagram

PWM Input Mode

In PWM input mode (set CMD_MOD to 01 for the PWM signal input), the IC controls the rotor speed reference by detecting the input signal duty cycle. The 100% duty cycle speed corresponds to the speed set by register bits SPEED_CMD. The minimum speed is set by the register bits SPD_MIN. To avoid speed reference changes caused by the PWM input jitter, the speed hysteresis is set by SPD_CMD_HYS. The speed gain is set by setting register bits SPD_RANGE.

The real speed output is set with the below equations, where $gain_{spd}$ is set through SPD_RANGE.

When NSTEP[0] = 0, calculate the speed with Equation (10):

$$speed(r/min) = SPEED\_CMD \times duty_{PWM} \times gain_{spd} \quad (10)$$

When NSTEP[0] = 1, calculate the speed with Equation (11):

$$speed(r/min) = SPEED\_CMD \times duty_{PWM} \times gain_{spd} \times 8 \quad (11)$$

Digital Interface Input Mode

In digital interface input mode (set CMD_MOD to 00), the speed reference is directly set by the internal register bits SPEED_CMD. The minimum speed is set by the register bits SPD_MIN. The speed accuracy is dependent on the accuracy of the f_{40M} clock frequency. To achieve a high accuracy of the rotor speed, a crystal oscillator is recommended in the digital input reference mode. The real speed output is set with the below equations.

When NSTEP[0] = 0, calculate the speed with Equation (12):

$$speed(r/min) = SPEED\_CMD \times gain_{spd} \quad (12)$$

With NSTEP[0] = 1, calculate the speed with Equation (13):

$$speed(r/min) = SPEED\_CMD \times gain_{spd} \times 8 \quad (13)$$

Where $gain_{spd}$ is set through SPD_RANGE.

Address: 05h			
Bit[15:0]	**Name**	**Default**	**Description**
[8:0]	NSTEP	10H	Defines the reference step value LSBs with each clock input. With clock input mode, the reference moves forward 4*NSTEP LSBs with each clock input. Therefore, the steps number per round is 65536/(4*NSTEP). With the digital and PWM input in speed mode, the gain coefficient is 1 when setting NSTEP[0] with 0. The gain coefficient is 8 when setting NSETEP[0] with 1.

Address: 20h			
Bit[15:0]	**Name**	**Default**	**Description**
[15:0]	SPEED_CMD	0064H	Defines the digital speed reference (r/min) together with the gain coefficient set by SPD_RANGE.

Address: 21h			
Bit[15:0]	**Name**	**Default**	**Description**
[15:7]	SPD_CMD_HYS	01H	Speed command hysteresis at PWM input signal input mode.
[6:4]	SPD_MON_GAIN	011	Set to 000 if $gain_{spd}$ is 1/8 Set to 001 if $gain_{spd}$ is 1/4 Set to 010 if $gain_{spd}$ is 1/2 Set to 011 if $gain_{spd}$ is 1 Set to 100 if $gain_{spd}$ is 2 Set to 101 if $gain_{spd}$ is 4 Set to 110 if $gain_{spd}$ is 8
[3:0]	SPD_RANGE	0000	Defines the speed reference, together with SPEED_CMD, in speed control mode. 4'b1100: $gain_{spd}$ is 1/8 4'b1010: $gain_{spd}$ is 1/4 4'b1001: $gain_{spd}$ is 1/2 4'b0100: $gain_{spd}$ is 8 4'b0010: $gain_{spd}$ is 4 4'b0001: $gain_{spd}$ is 2 4'bx000: $gain_{spd}$ is 1
[15:0]	SPD_MIN	0014H	Defines the min. speed reference in speed control mode.

Speed Reference Slope Control

When the speed reference changes with the digital and PWM input modes, the real speed reference is controlled smoothly to avoid overshoot and inrush current (see Figure 15).

The speed reference slope is set by spd_step/time_step.

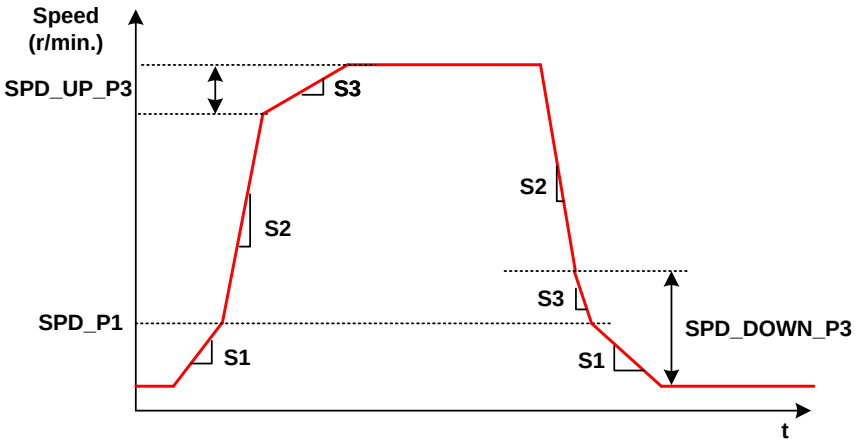


Figure 15: Speed Reference Slope Control

The following sequence occurs when the speed is increasing:

- During S1: spd_step is set by SPD_UP _STEP1, and time_step is set by SPD_STEP_TL.
- During S2: spd_step is set by SPD_UP _STEP2, and time_step is set by SPD_STEP_TH.
- During S3: spd_step is set by SPD_UP _STEP3, and time_step is set by SPD_STEP_TL.

The following sequence occurs when the speed is decreasing:

- During S1: spd_step is set by SPD_ DOWN _STEP1, and time_step is set by SPD_STEP_TL.
- During S2: spd_step is set by SPD_ DOWN _STEP2, and time_step is set by SPD_STEP_TH.
- During S3: spd_step is set by SPD_ DOWN _STEP3, and time_step is set by SPD_STEP_TL.

Address: 1Ch			
Bit[15:0]	**Name**	**Default**	**Description**
[9:0]	SPD_STEP_TH	064H	Defines the reference duration time for each step in the fast slope reference stage. The value is set by SPD_STEP_TH*10μs.

Address: 1Dh			
Bit[15:0]	**Name**	**Default**	**Description**
[9:0]	SPD_STEP_TH	064H	Defines the reference duration time for each step in the fast slope reference stage. The value is set by SPD_STEP_TL*10μs.

Address: 1Eh			
Bit[15:0]	**Name**	**Default**	**Description**
[14:10]	SPD_DOWN_STEP3	00001	The setting unit is r/min.
[9:5]	SPD_DOWN_STEP2	00001	The setting unit is r/min.
[4:0]	SPD_DOWN_STEP1	00001	The setting unit is r/min.

Address: 1Fh			
Bit[15:0]	**Name**	**Default**	**Description**
[14:10]	SPD_UP_STEP3	00001	The setting unit is r/min.
[9:5]	SPD_ UP _STEP2	00001	The setting unit is r/min.
[4:0]	SPD_ UP _STEP1	00001	The setting unit is r/min.

Address: 23h			
Bit[15:0]	**Name**	**Default**	**Description**
[14:0]	SPD_P1	0064H	The setting unit is r/min.

Address: 25h			
Bit[15:0]	**Name**	**Default**	**Description**
[14:0]	SPD_UP_P3	0064H	The setting unit is r/min.

Address: 26h			
Bit[15:0]	**Name**	**Default**	**Description**
[14:0]	SPD_DOWN_P3	0064H	The setting unit is r/min.

Position Control Mode

Clock Input Mode

In clock input mode (set CMD_MOD to 10 for the clock signal input), the IC controls the rotor position reference by detecting the input signal rising edge (see Figure 16). The rotor moves forward one step angle with one input clock pulse. In one angular sensor cycle, the total step angle number is programmable with the register bits NSTEP.

With a fixed number of input clock pulses, the rotation position angle of motor is controlled accordingly.

Set the step angle value with Equation (14):

$$\theta_{step} = \frac{NSTEP}{2^{14}} \times 360^{o} \quad (14)$$

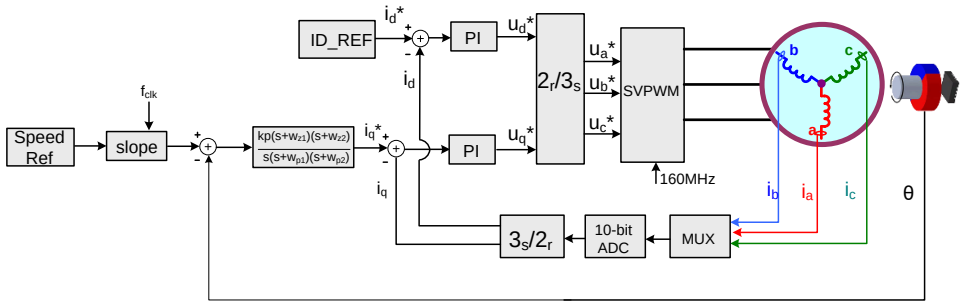


Figure 16: Position Control Block Diagram

Digital Interface Input Mode

In this mode, the position reference can be set by the internal register bits THETA_CMD.

The MP6570 can operate in either absolute position mode or relative position mode, which is set by THETA_CMD_TYPE.

Address: 01h			
Bit[15:0]	**Name**	**Default**	**Description**
[15:0]	THETA_CMD [15:0]	0000H	The position reference command THETA_CMD[15:0]. For positive reference setting: THETA_CMD[47:0] = 65536*x_cycle + x_theta / 360*65536 For negative reference setting: THETA_CMD[47:0] =2^{48} - 65536*x_cycle - x_theta /360*65536 x_theta: target position reference in one round (0° to 360°). x_ cycle: target position reference cycles beyond one round.

Address: 02h			
Bit[15:0]	**Name**	**Default**	**Description**
[15:0]	THETA_CMD [31:16]	0000H	The position reference command THETA_CMD [31:16].

Address: 03h			
Bit[15:0]	**Name**	**Default**	**Description**
[15:0]	THETA_CMD [47:32]	0000H	The position reference command THETA_CMD [47:32]. THETA_CMD [47] is the sign signal bit.

Address: 05h			
Bit[15:0]	**Name**	**Default**	**Description**
[14]	THETA_CMD_ TYPE	0	THETA_CMD_TYPE = 0: absolute position control THETA_CMD_TYPE = 1: relative position control

Position Reference Slope Control

When the position reference changes in digital input mode, the real position reference is smoothly controlled to avoid overshoot and inrush current (see Figure 17).

The speed reference slope is set by spd_step/time_step as shown in the sequence below.

1. During S1: spd_step is set by SPD_UP _STEP1 and time_step is set by SPD_STEP_TL.
2. During S2: spd_step is set by SPD_UP _STEP2 and time_step is set by SPD_STEP_TH.
3. During S3: spd_step is set by SPD_ DOWN _STEP2 and time_step is set by SPD_STEP_TH.

The register is the same as shown in the speed mode section.

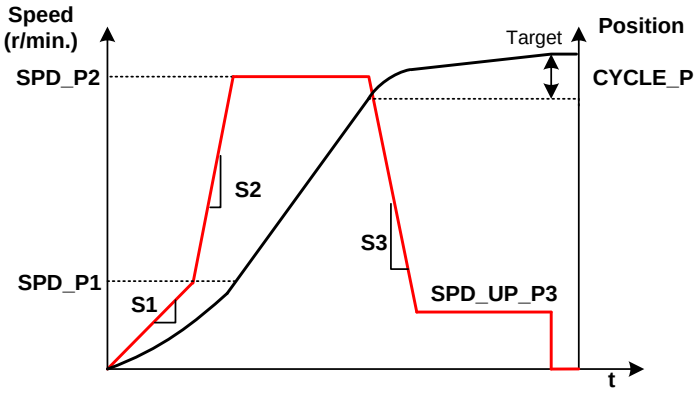


Figure 17: Position Reference Slope Control

Address: 04h			
Bit[15:0]	**Name**	**Default**	**Description**
[15:8]	CYCLE_P	01H	Defines the rounds left until the target position reference. During this time, the reference uses slow slope control to decrease the transient overshoot.

Address: 24h			
Bit[15:0]	**Name**	**Default**	**Description**
[14:0]	SPD_P2	03E8H	The setting unit is r/min.

Loop Compensation in Speed and Position Mode

It is recommended to use the MPS e.Motion Family Virtual Bench online developer tool for design. The loop compensation block diagram and general design guide are shown in Figure 18 and Figure 19, respectively.

The error limit between the reference and feedback position is set by ERR_LIMIT. For most applications, setting this to 180° (7FFF) is sufficient.

SAT_GAIN is set by SAT_GAIN1 and SAT_GAIN2. For most applications, set SAT_GAIN1 to 14H and set SAT_GAIN2 to 0AH.

IQ_LMT is the maximum IQ current reference limit.

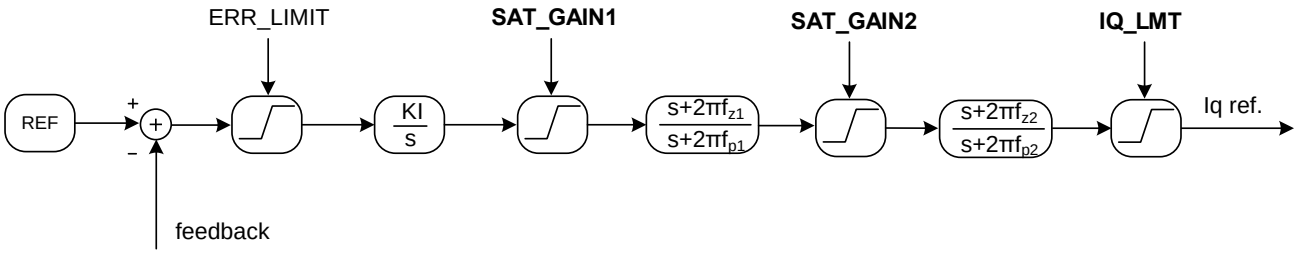


Figure 18: Loop Compensation Block Diagram

The integrator gain (KI) is set by THETA_KI_L, THETA_KI_H, and GAIN_COE. A starting loop setting can be set with Equation (15):

$$THETA\_KI\_L/H = 0.18 \cdot Ts(us) \cdot spd\_cont(rpm/V) \cdot gain\_ad \cdot J(g \cdot cm^2) \quad (15)$$

fz1 and fp1 are set by the ZP1_PARA_A and ZP1_PARA_B registers. fz1 is used to compensate for the system main pole. fz1 is recommended to be in the range of 0.1 - 2Hz. For most applications, 0.2Hz is sufficient. fp1 is recommended to be in the range of 20 - 200 * fz1. For most applications, 50Hz is sufficient. With a fixed fz1 value, a higher fp1 value provides higher system bandwidth.

ZP1_PARA_A and ZP1_PARA_B can be calculated with Equation (16) and Equation (17):

$$ZP1\_PARA\_A = \frac{1}{1 + 2\pi T_s \cdot f_{p1}} \cdot 2^{16} \quad (16)$$

$$ZP1\_PARA\_B = \frac{1 + 2\pi T_s \cdot f_{z1}}{1 + 2\pi T_s \cdot f_{p1}} \cdot 2^{16} \quad (17)$$

Where T_S is the switching period (i.e.: T_S = 20 * 10^{-6} @ 50kHz).

fz2 and fp2 is set by the ZP2_PARA_A and ZP2_PARA_B registers. fz2 is recommended to be in the range of 2 - 50Hz. For most applications, 5Hz is sufficient. A higher fz2 value provides a higher bandwidth but lower stability. fp2 is recommended to be in the range of 20 - 200 * fz2. For most applications, 1000Hz is sufficient. With a fixed fz2 value, a higher fp1 value provides a higher system bandwidth.

ZP2_PARA_A and ZP2_PARA_B can be calculated with Equation (18) and Equation (19):

$$ZP2\_PARA\_A = \frac{1}{1 + 2\pi T_s \cdot f_{p2}} \cdot 2^{16} \quad (18)$$

$$ZP2\_PARA\_B = \frac{1 + 2\pi T_s \cdot f_{z2}}{1 + 2\pi T_s \cdot f_{p2}} \cdot 2^{16} \quad (19)$$

Where T_S is switching period (i.e.: T_S = 20 * 10^{-6} @ 50kHz).

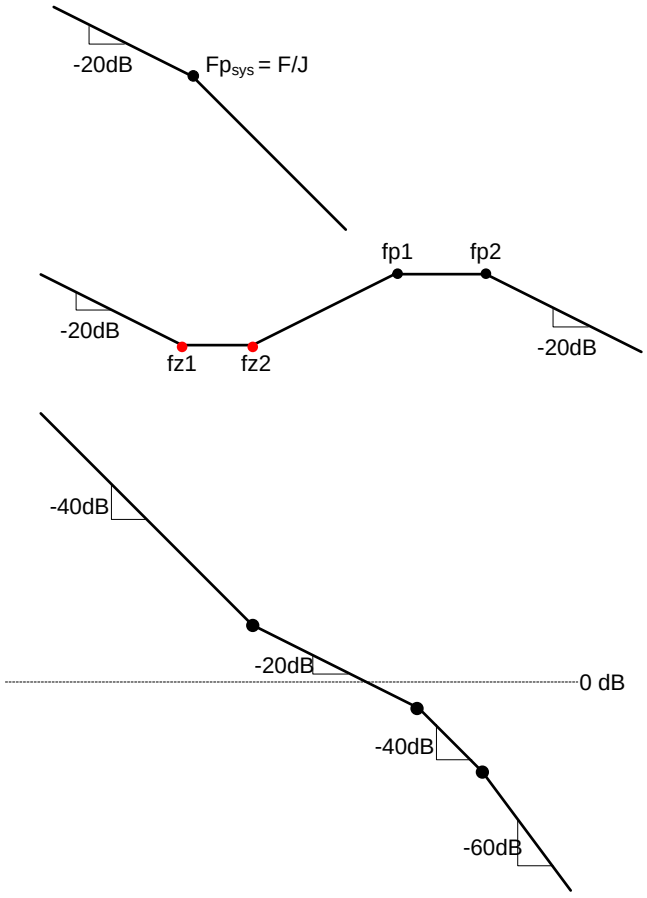


Figure 19: Loop Compensation Design Guide

Address: 06h			
Bit[15:0]	**Name**	**Default**	**Description**
[14:11]	GAIN_COE	0000	Defines the position/speed loop gain coefficient. GAIN_COE[2:0] is the gain coefficient (X). GAIN_COE[3] is the sign bit. 0: increase gain by 2^X 1: decrease gain by 2^X. For example: X000: gain coefficient is 1 0001: gain coefficient is 2 .... 0111: gain coefficient is 128 1001: gain coefficient is 1/2 ... 1111: gain coefficient is 1/128
[10:0]	IQ_LMT	352H	Defines the IQ current limit in speed or position control mode. IQ_LMT[10:0] is set according to: Iq_limit* sqrt(3/2)*gain_ad*1023/1.6 Where gain_ad is Rsense*Kad when ADMOD is set to 0, and gain_ad is Rpull/Kcs when ADMOD is set to 1. Kad: refer to the AD Gain description section. Kcs: current sense ratio. Refer to the MPS MP654x datasheet.

Address: 08h			
Bit[15:0]	**Name**	**Default**	**Description**
[15:0]	THETA_KI_L	0FA0H	Position/speed loop gain setting in steady stage.

Address: 09h			
Bit[15:0]	**Name**	**Default**	**Description**
[15:0]	THETA_KI_H	0FA0H	The position/speed loop gain setting in reference ramping up/down stage. Set it the same as THETA_KI_L.

Address: 0Ah			
Bit[15:0]	**Name**	**Default**	**Description**
[15:0]	ERR_LIMIT	7FFFH	Limit the angle error between reference and feedback in outer loop control. FFFF corresponds to 360°.

Address: 0Bh			
Bit[15:0]	**Name**	**Default**	**Description**
[15:0]	ZP1_PARA_A	FF32H	Defines the first zero and pole position for loop compensation together with ZP1_PARA_B[15:0].

Address: 0Ch			
Bit[15:0]	**Name**	**Default**	**Description**
[15:0]	ZP1_PARA_B	FF32H	Defines the first zero and pole position for loop compensation together with ZP1_PARA_A[15:0].

Address: 0Dh			
Bit[15:0]	**Name**	**Default**	**Description**
[15:0]	ZP2_PARA_A	DD43H	Defines the first zero and pole position for loop compensation together with ZP2_PARA_B[15:0].

Address: 0Eh			
Bit[15:0]	**Name**	**Default**	**Description**
[15:0]	ZP2_PARA_B	DD9BH	Defines the first zero and pole position for loop compensation together with ZP2_PARA_A[15:0].

Address: 0Fh			
Bit[15:0]	**Name**	**Default**	**Description**
[8:4]	SAT_GAIN1	0EH	Defines the gain limit of the second stage zero/pole filter. For most applications, it is sufficient to set this bit to 14H.
[3:0]	SAT_GAIN2	07H	Defines the gain limit of the second stage zero/pole filter. For most applications, it is sufficient to set this bit to 0AH.

Loop Decoupling

The d/q axis decoupling is set through LD_COE, LQ_COE, and PHIR_COE if needed. It is recommended to use the MPS e.Motion Family Virtual Bench for ease of design (see Figure 20).

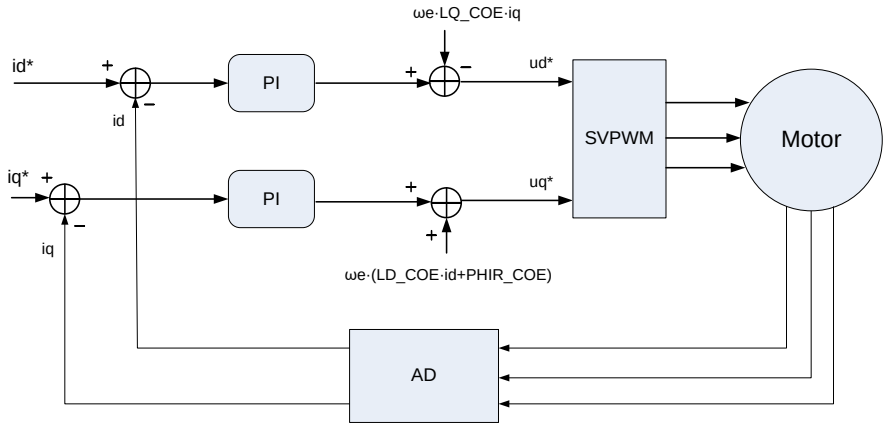


Figure 20: Loop Decoupling

Address: 14h			
Bit[15:0]	**Name**	**Default**	**Description**
[15:0]	LD_COE	0000H	Ld coefficient for loop decoupling. Set to 0 if not used.

Address: 15h			
Bit[15:0]	**Name**	**Default**	**Description**
[15:0]	LQ_COE	0000H	Lq coefficient for loop decoupling. Set to 0 if not used.

Address: 16h			
Bit[15:0]	**Name**	**Default**	**Description**
[15:0]	PHIR_COE	0000H	Rotor flux (ψ_r) coefficient for loop decoupling. Set to 0 if not used.

Direction Control

The MP6570 controls the motor direction through the DIR input signal on the DIR pin with the reference signal selected to be either PWM (set CMD_MOD to 01) or clock input mode (set CMD_MOD to 10).

If the reference signal is selected to the register input mode (set CMD_MOD to 00), the direction is controlled through the MSB bit of the position or speed reference register setting.

ADC Sample and Hold

The MP6570 provides real-time accurate signal sampling through a 10-bit ADC. The ADC reference is 1.6V. The clock frequency of the ADC is 20MHz (see Figure 21).

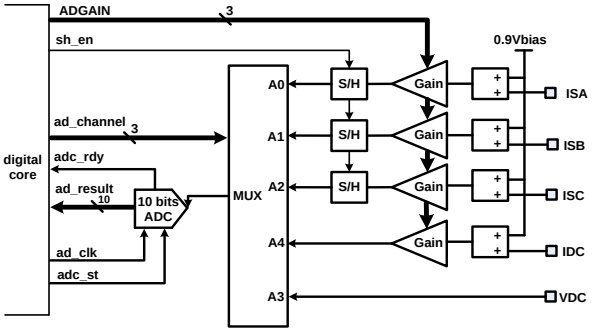


Figure 21: ADC Module Block Diagram

The MP6570 supports two types of connection for external current sample and bias. This is controlled by register bit AD_MOD.

The sample and hold signal is always active at the center of the on-time interval of the low-side MOSFETs except in single resistor sensing mode (SAM_MOD = 11). The sample-hold duration time is set by the register bits SH_CMP, and the delay time caused by the PWM gate driver is set by the SH_DELAY bits. The maximum on time (set by MAX_PERIOD) of the high-side MOSFETs should be set to provide enough time for the sample and hold time of the current signal (see Figure 22).

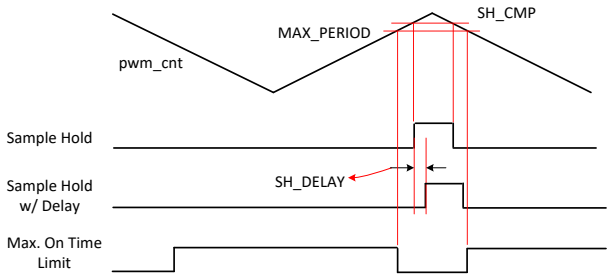


Figure 22: ADC Sample and Hold

Current Sensing Signal

If the external signal is a current source type, the connection shown below is recommended (AD_MOD = 1). This connection type is compatible with MPS power stage solutions, such as the MP654x family. Taking the ISA pin as an example, the gain is programmable with a resistor (R_b), and the bias voltage of the ADC input is 900mV (see Figure 23).

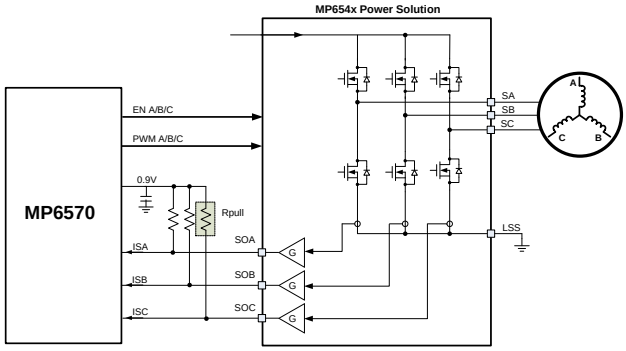


Figure 23: Current Sensing

The signal for the ISA sample can be calculated with Equation (20):

$$V_{ISA} = 0.9 - I_{SOA} \times R_{pull} \quad (20)$$

Voltage Sensing Signal

If the external signal is a voltage source type directly from a sensing resistor node, the connection shown in Figure 24 is recommended (AD_MOD = 0). Taking the ISA pin as an example, the gain is programmable with the internal register bits ADGAIN to increase the ADC resolution. The bias voltage for the current signal is 900mV.

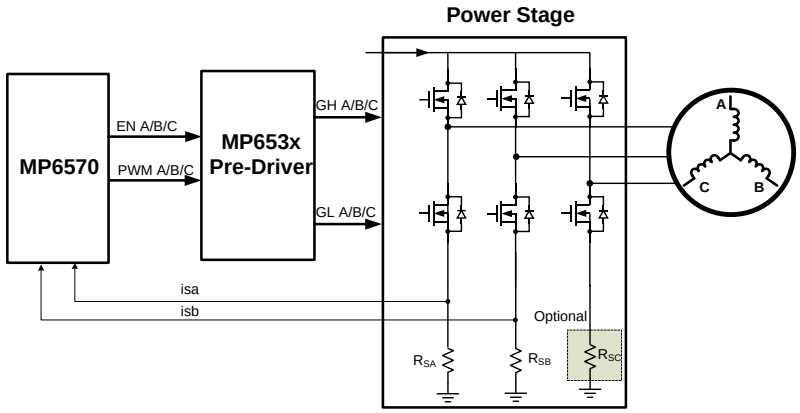


Figure 24: Voltage Signal Sensing

Address: 19h			
Bit[15:0]	**Name**	**Default**	**Description**
[14:7]	SH_DELAY	18H	Defines the sample hold delay time of sample-hold signal. The value is set by SH_DELAY * 12.5ns.

Address: 1Ah			
Bit[15:0]	**Name**	**Default**	**Description**
[15:0]	SH_CMP	07B7H	Defines the comparator counter value to generate the sample-hold signal. The sample-hold duration window is (PERIOD – SH_CMP) * 12.5ns.

Address: 30h			
Bit[15:0]	**Name**	**Default**	**Description**
[3]	AD_MOD	0	Defines the AD sample mode. 0: voltage signal input mode for ADC sample 1: current signal input mode for ADC sample
[2:0]	AD_GAIN	000	Defines the AD gain setting in voltage-signal input mode. ADGAIN = 000: Kad= 12X, $V_{ADC\_IN} = V_{ISA} * 12 + 900mV$ ADGAIN = 001: Kad = 8X, $V_{ADC\_IN} = V_{ISA} * 8 + 900mV$ ADGAIN = 010: Kad = 7X, $V_{ADC\_IN} = V_{ISA} * 7 + 900mV$ ADGAIN = 011: Kad = 6X, $V_{ADC\_IN} = V_{ISA} * 6 + 900mV$ ADGAIN = 100: Kad = 5X, $V_{ADC\_IN} = V_{ISA} * 5 + 900mV$ ADGAIN = 101: Kad = 4X, $V_{ADC\_IN} = V_{ISA} * 4 + 900mV$ ADGAIN = 110: Kad = 3X, $V_{ADC\_IN} = V_{ISA} * 3 + 900mV$ ADGAIN = 111: Kad = 2X, $V_{ADC\_IN} = V_{ISA} * 2 + 900mV$
dress: 1Ah			
Bit[15:0]	**Name**	**Default**	**Description**
[15:0]	SH_CMP	07B7H	Defines the comparator counter value to generate sample hold signal. The sample-hold duration window is (PERIOD - SH_CMP) * 12.5ns.

Current Signal Bias Auto-Sample

The bias voltage (900mV) for current signal is auto-sampled by the ADC during start-up when BIAS_SEL is set to 0. The bias voltage of the A/B/C channel signals can be input manually when BIAS_SEL is set to 1. In this mode, the bias is set through CUR_BIASA, CUR_BIASB and CUR_BIASC.

Address: 2Dh			
Bit[15:0]	**Name**	**Default**	**Description**
[10]	BIAS_SEL	0	1: non-auto bias mode 0: auto-bias mode
[9:0]	CUR_BIASA	200H	Defines the bias setting of ADC result for the phase A current sample.

Address: 2Eh			
Bit[15:0]	**Name**	**Default**	**Description**
[9:0]	CUR_BIASB	200H	Defines the bias setting of ADC result for the phase B current sample.

Address: 2Fh			
Bit[15:0]	**Name**	**Default**	**Description**
[9:0]	CUR_BIASC	200H	Defines the bias setting of ADC result for the phase C current sample.

Current Connection Mode

Different phase currents of windings A/B/C can be used for the ADC sampling. The mode is set by the register bits SAM_MOD.

Three-Phase Sensing

If SAM_MOD = 00, three phases of A/B/C are connected for current sampling. The sample sequence is $I_{SA}/I_{SB}/I_{SC}/V_{DC}/I_{DC}$.

Two-Phase Sensing

If SAM_MOD = 01, only two phases of A/B must be connected for current sampling. The sample sequence is $I_{SA}/I_{SB}/V_{DC}/I_{DC}$.

Single-Resistor Sensing

With SAM_MOD = 10, the connection shown in Figure 25 is recommended for current sampling. The sample sequence is $I_{SA}/V_{DC}/I_{DC}$. In this mode, the ADC samples the current from the ISA pin and the result is transferred internally to the phase A/B/C current.

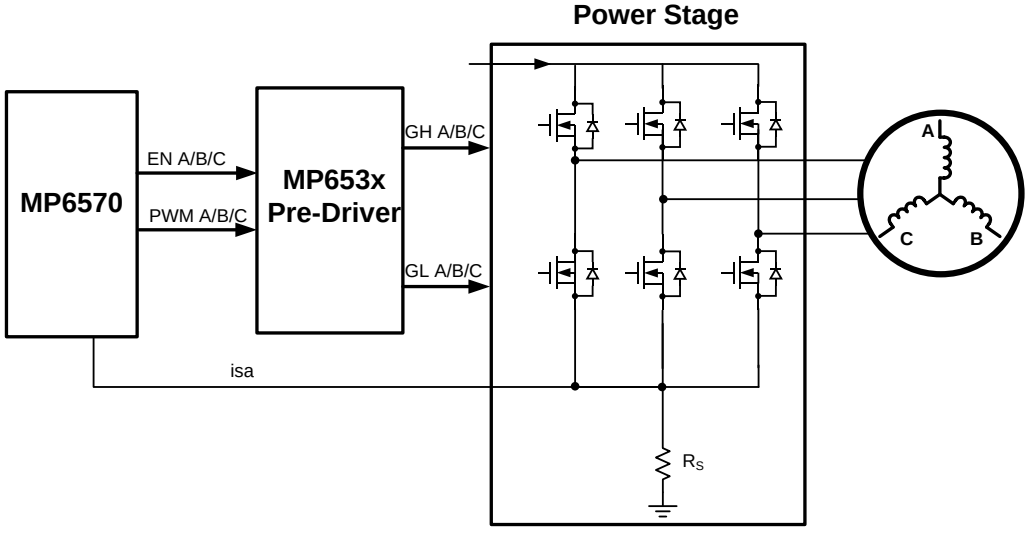


Figure 25: Single-Resistor Sensing

Address: 1Bh			
Bit[15:0]	**Name**	**Default**	**Description**
[15:8]	MIN_DELTA_CMP	50H	Defines the minimum time interval for adjacent PWM switching. This bit is only active in single-resistor sample mode. The value is set by MIN_DELTA_CMP * 25ns.
[7:0]	SWITCH_BLANK_TIME	06H	Defines the blanking time between the low-side MOSFET turn-on and sample hold active this. This bit is only active in single-resistor sample mode. The value is set by TBLANK *25ns.

Address: 33h			
Bit[15:0]	**Name**	**Default**	**Description**
[9:8]	SAM_MODE	00	Defines the sample mode. 00: three-phase current sample mode 01: two-phase current sample mode 10: single-resistor current sample mode

Bus Voltage Sample

To control the input bus voltage, use a resistor divider from the bus voltage to GND and connect the center node to the VDC pin directly.

SVPWM Module

The PWM module uses a 160MHz clock oscillator to increase the PWM resolution. The PWM resolution is dependent on the switching frequency. The PWM resolution has a 12-bit resolution when the switching frequency is ≤20kHz. The switching frequency is set by the PERIOD register bits.

Address: 17h			
Bit[15:0]	**Name**	**Default**	**Description**
[15:0]	PERIOD	07CFH	Defines the switching frequency period. The switching frequency period is (PERIOD + 1) * 12.5ns. The allowed maximum frequency is 80kHz. The minimum frequency is 1.22kHz.

Address: 18h			
Bit[15:0]	**Name**	**Default**	**Description**
[15:0]	MAX_ON_TIME	780H	Defines the maximum on time of the PWM output. PERIOD ≥ 2^{15}: max on time is MAX_ON_TIME * 200ns 2^{14} ≤ PERIOD < 2^{15}: max on time is MAX_ON_TIME * 100ns 2^{13} ≤ PERIOD < 2^{14}: max on time is MAX_ON_TIME * 50ns 2^{12} ≤ PERIOD < 2^{13}: max on time is MAX_ON_TIME * 25ns PERIOD < 2^{12}: max on time is MAX_ON_TIME * 12.5ns

The MP6570 supports two kinds of PWM driver signals for a three-phase bridge. This is controlled by the register bit PWM_MOD.

Mode 1

With PWM_MOD set to 0, $EN_A/EN_B/EN_C$ controls each phase independently. EN logic high enables the phase driver logic. EN logic low disables the phase driver logic. PWM high logic turns on the high-side MOSFET. PWM low logic turns on the low-side MOSFET. Table 2 shows the detail of the control logic. This mode is compatible with MP653x/4x family parts. The dead time is controlled by the MP653x/4x parts.

Table 2: Control Logic

EN_X	PWM_X	SW_X
H	H	VIN
H	L	GND
L	X	High Impedance

Mode 2

By setting PWM_MOD to 1, the MP6570 outputs six separate PWM signals for a three-phase bridge driver. Logic high on each gate output signal causes the MOSFET on state, and logic low on each gate output signal causes the MOSFET off state. The dead time of each PWM phase is set by the internal register bits DTPWM.

The signal logic is shown in Figure 26.

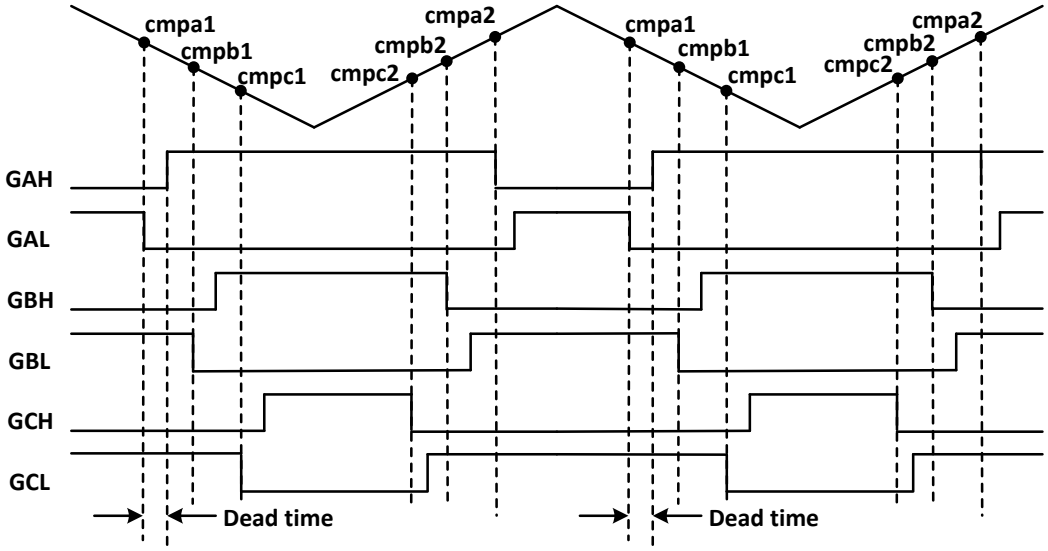


Figure 26: Mode 2 Signal Logic

Address: 19h			
Bit[15:0]	**Name**	**Default**	**Description**
[6:0]	DTPWM	000H	Defines the dead time of each phase in a separate PWM control mode. The value is set by (DTPWM * 25 + 12.5)ns.

Address: 33h			
Bit[15:0]	**Name**	**Default**	**Description**
[7]	PWM_MOD	0	Defines the 3-phase bridge PWM driver output mode. 0: EN and PWM combination mode, which is compatible with MPS MP65XX family parts. 1: outputs six separate PWM signals to drive the three-phase bridge MOSFETs.

Brake Mode

The brake signal input can come from either the internal BRAKE bit or the external signal on the BRAKE pin. This is selected by the register EXBRK bit. In brake mode, the MP6570 supports three modes to stop the motor rotation. The brake mode selection is done by setting the register bits BRK_MOD.

Coasting-Brake Mode

BRK_MOD = 00. When the brake signal is activated, all MOSFET driver outputs are turned off to set the phase A/B/C switching nodes to a high impedance. The energy stored in the motor winding and rotor is consumed by thermal dissipation and mechanical friction. This mode takes the longest time to stop the motor.

Fast-Brake Mode

BRK_MOD = 01. When the brake signal is activated, all low-side MOSFET driver outputs are turned on, and the phase A/B/C switching nodes are pulled to GND. This mode stops the motor rotation quickly, but the MOSFETs of the power stage must suppress the resultant large current spike.

Energy-Regeneration Brake Mode

BRK_MOD = 10: when the brake signal is activated, the motor brake is close-loop controlled with a negative torque current (IQ). IQ is programmable with the internal register bits BRK_IQ. When the speed is lower than the speed set by bits BRK_STOP_SPD, the brake mode turns to fast-brake mode, and all low-side MOSFETs are turned on to brake the motor to stop status.

In this mode, the energy stored in the motor is mostly regenerated back to the input power bus. Additionally, the rotor braking time is programmable via the torque current.

Address: 2Bh			
Bit[15:0]	**Name**	**Default**	**Description**
[11:0]	BRK_IQ	E02H	Defines the brake current reference in energy-regeneration brake mode. When i_{brake} is positive, BRK_IQ [11:0] = i_{brake} * sqrt(3/2) * gain_ad * 1023 /1.6 When i_{brake} is negative, BRK_IQ [11:0] = 4096 - abs(i_{brake}) * sqrt(3/2) * gain_ad * 1023/1.6 Where gain_ad is Rsense * Kad when ADMOD is set to 0, and gain_ad = Rpull/Kcs when ADMOD is set to 1. Kad is set by AD_GAIN in the ADC section, and Kcs is the current sense ratio. Refer to the MPS MP654x datasheet.

Address: 2Ch			
Bit[15:0]	**Name**	**Default**	**Description**
[15]	BRAKE	0	Internal brake enable register bit. 0: no brake 1: brake
[14:0]	BRK_STOP_SPD	0064H	Defines the minimum speed threshold in energy-regeneration brake mode. When the motor speed is less than this speed threshold, the IC exits energy-regeneration brake mode and switches to coasting-brake mode with all MOSFETs off.

Address: 33h			
Bit[15:0]	**Name**	**Default**	**Description**
[6:5]	BRK_MOD	00	00: coasting-brake mode with all MOSFETS off when braked 01: fast-brake mode with all low-side MOSFETS on when braked 10: energy-regeneration brake mode with close-loop control when braked
[3]	EXBRK	0	0: use internal register bit to enable brake mode 1: use external BRAKE pin signal to enable brake mode

FG/HOME Output Indication

By setting the FGHOME bit to 1, the MP6570 outputs a rotor speed signal through the FG/HOME pin. In one angular sensor cycle, the FG frequency can be set to 1, 2, 4, 8, 16, or 32 times by setting the register bits FG_SEL.

When setting the FGHOME bit to 0, the MP6570 outputs a rotor home indication signal through the FG/HOME pin. The signal remains at logic high when the angular sensor angle is between the HOME_P1 and HOME_P2 setting values.

Address: 05h			
Bit[15:0]	**Name**	**Default**	**Description**
[13:9]	FGSEL	00000	FGSEL[4:0] defines the (FG) number of pulses for the speed indication signal per angular sensor cycle. 5'd0: 32 pulses per cycle 5'd1: 16 pulses per cycle 5'd3: 8 pulses per cycle 5'd7: 4 pulses per cycle 5'd15: 2 pulses per cycle 5'd31: 1 pulse per cycle

Address: 31h			
Bit[15:0]	**Name**	**Default**	**Description**
[15:0]	HOME_P1	0800H	The lower threshold to output the HOME signal as the rotor position indication. The HOME signal is high when the rotor position is between HOME_P1 and HOME_P2.

Address: 32h			
Bit[15:0]	**Name**	**Default**	**Description**
[15:0]	HOME_P2	0C00H	The upper threshold to output the HOME signal as the rotor position indication.

Address: 33h			
Bit[15:0]	**Name**	**Default**	**Description**
[14]	FGHOME	0	1: FG/HOME pin outputs a FG signal 0: FG/HOME pin outputs a HOME signal

Fault Management

The MP6570 has robust protection to avoid unexpected failure modes and external component damage. For each protection mode described below, the protection mode can be set to latch-off or hiccup mode through the register FTRT bit.

Over-Current Protection (OCP)

By sensing the phase current in the three-phase bridge with the 10-bit ADC, the maximum current limit of the phase current is programmable. When the phase current exceeds the current limit set by the register bits IOCP, all MOSFET gate drives are disabled. They are automatically re-enabled after the timer value, which is set by FAULT_RT. During an OCP event, the OCP bit is set to 1, and the fault indication pin (nFT) is pulled low. This bit is not reset until the fault mode is clear.

Rotor-Lock Protection

A rotor-lock fault occurs in the event of a mechanical jam or excessive load torque, which causes the motor to stop rotating. The rotor-lock condition is detected if the FG signal or bit has no transition during the 1s/2s/4s/8s time set by the register bits LOCK_DET. When a rotor lock condition is asserted, the MP6570 stops switching and restarts automatically after the time set by register bits LOCK_RT. During a rotor lock event, the RLOCK bit is set to 1, and the fault indication pin (nFT) is pulled low. This bit is not reset until the fault mode is clear. The rotor-lock protection function can be disabled by LOCK_EN if it is not needed.

External Fault Input

In normal operation without any fault, nFT is kept in an open-drain state. If nFT is pulled low via an external input (i.e.: power stage fault), the MP6570 sets the internal PSFT bit to 1 and shuts down the PWM driver output. The MP6570 retries automatically after the time set by FAULT_RT.

Fault Indication Output

When any fault occurs, nFT is pulled low. After normal operation is resumed, nFT resumes its open-drain state, and the register bit nFT is cleared.

Address: 27h			
Bit[15:0]	**Name**	**Default**	**Description**
[9:0]	IOCP	3FFH	The motor winding current over-current limit setting. The protection threshold current is IOCP[9:0]/(sqrt(3/2)*gain_ad*1023/1.6) Where gain_ad is Rsense*Kad when ADMOD is set to 0, and gain_ad is Rpull/Kcs when ADMOD is setting to 1. Kad is set by AD_GAIN in the ADC section. Kcs is the current sense ratio. Refer to the MPS MP654x datasheet.

Address: 28h			
Bit[15:0]	**Name**	**Default**	**Description**
[9]	FTRT	0	0: latch-off mode when any fault occurs 1: auto-recovery mode when any fault occurs
[8]	LOCK_EN	0	Rotor-lock protection enable bit. 0: disable 1: enable
[7:5]	LOCK_DRT	0000	The rotor-lock fault retry timer. 000: 2s 001: 4s 010: 6s 011: 8s 100: 10s 101: 12s 110: 14s 111: 16s
[4:2]	FAULT_RT	000	The fault retry timer window. A timer starts whenever a fault occurs. If the fault protection is set to auto-recovery mode, the IC restarts after this timer window expires. 000: 200ms 001: 400ms 010: 600ms 011: 800ms 100: 1000ms 101: 2000ms 110: 4000ms 111: 8000ms
[1:0]	LOCK_DET	00	The rotor-lock detection timer window. 00: 0.5s 01: 1s 10: 2s 11: 4s

Input Bus Protection

Input bus voltage protection is enabled by the register bit VINPEN, and the threshold is set by the register bits VIN_LIMIT. The input bus current protection is enabled by the register bit IINPEN, and the threshold is set by the register bits IIN_LIMIT. When the input voltage or current exceeds the setting threshold, the control signal on VINCON is set to output high to turn on the external MOSFET.

The input bus voltage protection threshold is set according to Equation (21):

$$VIN\_LIMIT[7:0] = VIN_{sense}*255/1.6 \quad (21)$$

Where VIN_{sense} is the sensing voltage of the bus voltage for the VDC pin.

The input bus current protection threshold is set according to Equation (22):

$$IIN\_LIMIT[9:0] = (Vs+0.9)*1023/1.6 \quad (22)$$

Where Vs is the sensing voltage of the bus current for the IDC pin.

The function operation block is shown in Figure 27.

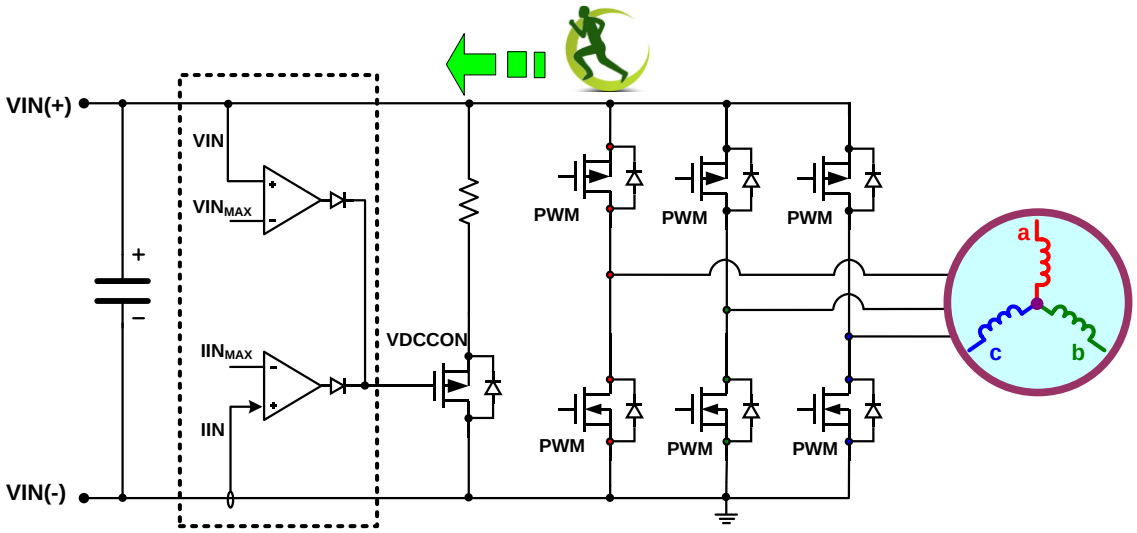


Figure 27: Input Bus Protection

Address: 29h			
Bit[15:0]	**Name**	**Default**	**Description**
[8:1]	VIN_LIMIT	9BH	Defines the input bus voltage protection threshold. The input voltage protection threshold is VIN_LIMIT*1.6/255/K_{VIN} Where K_{VIN} is resistor divider gain from VIN from the ADC sample.
[0]	VINPEN	0	The input bus voltage protection enable bit. 0: disable 1: enable

Address: 2Ah			
Bit[15:0]	**Name**	**Default**	**Description**
[10:1]	IIN_LIMIT	1E0H	Defines the input current protection threshold. The input protection threshold is set according to: IIN_LIMIT[9:0] = (Vs+0.9)*1023/1.6 Where Vs is the input current sensing voltage.
[0]	IINPEN	0	The input current protection enable bit. 0: disable 1: enable

Clock Oscillator

The MP6570 supports two modes for the internal clock reference by detecting the XTAL1 and XTAL2 pin connections during power-up.

The first is internal clock mode when XTAL1 is connected to ground and XTAL2 is float. In this mode, the MP6570 generates a 160MHz clock internally.

The second option is to use an external crystal. In this way, the MP6570 provides a very accurate clock. An accurate 10MHz crystal is needed between pins XTAL1 and XTAL2 (see Figure 28). Refer to the crystal component datasheet for correct Rx and Cy value selection. Typical value are Rx = 1MΩ and Cy = 15pF.

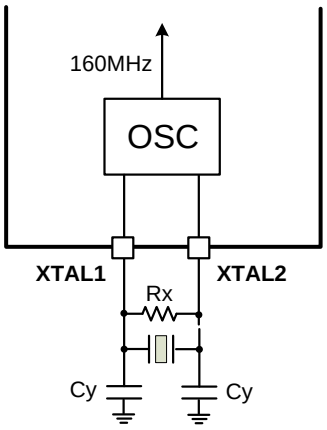


Figure 28: MP6570 with External Crystals

The internal PLL clock can be enabled or disabled with the command operations below.

- Write 0000H to register 62H to enable the clock.
- Write 0000H to register 63H to disable the clock to reduce power.

Non-Volatile Memory (NVM)

All parameters programmed and stored in the non-volatile memory are automatically downloaded to the MP6570 RAM after power-on or EN reset. The available operation commands are shown below:

- Write 0000H to register 64H to save data from the RAM to the NVM.
- Write 0000H to register 65H to load data from the NVM to the RAM.
- Write 0000H to register 66H to clear the memory fault state bit.

The memory section to be programmed is controlled through setting bits MEM_SECTION.

Address: 51h			
Bit[15:0]	**Name**	**Default**	**Description**
[1:0]	MEM_SECTION	00	Defines the section of the NVM to be programmed. 00: 00h ~ 4Fh 01: 33h ~ 3Fh 10: 40H ~ 4Fh 11: 00h ~ 32h

IC Enable/Disable

The MP6570 can be enabled or disabled using SBD_EN.

When SDB_EN = 1, pull EN high to make the IC enter standby mode with only the digital interface active. Write 0000H to register 60H to make the IC enter normal operation mode. Then write 0000H to register 61H to make the IC enter standby mode.

When SDB_EN = 0, pull EN high to make the IC enter normal operation mode. Pull EN low to make the IC enter shutdown mode.

Address: 33h			
Bit[15:0]	**Name**	**Default**	**Description**
[15]	SDB_EN	1	0: IC goes to run state by pulling EN high 1: IC goes to run standby mode by pulling EN high

Initial Rotor Positioning

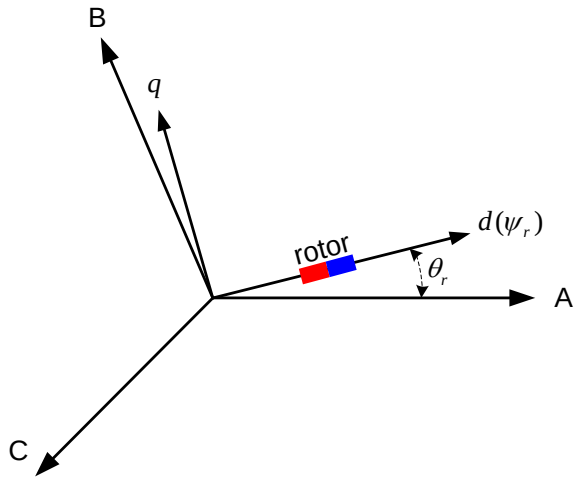


Figure 29: Initial Rotor Positioning

In the FOC d/q calculation, the position data (θ_r) is the relative angle difference between the sensor output of the current rotor position and the sensor output when the rotor aligns with the phase A winding. At the system construction time when the two-pole magnet is first attached to the rotor shaft and the sensor PCB mounted, the poles of the magnet are not aligned to the poles of the rotor magnets. Therefore it is necessary to find the offset value (THETA_BIAS) so the sensor angle output can be corrected to the true position when the rotor aligns with the phase A winding (see Figure 29).

This can be done by two methods: using the MPS e.Motion Family Virtual Bench tool to get the initial position automatically, or by experimentation.

When experimenting, follow the procedure below.

1. Power up the motor winding A+B- and position the rotor. Then read the sensor data through THETA_M (register 55h), calling the result θ_{AB}.
2. Power up the motor winding A+C- and position the rotor. Then read the sensor data through THETA_M (register 55h), calling the result is θ_{AC}.
3. If the data value is increasing from θ_{AB} to θ_{AC}, set register bit THETA_DIR to 0. If the data value is decreasing from θ_{AB} to θ_{AC}, exchange the winding B and winding C, and redo steps 1 and 2.
4. Save (θ_{AB} + θ_{AC}) / 64 to register THETA_BIAS (register 07h).

This procedure is shown in Figure 30.

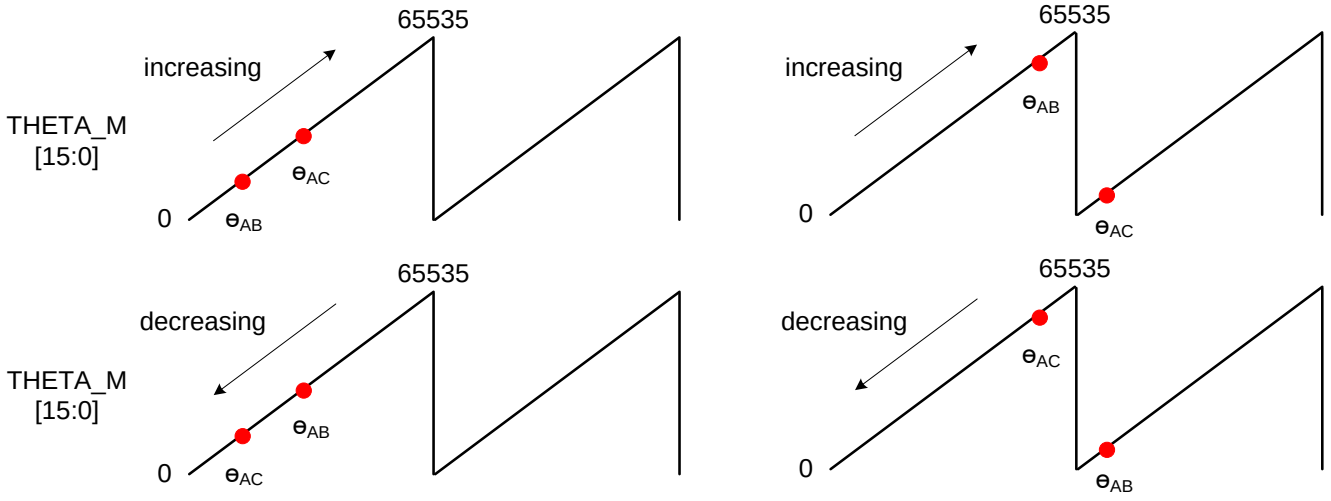


Figure 30: Initial Rotor Position Calculation

Address: 05h			
Bit[15:0]	**Name**	**Default**	**Description**
[15]	THETA_DIR	0	0: IC uses the original data value from the angular sensor 1: IC uses the complementary data value from the angular sensor

Address: 07h			
Bit[15:0]	**Name**	**Default**	**Description**
[10:0]	THETA_BIAS	4BCH	Defines the initial rotor position when the rotor flux is aligned with the winding A current.

Address: 51h			
Bit[15:0]	**Name**	**Default**	**Description**
[11:0]	CMPA_SET	000H	Defines the constant duty of PWMA.

Address: 52h			
Bit[15:0]	**Name**	**Default**	**Description**
[12:1]	THETA_BIAS_TIME	000H	Defines the orientation time when detecting the initial angle of the sensor.
[0]	THETA_BIAS_EN	0	0: disable 1: enable

Communication Interface

Slave Address and Communication Mode

The MP6570 supports up to 32 slave address, which are programmable through SLV_ADDR_SET. The communication mode supports I^2C, SPI, and RS485 mode, which is set by COM_MOD.

Address: 33h			
Bit[15:0]	**Name**	**Default**	**Description**
[2:1]	COM_MODE	00	0: sets I^2C interface as communication bus 1: sets SPI interface as communication bus 2: sets RS485 interface as communication bus
[0]	SPI_O_MOD	0	0: SDO signal open-drain output 1: SDO signal push-pull output

Address: 3Bh			
Bit[15:0]	**Name**	**Default**	**Description**
[11:7]	SLV_ADDR_SET	00000	Defines the IC slave address. See the address table below.

Address: 3Bh			
SLV_ADDR_SET	**Slave Address**	**SLV_ADDR_SET**	**Slave Address**
0 0000	12H	1 0000	52H
0 0001	13H	1 0001	53H
0 0010	18H	1 0010	58H
0 0011	19H	1 0011	59H
0 0100	1AH	1 0100	5AH
0 0101	1BH	1 0100	5BH
0 0110	1CH	1 0110	5CH
0 0111	1DH	1 0111	5DH
0 1000	1EH	1 1000	5EH
0 1001	1FH	1 1001	5FH
0 1010	20H	1 1010	60H
0 1011	21H	1 1011	61H
0 1100	22H	1 1100	62H
0 1101	23H	1 1101	63H
0 1110	24H	1 1110	64H
0 1111	25H	1 1111	65H

I²C Interface

If the COM_MOD[1:0] bits are set to 00, the I²C interface is selected to write or read the register values. The MP6570 uses standard I²C protocol to write/read the RAM registers and non-volatile memory.

Figure 31 details the various I²C protocols supported by the MP6570. The supported protocols include word write and word read. The communication clock is supported with a maximum frequency of 1000kHz.

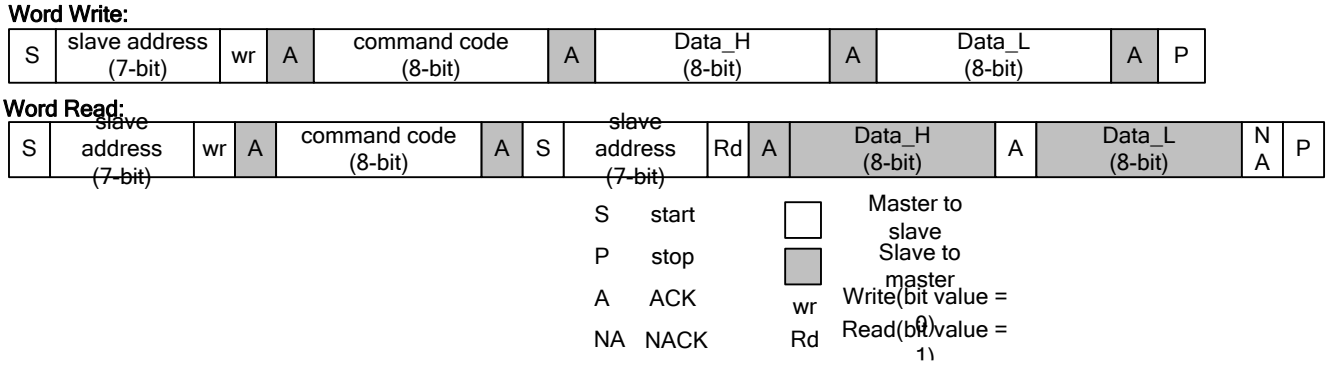


Figure 31: I²C Read/Write Protocol

SPI Port 1 Interface

If the COM_MOD[1:0] bits are set to 01, the SPI port 1 interface is selected. The device can be configured as a slave with programmable device addresses. The SDO data output pin is selectable with push-pull and open-drain modes, which are set through bit SPI_O_MOD (33h).

Both the master and slave send data at the clock falling edge and receive data at the clock rising edge. The communication clock is supported with a maximum frequency 24MHz.

Figure 32 and Figure 33 detail the various SPI protocols supported by the MP6570.

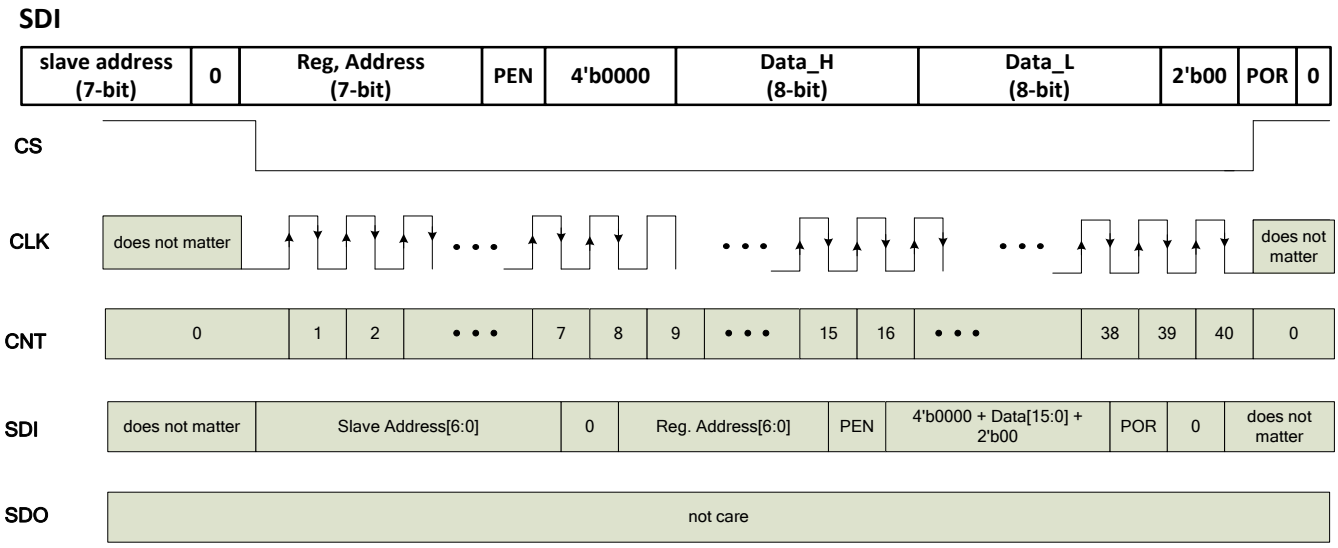


Figure 32: Word Write Command

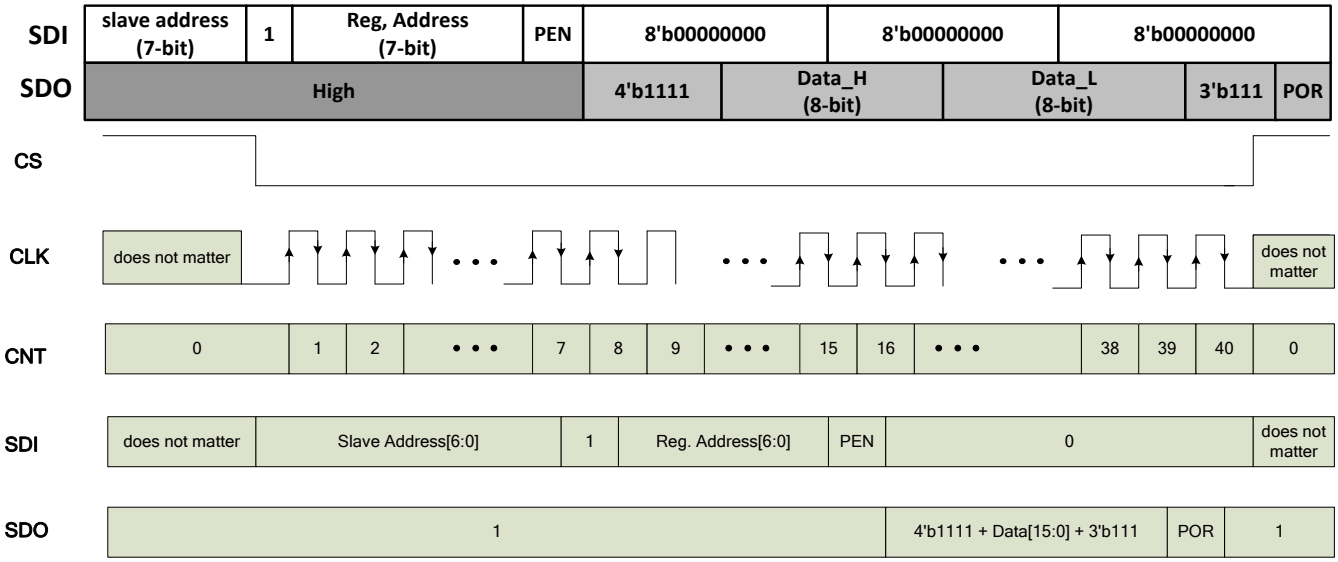


Figure 33: Word Read Command

Where PEN is the polarity enable bit, and POR is the polarity data bit when the data polarity check is enabled.

When PEN is set to 1, data polarity check is enabled. When PEN is set to 0, data polarity check is disabled.

When POR is set to 1, all other bits on SDI have an odd-bit 1. When POR is set to 0, all other bits on SDI have an even-bit 1.

RS485 Interface

If the COM_MOD[1:0] bits are set to 10, the RS485 compatible interface is selected. In this mode, the TX output signal must be set to push-pull mode by setting bit SPI_O_MOD = 1.

The following protocol shows the top-level data frame protocol supported by the MP6570. The MP6570 DE and REN pins are compatible with an RS485 protocol transceiver. The communication baud rate is programmable with the BAUD_RATE[12:0] (register 34h) register bits. The internal signal sampling clock is fixed at 40MHz. A maximum 40MHz/16 baud rate is recommended (see Figure 34).

Supported protocols include word write command and word read command (see Figure 35 and Figure 36).

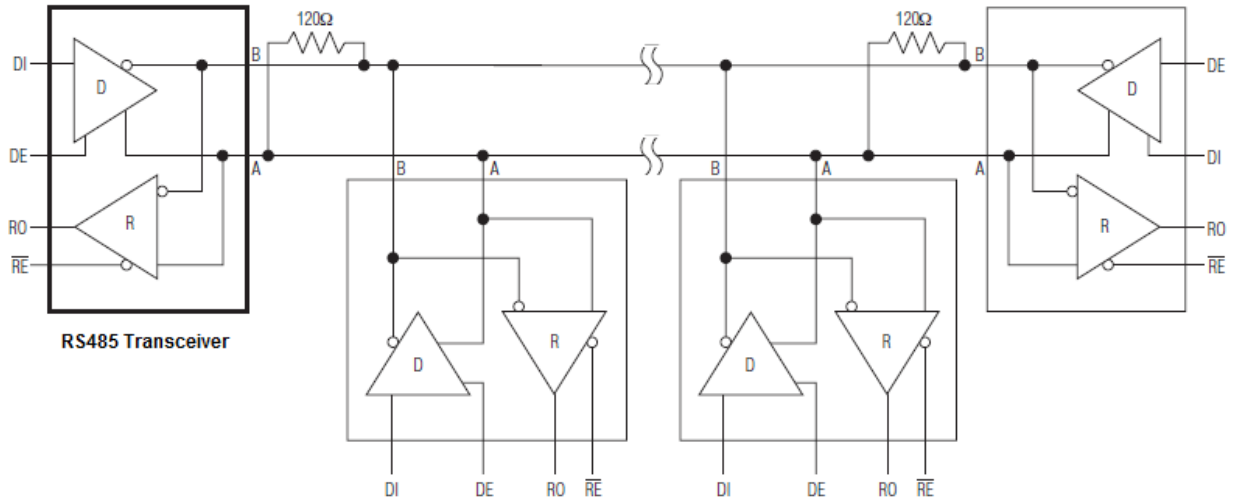


Figure 34: RS485 Interface

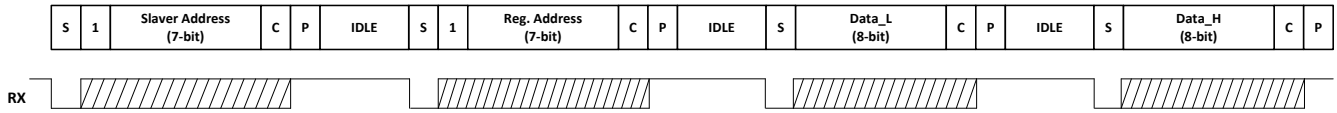


Figure 35: Word Write Command

The data communication order is LSB of the data first and MSB of the data last.

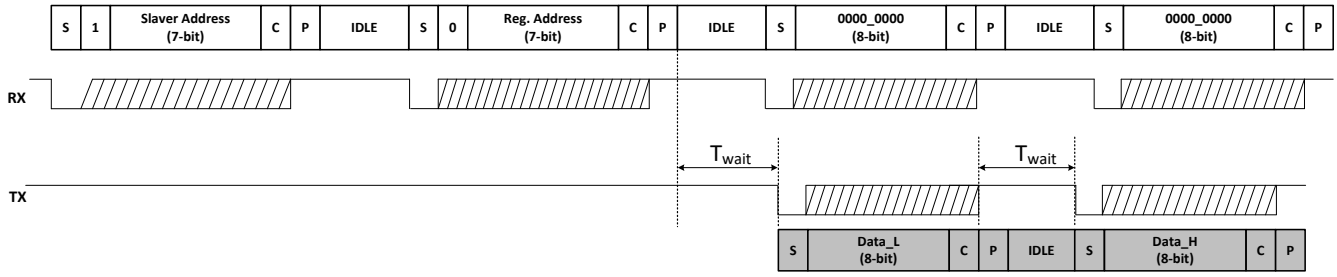


Figure 36: Word Read Command

Where T_{wait} is programmable from 200ns to 25.6µs. The data communication order is LSB of the data first and MSB of the data last.

Address: 33h			
Bit[15:0]	**Name**	**Default**	**Description**
[0]	SPI_O_MOD	0	0: SPI SDO signal open-drain output 1: SPI SDO signal push-pull output

Address: 34h			
Bit[15:0]	**Name**	**Default**	**Description**
[12:0]	BAUR_RATE	0027H	Sets the baud rate of RS485. BAUR_RATE[12:0] = 40000000/f_{bps} - 1 Where f_{bps} (bit/s) is target baud rate.

Address: 3Bh			
Bit[15:0]	**Name**	**Default**	**Description**
[6:0]	UART_IDLE_TIME	00H	Defines the T_{WAIT} time during a read operation. T_{WAIT} time is (UART_IDLE_TIME+1) * 200ns

Read-Only Register

Address: 53h				
Bit[15:0]	**Bit Name**	**Access**	**Default**	**Description**
[15:4]	N/A			
[3]	LOCK_FLAG	r		Lock fault indication bit.
[2]	OCP_FLAG	r		OCP fault indication bit.
[1]	PSFT_FLAG	r		Power stage fault indication bit.
[0]	MEM_FAULT	r		Memory load fault indication bit.

Address: 54h				
Bit[15:0]	**Bit Name**	**Access**	**Default**	**Description**
[15:3]	N/A			
[2:0]]	SYS_STATE[2:0]	r		System state machine. 0: idle 1: load memory 2: address sample 3: bias sample 4: motor start 5: fault retry 6: memory fault

Address: 55h				
Bit[15:0]	**Bit Name**	**Access**	**Default**	**Description**
[15:0]]	THETA_M[15;0]	r		Theta data from sensor.

Address: 56h				
Bit[15:0]	**Bit Name**	**Access**	**Default**	**Description**
[15:11]	N/A			
[10:0]]	IA_SENSE10:0]	r		ISA ADC result.

Address: 57h				
Bit[15:0]	**Bit Name**	**Access**	**Default**	**Description**
[15:10]	N/A			
[10:0]]	IB_SENSE[10:0]	r		ISB ADC result.

Address: 58h				
Bit[15:0]	**Bit Name**	**Access**	**Default**	**Description**
[15:10]	N/A			
[10:0]]	IB_SENSE[10:0]	r		ISC ADC result.

Address: 59h				
Bit[15:0]	**Bit Name**	**Access**	**Default**	**Description**
[15:10]	N/A			
[9:0]]	IA_BIAS_N[9:0]	f		ISA bias ADC result.

Address: 5Ah				
Bit[15:0]	**Bit Name**	**Access**	**Default**	**Description**
[15:10]	N/A			
[9:0]]	IB_BIAS_N[9:0]	r		ISB bias ADC result.

Address: 5Bh				
Bit[15:0]	**Bit Name**	**Access**	**Default**	**Description**
[15:10]	N/A			
[9:0]]	IC_BIAS_N[9:0]	r		ISC bias ADC result.

Address: 5Ch				
Bit[15:0]	**Bit Name**	**Access**	**Default**	**Description**
[15]	CURRENT_DIR	r		Current motor rotor direction.
[14:0]]	SENSOR_ SPEED[14:0]	r		Current motor speed from sensor data.

Address: 5Dh				
Bit[15:0]	**Bit Name**	**Access**	**Default**	**Description**
[15:12]	N/A			
[11:0]]	IQ_REF_ LATCH[14:0]	r		Q axis current reference.

Address: 5Eh				
Bit[15:0]	**Bit Name**	**Access**	**Default**	**Description**
[15:8]	N/A			
[7:0]]	VIN_SENSE[7:0]	r		VDC ADC result.

Address: 5Fh				
Bit[15:0]	**Bit Name**	**Access**	**Default**	**Description**
[15:10]	N/A			
[9:0]]	IIN_SENSE[7:0]	r		IDC ADC result.

Address: 69h				
Bit[15:0]	**Bit Name**	**Access**	**Default**	**Description**
[15:13]	N/A			
[11:0]]	ID_LATCH[7:0]	R		D axis current.

Address: 6Ah				
Bit[15:0]	**Bit Name**	**Access**	**Default**	**Description**
[15:13]	N/A			
[11:0]]	IQ_LATCH[7:0]	r		Q axis current.

Address: 6Bh				
Bit[15:0]	**Bit Name**	**Access**	**Default**	**Description**
[15:13]	N/A			
[11:0]]	UD _LATCH[7:0]	r		D axis voltage reference.

Address: 6Ch				
Bit[15:0]	**Bit Name**	**Access**	**Default**	**Description**
[15:13]	N/A			
[11:0]	UQ _LATCH [7:0]	r		Q axis voltage reference.

REGISTER MAPPING

Add	D[15:0]			
01h	THETA_CMD [15:0]			
02h	THETA_CMD[31:16]			
03h	THETA_CMD[47:32]			
04h	CYCLE_P[7:0]			POLE_PAIR[7:0]
05h	THETA_DIR	THETA_CMD_TYPE	FGSEL[4:0]	NSTEP[8:0]
06h	D[15]: N/A	GAIN_COE[3:0]	IQ_LMT[10:0]	
07h	D[15:11]: N/A	THETA_BIAS[10:0]		
08h	THETA_KI_L[15:0]			
09h	THETA_KI_H[15:0]			
0ah	ERR_LIMIT_H[15:0]			
0bh	ZP1_PARA_A[15:0]			
0ch	ZP1_PARA_B[15:0]			
0dh	ZP2_PARA_A[15:0]			
0eh	ZP2_PARA_B[15:0]			
0fh	D[15:9]: N/A	SAT_GAIN1[4:0]	SAT_GAIN2[3:0]	
10h	D[15:12]: N/A	ID_REF[11:0]		
11h	D[15:12]: N/A	IQ_REF[11:0]		
12h	CURRENT_KI[15:0]			
13h	CURRENT_KP[15:0]			
14h	LD_COE[15:0]			
15h	LQ_COE[15:0]			
16h	PHIR_COE[15:0]			
17h	PERIOD[15:0]			
18h	D[15:12]: N/A	MAX_PERIOD[11:0]		
19h	N/A	SH_DELAY[7:0]	DTPWM[6:0]	
1Ah	SH_CMP[15:0]			
1Bh	MIN_DELTA_CMP[7:0]	SWITCH_BLANK_TIME[7:0]		
1Ch		SPD_STEP_TH[9:0]		
1Dh		SPD_STEP_TL[9:0]		
1Eh	N/A	SPD_DOWN_STEP3[4:0]	SPD_DOWN_STEP2[4:0]	SPD_DOWN_STEP1[4:0]
1Fh	N/A	SPD_UP_STEP3[4:0]	SPD_UP_STEP2[4:0]	SPD_UP _STEP1[4:0]
20h	SPEED_CMD[15:0]			

REGISTER MAPPING *(continued)*

Add	D[15:0]										
21h	SPD_CMD_HYS[8:0]								SPD_MON_GAIN[2:0]		SPD_RANGE[3:0]
22h	N/A	SPD_MIN[14:0]									
23h	N/A	SPD_P1[14:0]									
24h	N/A	SPD_P2[14:0]									
25h	N/A	SPD_UP_P3[14:0]									
26h	N/A	SPD_DOWN_P3[14:0]									
27h	D[15:10]: N/A						IOCP[9:0]				
28h	D[15:10]: N/A		FTRT	LOCK_EN	LOCK_DRT[2:0]		FAULT_RT[2:0]		LOCK_DET[1:0]		
29h	D[15:10]: N/A		VIN_LIMIT[7:0]								VINPEN
2Ah	D[15:10]: N/A		IIN_LIMIT[9:0]								IINPEN
2Bh			BRK_IQ[11:0]								
2Ch	BRAKE		BRK_STOP_SPD[14:0]								
2Dh	D[15:11]: N/A			BIAS_SEL			CUR_BIASA[9:0]				
2Eh	D[15:10]: N/A				CUR_BIASB[9:0]						
2Fh	D[15:10]: N/A				CUR_BIASC[9:0]						
30h	D[15:4]: N/A				AD_MOD			AD_GAIN[2:0]			
31h	HOME_P1[15:0]										
32h	HOME_P2[15:0]										
33h	SDB_EN	FGHOME	MODE [1:0]	CMD_MOD [1:0]	SAM_MOD [1:0]	PWM_MOD	BRK_MOD [1:0]	EXANG	EXBRK	COM_MOD [1:0]	SPI_O_MOD
34h	D[15:13]: N/A			BAUD_RATE[12:0]							
35h	D[15:10]: N/A			ETX	ETY		BCT[7:0]				
36h	D[15:13]: N/A	KALMANN1[1:0]		ZERO_OFFSET			ZERO[9:0]				
37h	D[15:14]: N/A			[9:0]: Reserved				[3:0]: Reserved			
38h	RESERVED										
39h	RESERVED										
3Ah	RESERVED										
3Bh	RESERVED							UART_IDLE_TIME[6:0]			
3Ch	RESERVED FOR TRIM_BG										
3Dh	RESERVED FOR TRIM_BIAS										
3Eh	RESERVED FOR TRIM_ADC										

REGISTER MAPPING *(continued)*

Add	D[15:0]			
3Fh	RESERVED FOR TRIM_OSC			
40h	DATA_COMP_00[15:0]			
41h	DATA_COMP_01[15:0]			
42h	DATA_COMP_02[15:0]			
43h	DATA_COMP_03[15:0]			
44h	DATA_COMP_04[15:0]			
45h	DATA_COMP_05[15:0]			
46h	DATA_COMP_06[15:0]			
47h	DATA_COMP_07[15:0]			
48h	DATA_COMP_08[15:0]			
49h	DATA_COMP_09[15:0]			
4Ah	DATA_COMP_0A[15:0]			
4Bh	DATA_COMP_0B[15:0]			
4Ch	DATA_COMP_0C[15:0]			
4Dh	DATA_COMP_0D[15:0]			
4Eh	DATA_COMP_0E[15:0]			
4Fh	DATA_COMP_0F[15:0]			
50h	D[15:11]: NA	THETA_GEN_TIME[7:0]	THETA_GEN_EN	MEM_SECTION[1:0]
51h	D[15:13]: NA	OPEN_LOOP_DBG	CMPA_SET[11:0] (UD_SET_DBG[11:0])	
52h	D[15:13]: NA	THETA_BIAS_TIME[11:0] (UQ_SET_DBG[11:0])	THETA_BIAS_EN	

REGISTER MAPPING *(continued)*

Add	Read-Only Address							
53h					LOCK	OCP	PSFT	MEM_FAULT
54h	SYS_STATE							
55h	THETA_M[15:0]							
56h	IA_SENSE[9:0]							
57h	IB_SENSE [9:0]							
58h	IC_SENSE [9:0]							
59h	IA_BIAS_N[9:0]							
5Ah	IB_BIAS_N [9:0]							
5Bh	IC_BIAS_N [9:0]							
5Ch	Reserved	SENSOR_SPEED[14:0]						
5Dh	IQ_REF_LATCH[11:0]							
5Eh	VIN_SENSE [7:0]							
5Fh	IIN_SENSE[9:0]							
69h	ID_LATCH[11:0]							
6Ah	IQ_LATCH [11:0]							
6Bh	UD_LATCH [11:0]							
6Ch	UQ_LATCH [11:0]							

APPLICATION INFORMATION

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent the high-frequency switching current from passing through to the input. Use ceramic capacitors with X5R or X7R dielectrics for their low ESR and small temperature coefficients. A higher value capacitor is useful for reducing input voltage ripple and noise.

Setting the Switching Frequency

A higher switching frequency leads to smaller current ripple but higher switching loss of the MOSFETs. A trade-off is needed for the design. For most applications, a frequency of 20 - 80kHz is sufficient.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, follow the guidelines below.

1. Place a decoupling capacitor close to the 3.3V, 1.8V, and 0.9V pins. For most applications, a 1µF/X7R ceramic capacitor is recommended.
2. Use a wider copper for the input, output, and GND connecting wire to improve thermal performance.
3. Place GND vias near the output and input capacitor to improve thermal performance and reduce ground impedance.
4. Connect the ground copper near the external sensing resistor of the power stage to the IC's GND pin with a wide copper plane.

TYPICAL APPLICATION CIRCUIT

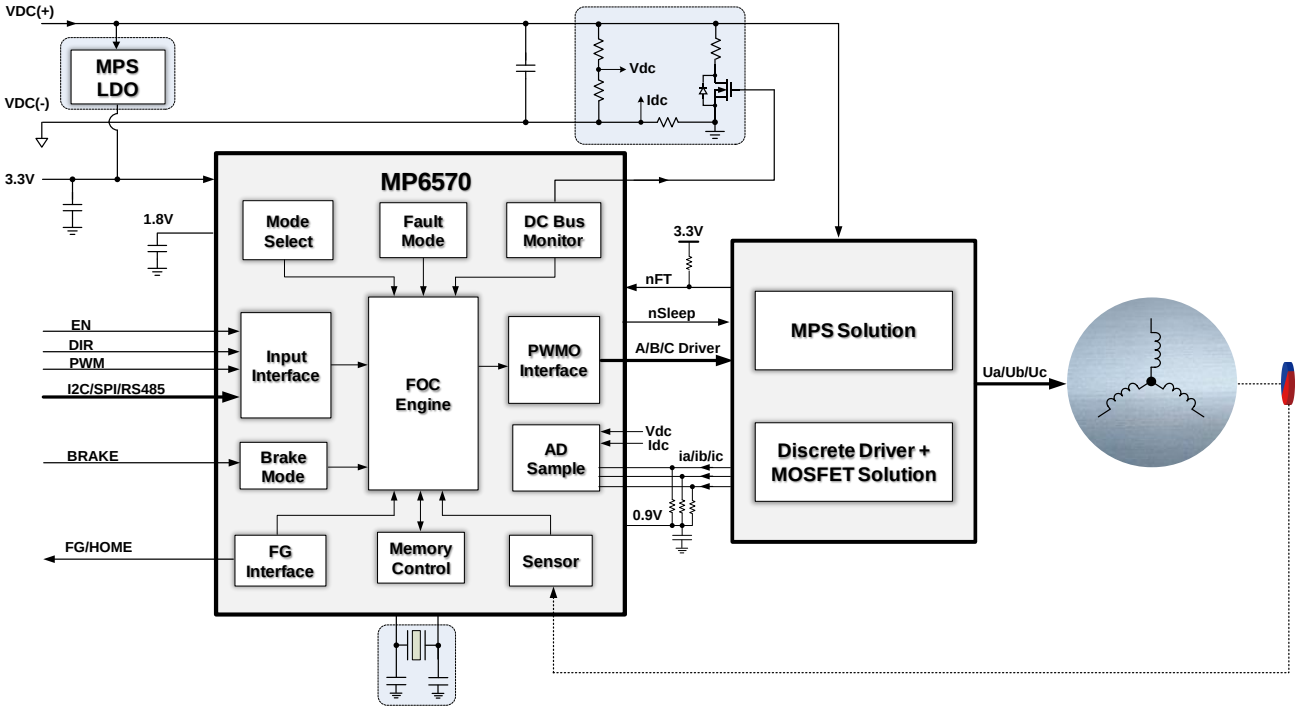
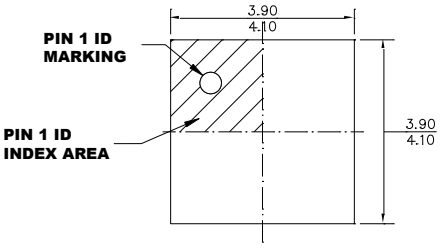


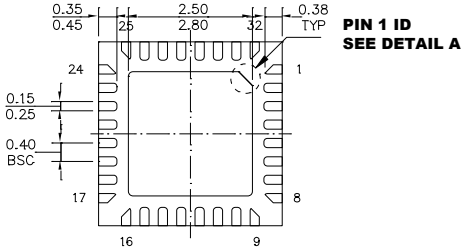
Figure 37: Typical Application Circuit

PACKAGE INFORMATION

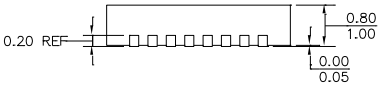
QFN-32 (4mmx4mm)



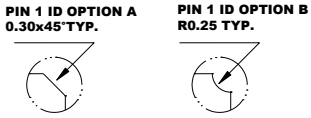
TOP VIEW



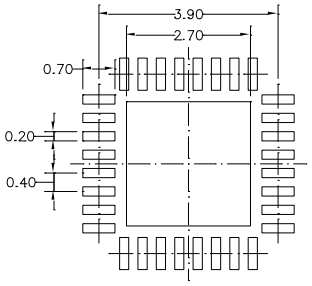
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.