MPQ6541, MPQ6541A

45V 8A Three-Phase Power Stage

The Future of Analog IC Technology

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MPQ6541 and MPQ6541A are 3-phase brushless DC motor drivers. They integrate 3 half bridges, consisting of 6 N-channel Power MOSFETs, along with pre-drivers, gate drive power supplies, and current sense amplifiers.

The MPQ6541 has ENABLE and PWM inputs for each ½-H-bridge; the MPQ6541A has separate high-side and low-side inputs. Otherwise, they are identical. References to the MPQ6541 in this document also apply to the MPQ6541A unless otherwise noted.

The MPQ6541 is able to deliver up to 15A peak current for 1 second, and 8A continuously (depending on thermal and PCB conditions). It uses an internal charge pump to generate the gate drive supply voltage for the high-side MOSFETs, and a trickle charge circuit that maintains sufficient gate drive voltage to operate at 100% duty cycle.

Internal safety features include thermal shutdown, undervoltage lockout and overcurrent protection.

The MPQ6541 is available in a 26-pin, 6mm x 6mm QFN package.

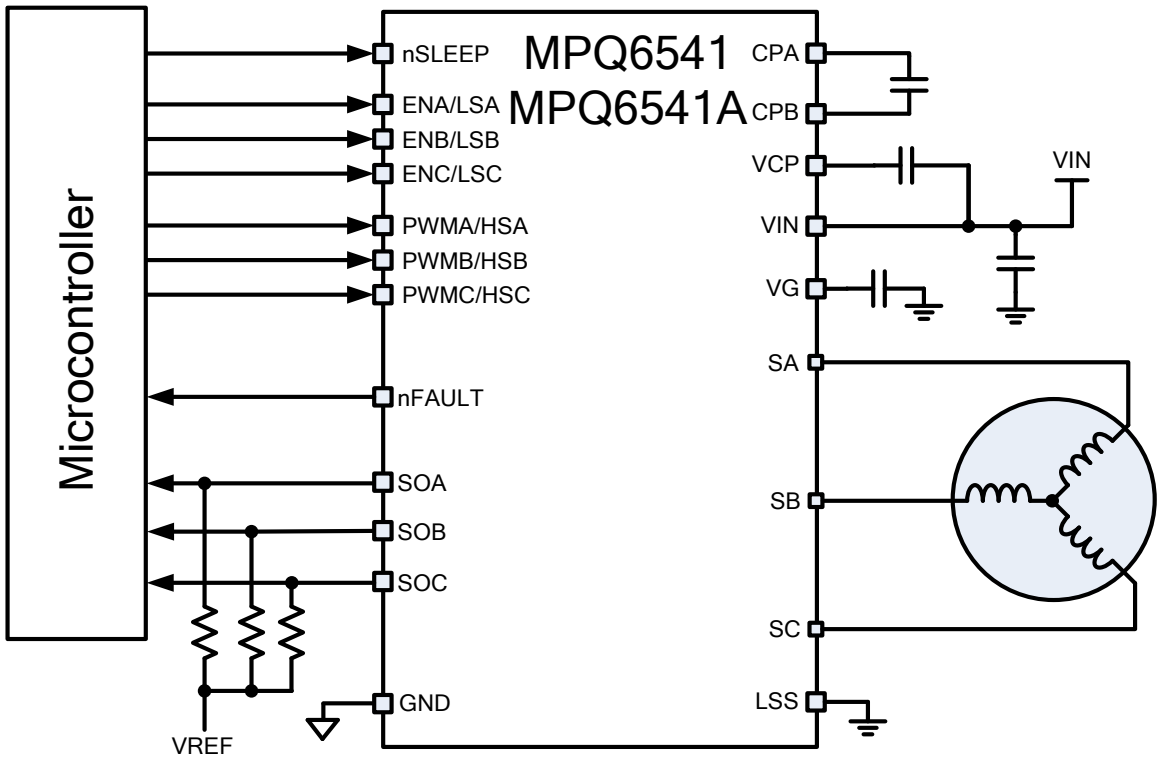
FEATURES

- AEC-Q100 Qualified
- 4.75V to 45V Operating Supply Voltage
- Three integrated half-bridge drivers
- 8A Continuous Output Current
- MOSFET On-Resistance: 13mΩ / FET
- MPQ6541 PWM & ENBL inputs
  MPQ6541A: HS & LS inputs
- Internal Charge Pump Supports 100% Duty Cycle Operation
- Automatic Synchronous Rectification
- UVLO and overvoltage protection
- Thermal Shutdown Protection
- Overcurrent Protection
- Integrated Bi-directional Current Sense Amplifiers
- Available in a FCQFN6x6-26 package

APPLICATIONS

- Brushless DC Motors
- Permanent Magnet Synchronous Motors

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number	Package	Top Marking
MPQ6541GQK*	QFN-26 (6×6 mm)	*See Below*
MPQ6541AGQK**	QFN-26 (6×6 mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MPQ6541GQK–Z).

* * For Tape & Reel, add suffix –Z (e.g. MPQ6541AGQK–Z).

TOP MARKING (MPQ6541GQK)

MPSYYWW
MP6541
LLLLLLLLL

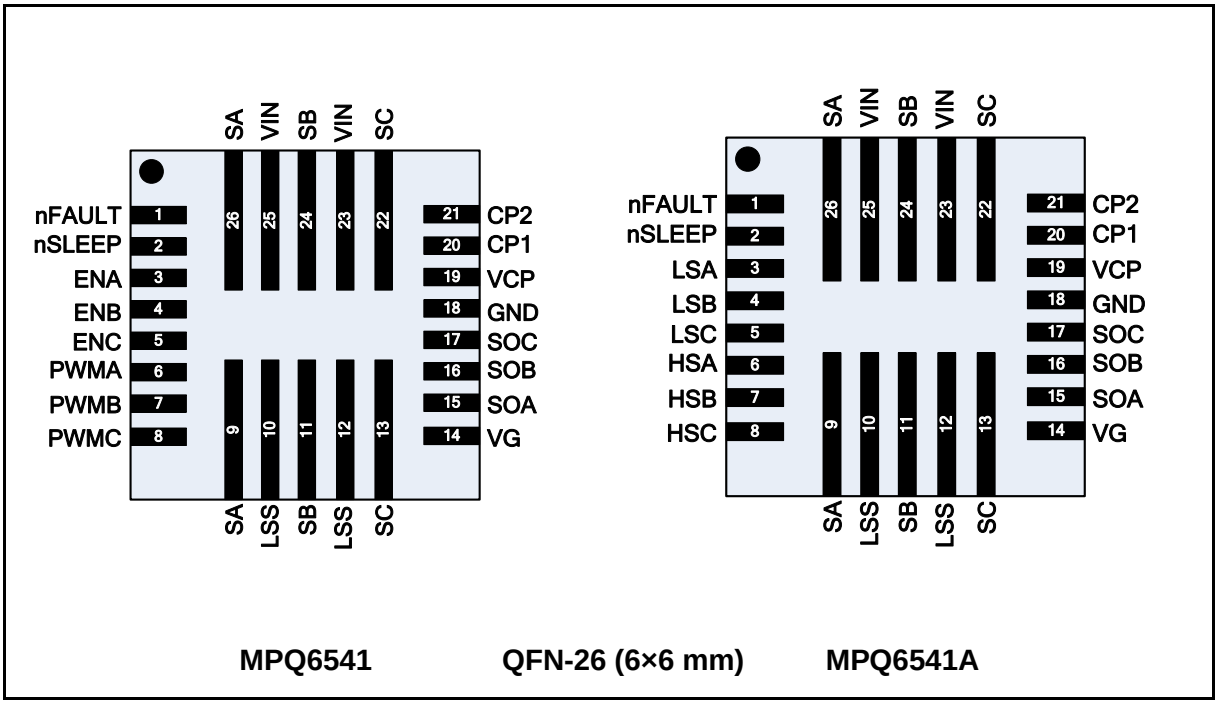
MPS: MPS prefix:
YY: year code;
WW: week code:
MP6541: part number;
LLLLLLLLL: lot number;

TOP MARKING (MPQ6541AGQK)

MPSYYWW
MP6541A
LLLLLLLLL

MPS: MPS prefix:
YY: year code;
WW: week code:
MP6541A: part number;
LLLLLLLLL: lot number;

PACKAGE REFERENCE



MPQ6541 **QFN-26 (6×6 mm)** **MPQ6541A**

ABSOLUTE MAXIMUM RATINGS (1)

Input Voltage V_{IN} ..... -0.3V to 48V
CPA ..... -0.3V to 48V
CPB, VREG ..... -0.3V to 15V
SA/B/C ..... -0.3V to 48V
ESD Rating (HBM) 2kV
All Other Pins to GND ..... -0.3V to 6.5V
Continuous Power Dissipation (T_A = +25°C) (2)
QFN26 (5x5mm) 3.47W
Storage Temperature ..... -55°C to +150°C
Junction Temperature ..... +150°C
Lead Temperature (Solder) ..... +260°C

Recommended Operating Conditions (3)

Input Voltage V_{IN} ..... +4.5V to 45V
Operating Junct. Temp (T_J) ..... -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}
QFN26 (6x6mm)	TBD ..	TBD..°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown..
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, T_A = 25°C, LSS = GND = 0V, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}		4.75		45	V
Quiescent current	I_Q	nSLEEP = 1, ENx = 0		4	8	mA
	I_{SLEEP}	nSLEEP = 0		1		µA
Control Logic						
Input logic 'low' threshold	V_{IL}				0.8	V
Input logic 'high' threshold	V_{IH}		2			V
Logic input current	$I_{IN(H)}$	V = 5V	-20		20	µA
	$I_{IN(L)}$	V = 0V	-20		20	µA
Power up delay	t_{PUD}	At V_{IN} rising or nSLEEP rising		1		mS
Internal pull down resistance	R_{PD}	All logic Inputs		500		kΩ
nFAULT pull down R_{ON}	$R_{ON(NFAULT)}$			15		Ω
Protection Circuits						
UVLO threshold	V_{UVLO}	V_{IN} rising	TBD		4.75	V
UVLO hysteresis	ΔV_{UVLO}			400		mV
OVP threshold	V_{OVP}	V_{IN} rising	45	48	TBD	V
OVP hysteresis	ΔV_{OVP}			500		mV
HS OCP threshold	$I_{OCP(HS)}$		16	20	TBD	A
LS OCP threshold	$I_{OCP(LS)}$		16	20	TBD	A
OCP deglitch time (Note 1)	t_{OCD}			2		µs
OCP retry time	t_{OCR}			2		ms
Thermal Shutdown	T_{TSD}			150		°C
Thermal Shutdown Hysteresis	ΔT_{TSD}			25		°C
Current sense						
Current sense ratio				1/10,000		A/A
Current sense output current	I_{SOx}	LS FET current = 1A		100		µA
		LS FET current = -1A		-100		µA
Current sense output voltage swing		I_{SOx} = +2mA	0		TBD	V
		I_{SOx} = -2mA	TBD		5	
		I_{SOx} = +100µA	0		TBD	
		I_{SOx} = -100µA	TBD		5	
Outputs						
HS FET on resistance	$R_{ON(HS)}$	I_{OUT} = 1A, T_J = 25°C		13		mΩ
		I_{OUT} = 1A, T_J = 150°C		TBD		
LS FET on resistance	$R_{ON(LS)}$	I_{OUT} = 1A, T_J = 25°C		13		
		I_{OUT} = 1A, T_J = 150°C		TBD		
Output rise time (Note 1)		I_{OUT} = 1A		2		V/nS
Output fall time (Note 1)		I_{OUT} = 1A		1.5		V/nS
Charge pump output voltage	V_{CP}			V_{IN} + 5		V
V_{CP} switching freq	f_{CP}		1800	2000		kHz

Note 1 – derived from bench characterization – not production tested

TYPICAL CHARACTERISTICS

TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section.
T_A=25°C, unless otherwise noted.

PIN FUNCTIONS

QFN26 Pin #	MPQ6541 Name	MPQ6541A Name	Description
1	nFAULT		Fault Indication. Open-drain output type, logic low when in fault condition.
2	nSLEEP		Sleep Mode Input. Logic low to enter low-power sleep mode; logic high for normal operation. Internal pull down.
3	ENA	-	Enable Pin for Phase A
	-	LSA	Enable Low-side FET for Phase A
4	ENB	-	Enable Pin for Phase B
	-	LSB	Enable Low-side FET for Phase B
5	ENC	-	Enable Pin for Phase C
	-	LSC	Enable Low-side FET for Phase C
6	PWMA	-	PWM Input Pin for Phase A
	-	HSA	Enable High-side FET for Phase A
7	PWMB	-	PWM Input Pin for Phase B
	-	HSB	Enable High-side FET for Phase B
8	PWMC	-	PWM Input Pin for Phase C
		HSC	Enable High-side FET for Phase C
9,26	SA		Phase A output
10,12	LSS		Low-side Source Connection for Phase A,B,C. Must be connected directly to GND.
11,24	SB		Phase B output
13,22	SC		Phase C output
14	VG		Low-side gate drive voltage bypass. Connect a 4.7uF 10V X7R ceramic capacitor to ground.
15	SOA		Current Sense Output for Phase A
16	SOB		Current Sense Output for Phase B
17	SOC		Current Sense Output for Phase C
18	GND		Ground
19	VCP		Charge Pump Output. Connect a 1uF 16V X7R ceramic capacitor to VIN
20	CP1		Charge Pump Capacitor Pins. Connect a 100nF X7R ceramic capacitor rated for at least VIN between CP1 and CP2
21	CP2		
23,25	VIN		Input Power

BLOCK DIAGRAM

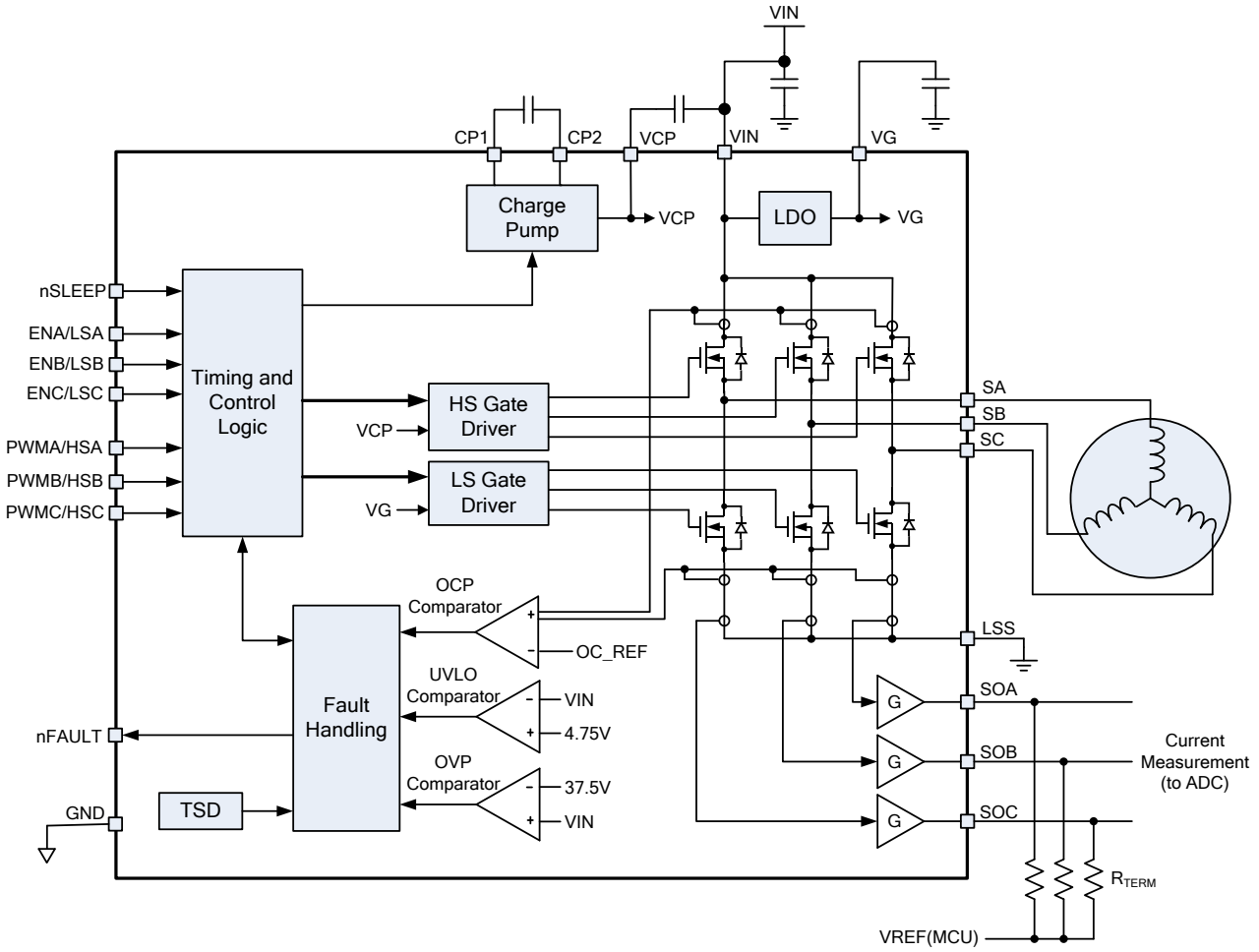


Figure 1: Function Block Diagram

OPERATION

Input Logic

The MP6542 has logic input pins ENA, ENB, and ENC, which enable the outputs SA, SB, and SC. When ENx is low, the corresponding output is disabled (output is high impedance), and the PWM input on that phase is ignored. When ENx is high, the output is enabled, and the PWM input controls the state of the output. Refer to Table 1 for the logic truth table.

Table 1: Input Logic Truth Table

ENx	PWMx	Sx
H	H	VIN
H	L	GND
L	X	High Impedance

The MPQ6541A has separate inputs that are used to enable the HS and LS FETs of each phase independently. Refer to Table 2 for the logic truth table.

Table 2: Input Logic Truth Table

HSx	LSx	Sx
L	L	High Impedance
L	H	GND
H	L	VIN
H	H	High Impedance

Note that the logic inputs have internal weak pulldown resistors.

nSLEEP Operation

Driving nSLEEP low will put the device into a low power sleep state. In this state, all the internal circuits are disabled. All inputs are ignored when nSLEEP is active low. When waking up from sleep mode, some time (approximately 1 ms) needs to pass before the device will respond to inputs. The nSLEEP input has a weak pulldown resistor.

Current Sense Amplifiers

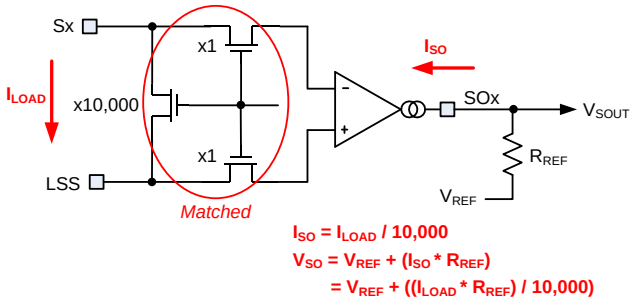
The current flowing in each of the three outputs is sensed by internal current sensing circuits. An output pin for each phase sources or sinks a current that is proportional to the current flowing in each phase. Note that only current flowing in the low-side FET is sensed, and that it is sensed in both the forward and reverse direction.

To convert this current into a voltage (to input to an A/D converter, for example) a termination resistor (R_{TERM}) is used to a reference voltage. When there is no current flowing, the resultant output will be equal to the reference voltage; when current is flowing, the voltage will be above or below the reference voltage according to the following equation:

$$V = V_{TERM} + (R_{TERM} * I_{OUT}) / 10{,}000$$

To terminate the outputs when using an A/D converter with inputs that are ratiometric to its supply voltage, use two equal value resistors to the ADC supply and ground. The resulting ADC code will be half scale at zero current.

The diagram below shows a simplified drawing of the current measurement circuit.



Automatic Synchronous Rectification

When driving current through an inductive load, when the output MOSFETs are both turned off, recirculation current must continue to flow. This current normally is passed through the MOSFET body diodes. To prevent excess power dissipation in the body diodes, the MPQ6541 implements an automatic synchronous rectification feature.

When both the HS and LS MOSFETSs are turned off, if the voltage on an Sx output pin is driven below ground, the LS MOSFET is turned on until the current flowing through it reaches near zero, or until the HS MOSFET is commanded to turn on. Similarly, if the Sx pin rises above VIN, the HS MOSFET is turned on until the current reaches near zero, or the LS MOSFET is turned on.

nFAULT Output

MPQ6541 provides an nFAULT output pin which is driven active low in the case of a fault condition, such as overcurrent (OCP) or overtemperature

(OTP). This pin is an open-drain output and must be pulled up by an external pullup resistor.

Input UVLO Protection

If at any time the voltage on the VIN pin falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled and internal logic will be reset. The nFAULT pin will not be driven active low. Operation will resume when VIN rises above the UVLO threshold.

Overvoltage Protection

If VIN exceeds the overvoltage protection threshold, all outputs of the device will be disabled. The nFAULT pin will not be driven active low. Operation will automatically resume when VIN falls below the OVP threshold.

Thermal Shutdown

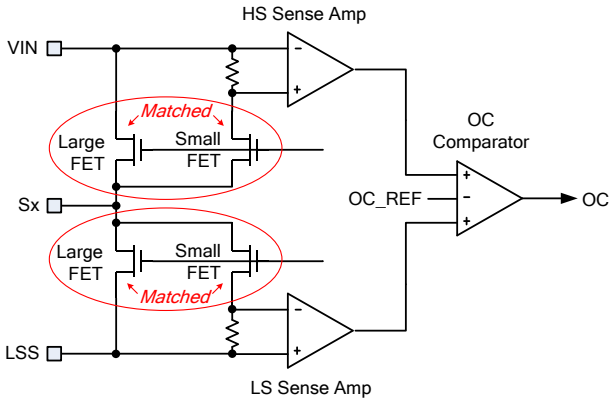
If the die temperature exceeds safe limits, all output FETs will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume.

Overcurrent Protection

The overcurrent protection circuit limits the current through each FET by disabling its gate driver. If the overcurrent limit threshold is reached and lasts for longer than the overcurrent deglitch time, all six output FETs will be disabled (outputs become high impedance) and the nFAULT pin will be driven low. During this time current will be recirculated through the body diodes. The outputs will be disabled for 2ms (typ), then are automatically re-enabled.

Over-current conditions on both high and low side devices; i.e., a short to ground, supply, or across the motor winding will all result in an over-current shutdown.

A simplified diagram of the OCP circuit for one output is shown below.



Charge Pump and VG Regulator

An internal LDO regulator generates a low-side gate drive voltage of approximately 5.5V. A bypass capacitor of 4.7µF – 10µF is required from the VG pin to ground.

A charge pump is used to generate the gate drive for the high-side FETs. The charge pump requires two external capacitors: a 0.1µF ceramic capacitor rated for at least VIN between the CP1 and CP2 pins, and a 1µF ceramic capacitor rated for at least 10V between VIN and VCP.

APPLICATIONS INFORMATION

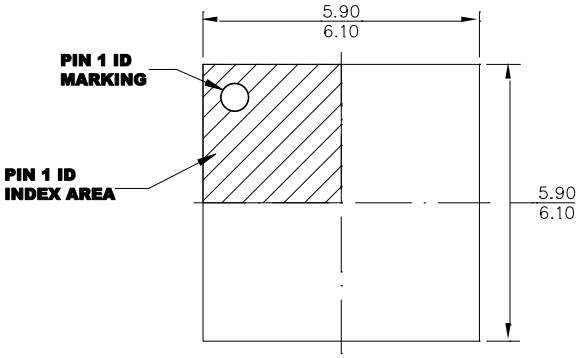
Charge Pump External Capacitors

The external charge pump capacitors should be selected as shown in the table below:

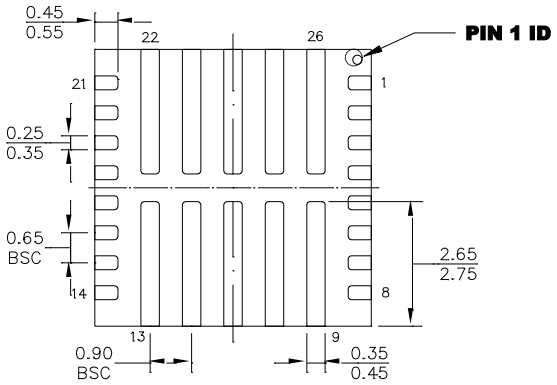
	Min	Nom	Max	Unit
CP1 - CP2 capacitance		0.1		µF
CP1 - CP2 cap voltage	V_{IN}			V
V_{CP} - V_{IN} capacitance		1		µF
V_{CP} - V_{IN} cap voltage	10			V
V_G capacitance	4.7		10	µF
V_G cap voltage	10			V

PACKAGE INFORMATION

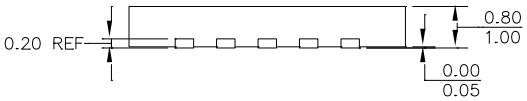
QFN-26 (6×6 mm)



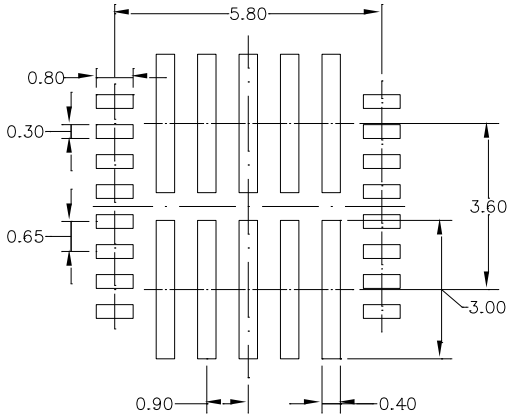
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO220.
4) DRAWING IS NOT TO SCALE.