

8Gb (x16 x 2 channel) Mobile LPDDR4/LPDDR4X

FEATURES

- Configuration:
 - 256Mb x16 x 2 channels
 - 2channels composition per device
 - 8 internal banks per each channel
- Low-voltage Core and I/O Power Supplies
 - VDD1 = 1.70-1.95V
 - VDD2 = 1.06-1.17V
 - VDDQ = 1.06-1.17V (LPDDR4)
 - VDDQ = 0.57-0.65V (LPDDR4X)
- LVSTL(Low Voltage Swing Terminated Logic) I/O Interface
- Internal VREF and VREF Training
- Dynamic ODT :
 - DQ ODT :VSSQ Termination
 - CA ODT :VSS Termination
- Max. Clock Frequency : 1.6GHz (3.2Gbps)
- 16n Pre-fetch DDR architecture
- Single data rate (multiple cycles) command/ address bus
- Bidirectional/differential data strobe per byte of data (DQS/DQS#)
- Programmable burst lengths (16 or 32)
- ZQ Calibration
- Operation Temperature
 - Industrial (T_c = -40°C to 85°C)
 - Automotive, A1 (T_c = -40°C to 85°C)
 - Automotive, A2 (T_c = -40°C to 105°C)
- Clock-Stop capability

ADVANCED INFORMATION APRIL 2019

DESCRIPTION

The IS43/46LQ32256A and IS43/46LQ32256AL are 8Gbit CMOS LPDDR4 SDRAM. The device is organized as 2 channels per device, and individual channel is 8-banks and 16-bits. This product uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 16N prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. This product offers fully synchronous operations referenced to both rising and falling edges of the clock. The data paths are internally pipelined and 16n bits prefetched to achieve very high bandwidth.

- On-chip temperature sensor whose status can be read from MR4
- 200-ball x32 Discrete Package (0.80mm x 0.65mm)

ADDRESS TABLE *

Parameter	
# of Channel	2
Row Addresses	R0-R14
Column Addresses	C0-C9
Bank Addresses	BA0-BA2

Note: Address information is per channel base.

KEY TIMING PARAMETERS

Speed Grade	Freq. (MHz)	Data Rate (Mb/s)	Write Latency		Read Latency	
			Set A	Set B	DBI OFF	DBI ON
-062	1600	3200	14	26	28	32
-075	1333	2666	12	22	24	28
-093	1066	2133	10	18	20	22

Note: Other clock frequencies/data rates supported; please refer to AC timing tables.

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- the risk of injury or damage has been minimized;
- the user assume all such risks; and
- potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

200-ball x32 Discrete Package, 0.80mm x 0.65mm using MO-311

0.65mm Pitch

NOTE 3 The ODT_CA pin is ignored by LPDDR4X devices.

2. INPUT/OUTPUT FUNCTIONAL DESCRIPTION

2.1 PAD DEFINITION AND DESCRIPTION

Table 2.1 — Pad Definition and Description

Symbol	Type	Description
CK_t_A, CK_c_A, CK_t_B, CK_c_B	Input	Clock: CK_t and CK_c are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to CK. Each channel (A & B) has its own clock pair.
CKE_A CKE_B	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code. Each channel (A & B) has its own CKE signal.
CS_A CS_B	Input	Chip Select: CS is part of the command code. Each channel (A & B) has its own CS signal.
CA[5:0]_A CA[5:0]_B	Input	Command/Address Inputs: CA signals provide the Command and Address inputs according to Table 63 — Command Truth Table. Each channel (A&B) has its own CA signals.
ODT_CA_A ODT_CA_B	Input	LPDDR4 CA ODT Control: The ODT_CA pin is used in conjunction with the Mode Register to turn on/off the On-Die-Termination for CA pins. LPDDR4X CA ODT Control: The ODT_CA pin is ignored by LPDDR4X devices. CA ODT is fully controlled through MR11 and MR22. The ODT_CA pin shall be connected to either VDD2 or VSS.
DQ[15:0]_A, DQ[15:0]_B	I/O	Data Input/Output: Bi-direction data bus.
DQS[1:0]_t_A, DQS[1:0]_c_A, DQS[1:0]_t_B, DQS[1:0]_c_B	I/O	Data Strobe: DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and must arrive prior to Data. Each byte of data has a Data Strobe signal pair. Each channel (A & B) has its own DQS strobes.
DMI[1:0]_A, DMI[1:0]_B	I/O	Data Mask Inversion: DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel (A & B) has its own DMI signals.
ZQ	Reference	Calibration Reference: Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to V _{DDQ} through a 240Ω ± 1% resistor.
V _{DDQ} , V _{DD1} , V _{DD2}	Supply	Power Supplies: Isolated on the die for improved noise immunity.
V _{SS} , V _{SSQ}	GND	Ground Reference: Power supply ground reference
RESET_n	Input	RESET: When asserted LOW, the RESET_n signal resets both channels of the die.

ORDERING INFORMATION – Valid Part Numbers

IS 43 LQ 32256 _ A _ - 062 B L I

TEMPERATURE RANGE

I = Industrial (-40°C to +85°C)

A1 = Automotive A1 Grade (-40°C to +85°C)

A2 = Automotive A2 Grade (-40°C to +105°C)

PACKAGING CONTENT

L = RoHS compliant

Package Type

B = 200-ball BGA

Speed Grade

093 = 1066MHz

075 = 1333MHz

062 = 1600MHz

VDDQ

Blank = Regular VDDQ (LPDDR4)

L = Low VDDQ (LPDDR4X)

Die GenerationA = 1st Generation**ECC support**

Blank = No ECC

Density

32256 = 256Mb x 32 (8Gb)

Device Type

LQ = LPDDR4 DRAM

Product Family

43 = DDR DRAM

46 = Automotive DDR DRAM

ISSI Prefix

IS = Integrated Silicon Solution Inc.

ORDERING INFORMATION, 256Mb x 32 LPDDR4Industrial Range: $T_c = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Clock	Speed Grade	Order Part No.	Package
1066 MHz	-093	IS43LQ32256A-093BLI	200 ball FBGA, lead free
1333 MHz	-075	IS43LQ32256A-075BLI	200 ball FBGA, lead free
1600 MHz	-062	IS43LQ32256A-062BLI	200 ball FBGA, lead free

Automotive, A1 Range: $T_c = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Clock	Speed Grade	Order Part No.	Package
1066 MHz	-093	IS46LQ32256A-093BLA1	200 ball FBGA, lead free
1333 MHz	-075	IS46LQ32256A-075BLA1	200 ball FBGA, lead free
1600 MHz	-062	IS46LQ32256A-062BLA1	200 ball FBGA, lead free

Automotive, A2 Range: $T_c = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$

Clock	Speed Grade	Order Part No.	Package
1066 MHz	-093	IS46LQ32256A-093BLA2	200 ball FBGA, lead free
1333 MHz	-075	IS46LQ32256A-075BLA2	200 ball FBGA, lead free
1600 MHz	-062	IS46LQ32256A-062BLA2	200 ball FBGA, lead free

ORDERING INFORMATION, 256Mb x 32 LPDDR4XIndustrial Range: T_c = -40°C to +85°C

Clock	Speed Grade	Order Part No.	Package
1066 MHz	-093	IS43LQ32256AL-093BLI	200 ball FBGA, lead free
1333 MHz	-075	IS43LQ32256AL-075BLI	200 ball FBGA, lead free
1600 MHz	-062	IS43LQ32256AL-062BLI	200 ball FBGA, lead free

Automotive, A1 Range: T_c = -40°C to +85°C

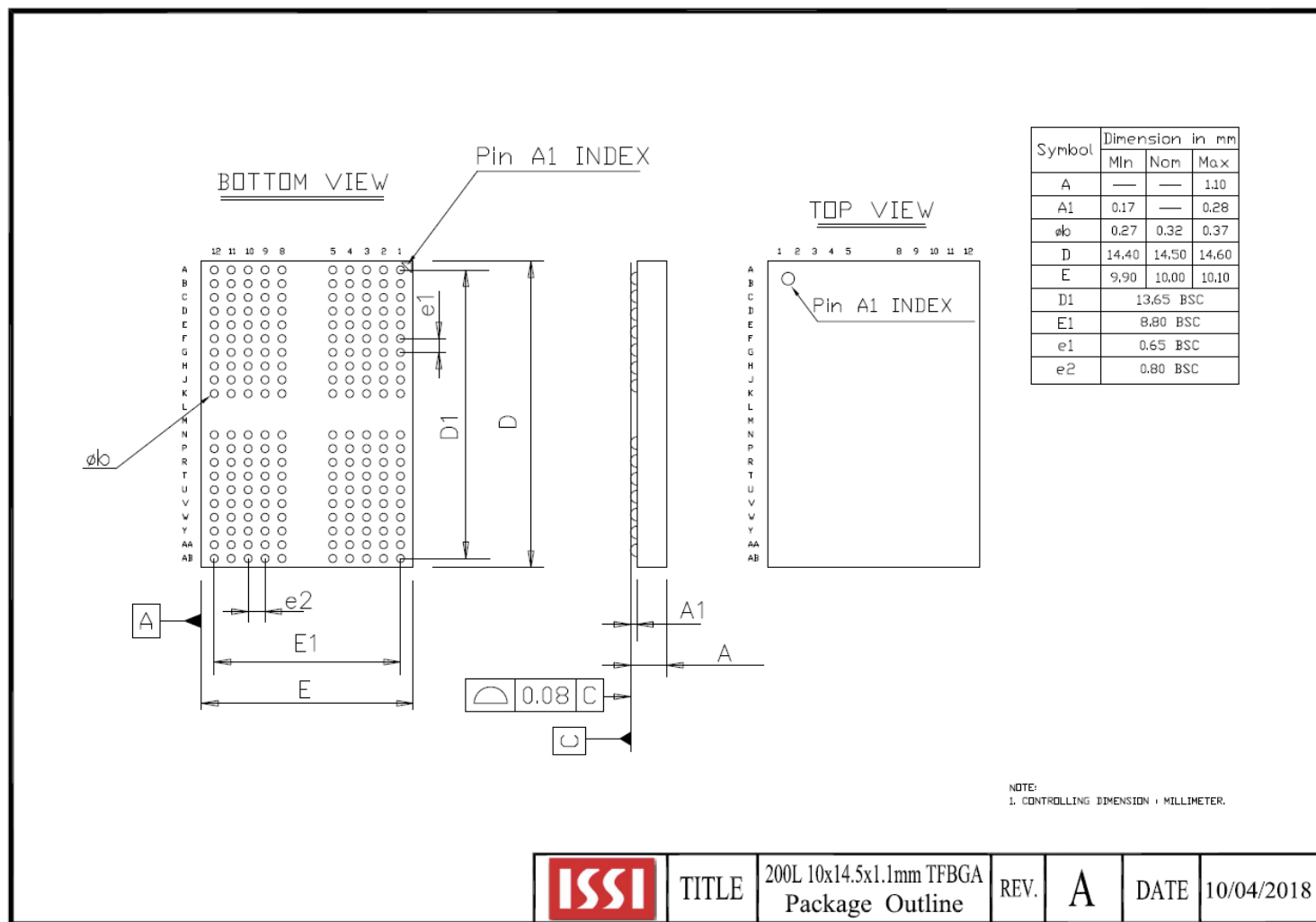
Clock	Speed Grade	Order Part No.	Package
1066 MHz	-093	IS46LQ32256AL-093BLA1	200 ball FBGA, lead free
1333 MHz	-075	IS46LQ32256AL-075BLA1	200 ball FBGA, lead free
1600 MHz	-062	IS46LQ32256AL-062BLA1	200 ball FBGA, lead free

Automotive, A2 Range: T_c = -40°C to +105°C

Clock	Speed Grade	Order Part No.	Package
1066 MHz	-093	IS46LQ32256AL-093BLA2	200 ball FBGA, lead free
1333 MHz	-075	IS46LQ32256AL-075BLA2	200 ball FBGA, lead free
1600 MHz	-062	IS46LQ32256AL-062BLA2	200 ball FBGA, lead free

PACKAGE INFORMATION

200-ball FBGA



TITLE

200L 10x14.5x1.1mm TFBGA
Package Outline

REV.

A

DATE

10/04/2018